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Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST

M. Omaña, D. Rossi, F. Fuzzi, C. Metra, C. Tirumurti and R. Galivanche

***Abstract*—The generation of significant power droop (PD) during at-speed test performed by Logic BIST is a serious concern for modern ICs. In fact, the PD originated during test may delay signal transitions of the circuit under test (CUT): an effect that may be erroneously recognized as delay faults, with consequent erroneous generation of test fails, and increase in yield loss. In this paper, we propose a novel, scalable approach to reduce the PD during at-speed test of sequential circuits with scan-based Logic BIST using the Launch-On-Capture scheme. This is achieved by reducing the activity factor of the CUT, by proper modification of the test vectors generated by the Logic BIST of sequential ICs. Our scalable solution allows us to reduce PD to a value similar to that occurring during the CUT in field operation, without increasing the number of test vectors required to achieve a target Fault Coverage (FC). We present a hardware implementation of our approach that requires limited area overhead. Finally, we show that, compared to recent alternative solutions providing a similar PD reduction, our approach enables a significant reduction of the number of test vectors (by more than 50%), thus the test time, to achieve a target FC.**

***Index Terms*— Logic BIST, Power Droop, Test, Microprocessor**

I. Introduction

THE aggressive scaling of microelectronic technology is enabling the fabrication of increasingly complex ICs. Together with several benefits (improved performance, decreased cost per function, etc.), this poses serious challenges in terms of test and reliability [1, 2, 3, 4, 5, 6, 7]. In particular, during at-speed test of high performance microprocessors, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during in field operation [5, 8, 9, 11, 13, 14, 15]. Consequently, excessive power droop (PD) may be generated, which will slow down the circuit under test (CUT) signal transitions. This phenomenon is likely to be erroneously recognized as due to delay faults. As a result, a false test fail will be generated, with consequent increase in yield loss [9, 13, 16].

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At-speed test of logic blocks is nowadays frequently performed using Logic BIST (LBIST) [2, 8, 9, 10], which can take the form of either combinational LBIST, or scan-based LBIST, depending on whether the CUT is a combinational circuit, or a sequential one with scan [8, 12]. In case of scan-based LBIST, two basic capture-clocking schemes exist [8, 12]: the launch-on-shift (LOS) scheme, and the launch-on-capture (LOC) scheme. In LOS schemes, test vectors are applied to the CUT at the last clock (CK) of the shift phase, and the CUT response is sampled on the scan chains at the following capture CK. In the LOC scheme, instead, test vectors are first loaded into the scan-chains during the shift phase; then, in a following capture phase, they are first applied to the CUT at a launch CK, and the CUT response is captured on the scan chains in a following capture CK [8].

In this paper, we consider the case of sequential CUTs with scan-based LBIST adopting a LOC scheme, which is frequently adopted for high performance microprocessors. They suffer from the PD problems discussed above, especially during the capture phase, due to the high AF of the CUT induced by the applied test patterns.

Solutions allowing designers to reduce PD during the capture phase in scan-based LBIST are therefore needed. While several approaches have been proposed to reduce PD for combinational LBIST (e.g., [8, 11, 13]), only a few solutions exist for scan-based LBIST [2, 9, 17-21].

In [2], PD is reduced by a multi-cycle BIST scheme with partial observation. This approach does not impact FC (actually it presents a slight FC increase of 5% compared to conventional scan-based-LBIST), but enables to reduce PD by the 33% only, compared to conventional scan-based-LBIST.

In [9], PD can be reduced of more than 50% by alternately disabling groups of scan chains during test. However, this approach implies an increase of more than 90% in the number of test vectors required to achieve a target FC, with consequent increase in test time (TT), compared to conventional scan-based LBIST.

In [21], a test pattern generator with a pre-selected toggling level (PRESTO) is presented. It enables more than 50% reduction in the AF of the scan chains by preselecting the number of shift cycles during which the scan chains are loaded with constant logic values. However, it requires more than 60% increase in the number of test vectors (thus TT) to achieve the same FC as with conventional scan-based LBIST.

The solution in [17, 18] relies on inserting an additional phase, namely a “burst” phase, between each shift and capture

phase. Such a burst phase aims at increasing the current drawn from the power supply, up to a value similar to that absorbed by the CUT during capture phases. This way, the inductive component of PD occurs during the burst phase, and vanishes before the following capture phase. This solution causes an increase in both the total power consumed during test and TT.

In [19, 20], we recently proposed alternative approaches to reduce PD during scan-based LBIST, for the LOS scheme. They enable to reduce PD (up to 50% in [19], and up to 87% in [20]) by increasing the correlation between adjacent bits of the scan chains. However, these approaches do not increase the correlation between test vectors applied at following capture cycles, so that they are not effective in reducing PD during scan-based LBIST adopting the LOC scheme.

In this paper, we propose a novel, scalable approach to reduce PD during capture phases of scan-based LBIST, thus reducing the probability to generate false test fails during test. Similarly to the solutions in [8, 11], our approach reduces the AF of the CUT compared to conventional scan-based LBIST, by properly modifying the test vectors generated by the LFSR. Our approach is somehow similar to re-seeding techniques (e.g., that in [22]), to the extent that the sequence of test vectors is properly modified in order to fulfill a given requirement that, however, is not to increase FC (as it is usually the case for re-seeding), but to reduce PD. The basic idea behind our approach (in its non-scalable version) was introduced in [23].

In our proposed scalable approach, one (or more) test vector(s) to be applied to the CUT according to conventional scan-based LBIST is (are) replaced by new, proper test vector(s), hereinafter referred to as substitute test (ST) vector(s). The ST vector(s) is (are) generated based on the test vectors to be applied at previous and future capture phases, in order to reduce the maximum number of transitions between any two following test vectors. This way, the CUT AF and PD are reduced compared to the original test sequence [11]. We consider the presence of a phase shifter (PS), which is usually adopted in scan-based LBIST to reduce the correlation among the test vectors applied to adjacent scan-chains [10]. As shown in [2], all test vectors to be applied at previous and future capture phases to any scan-chain are usually given at proper outputs of the PS, or the PS can be easily modified to provide them. In our approach, this property is exploited to enable its low cost hardware implementation. However, our approach can be adopted also if the PS does not provide the previous and future test vectors for all scan-chains, or if the scan-based LBIST does not present a PS. Indeed, as shown in Section IV, the previous and future test vectors of scan-chains can be obtained as a linear combination of proper LFSR outputs.

Our approach is scalable in the achievable PD reduction. Therefore, test engineers could choose the proper AF in order to avoid that: a) faulty chips are tested as good (due to an induced too low AF, lower than that experienced during normal operation) and b) good chips are tested as faulty (due to an induced excessive AF, higher than that experienced during normal operation). PD scalability is obtained by scaling the number of ST vectors to be applied between original test vectors. We will prove that our approach can reduce the maximum AF between following capture phases from 50% (one ST vector only) to 89% (10 ST vectors) compared to conventional scan-based LBIST. This is achieved without increasing the number of test vectors (thus TT) over conventional scan-based LBIST, for a given target FC. Moreover, our approach requires a very limited area overhead compared to conventional scan-based LBIST, which ranges from approximately 1.5% (1 ST vector), to approximately 14% (10 ST vectors). Additionally, our solution requires substantially less test vectors (thus TT) to achieve a target FC compared to the alternative solutions in [9, 21].

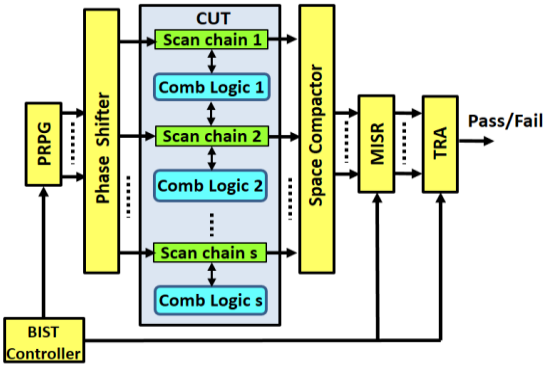

Fig. 1. Schematic representation of the considered scan-based LBIST architecture.

The remainder of this paper is organized as follows. In Section II, we describe the considered conventional scan-based LBIST. In Section III, we introduce our approach for PD reduction during capture phases. In Section IV, we show a possible hardware implementation of our approach. In Section V, we evaluate the cost of our approach and compare it to conventional scan-based LBIST and to the solutions in [9, 21]. Finally, some conclusions are drawn in Section VI.

II. Considered Scenario

We consider the conventional scan-based LBIST (Conv-LBIST) architecture shown in Fig. 1 [8, 10, 11, 12, 14]. The state flip-flops of the CUT are scan flip-flops, arranged into many scan chains (*s* scan chains in Fig. 1).

The Pseudo-Random Pattern Generator (PRPG) is implemented by an LFSR [10, 12, 14]. The PS, which reduces the correlation among the test vectors applied to adjacent scan-chains [10], is composed by an XOR network expanding the number of outputs of the LFSR to match the number of scan chains *s* [10]. As discussed more in details in Section IV, the PS gives to its output the current LFSR output configuration, together with future/past configurations at each shift CK.

The Space Compactor compacts the outputs of the *s* scan chains to match the number of inputs of the MISR. The MISR, the Test Response Analyzer (TRA) and the BIST Controller are the same as in combinational scan-based LBIST [8, 12].

As for the scan flip-flops, our approach requires that, during shift phases, they maintain the last test vector applied to the CUT at their outputs. This is guaranteed by the scan-flip flop in [24], which is frequently employed in microprocessors [24], and considered here as significant example. However, this can

be also achieved with other different scan flip-flops. The internal structure of this flip-flop is shown in Fig. 2. It consists of two sub-blocks, namely the scan portion and the system portion, each consisting of a master-slave flip-flop composed by two latches (Latches LA and LB for the scan portion, and latches PH2 and PH1 for the system portion) [24]. The latches have two clocks, and sample one out of two input data lines, depending on which clock is active [24].

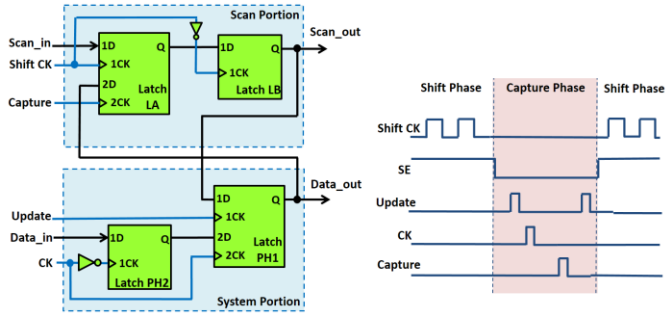

Fig. 2. Considered scan flip-flop in [24] and signals' timing.

The clocking scheme adopted to implement a LOC strategy is also reported in Fig. 2. It consists of a shift phase (scan enable - SE=1) and a capture phase (scan enable - *SE*=0). During the shift phase, a new test vector is loaded in the scan chains after *n* shift CKs, where *n* is the number of scan flip-flops of the longest scan chain. At each *shift CK*, a new bit of the test vector present at the *scan_in* of latch LA is shifted to the *scan_out* of latch LB. We refer hereinafter to T_i^m as the part of the test vector that is loaded in the *m-th* scan chain ($m = 1..s$) and is applied to the CUT at the *i-th* capture phase. During the capture phase, a pulse is first applied on the *Update* clock (launch CK) to load the test vector (loaded on LB latches at the previous shift phase) on the PH1 latches. Thus, after the pulse on *Update*, the test vector T_i^m ($m=1...s$) is applied to the CUT. Then, a pulse is applied on *CK* (capture CK) to sample the CUT response on PH1 latches. Then, the CUT response is copied to the latches LA (to enable to shift it out at the following shift phase) by applying a pulse on the *Capture* clock (Fig. 2). Finally, another pulse is applied on *Update* to load T_i^m again on the latches PH1. Since *Update* is not asserted during the following shift phase, T_i^m is maintained at the inputs of the CUT until the following test vector T_{i+1}^m is applied. Therefore, in the LOC clocking scheme in Fig. 2, the CUT AF (thus PD) that occurs between the launch and capture CKs (i.e., between *Update* and *CK* pulses) and that may generate false test fails during testing, is proportional to the number of transitions between following test vectors T_i^m and T_{i+1}^m.

III. Proposed Scalable Approach

As we introduced in Section I, the goal of our approach is to reduce the PD that may generate false test fails during at-speed test with scan-based LBIST. Such a PD occurs after the application of a new test vector to the CUT. This occurs at the launch CK (*Update* pulse in Fig. 2) within capture phases. The generated PD is proportional to the CUT AF induced by the application of a new test vector, which in turn is depends on the AF of the scan flip-flops' outputs [8]. For the considered scan flip-flops (Fig. 2), such an AF depends on the number of flip-flops' outputs switching when the new test vector is applied. Therefore, the target of our approach is to reduce the number of flip-flops' outputs transitions occurring after the application of a new test vector to the CUT.

In order to derive a mathematical description of our proposed solution, we make the following simplifying assumptions for Conv-LBIST: a) all scan chains have the same number of scan flip-flops; b) the maximum AF between two following test vectors T_i^m and T_{i+1}^m is the same for all scan chains ($m=1..s$). However, by logic level simulations performed by the Synopsys Design Compiler tool, we have verified that our approach can achieve the same AF reduction also if such simplifying hypotheses are not satisfied.

A. Approach with 1 Substitute Test Vector

For each scan chain *m* ($m = 1...s$), one ST vector ST_i^m replaces the original test vector T_i^m to be applied to the CUT at the *i-th* capture phase according to Conv-LBIST (Fig. 3). It will be shown that this enables a 50% AF reduction compared to Conv-LBIST.

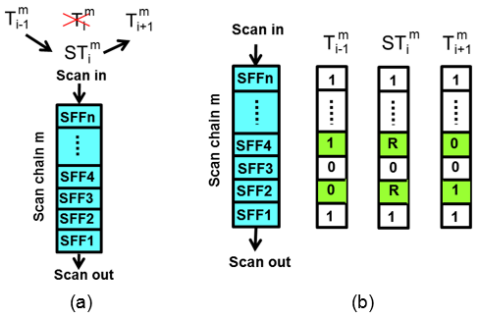

Fig. 3. Schematic representation of the: (a) sequence of test vectors filling each scan chain *m*; (b) bits in the ST vector ST_i^m, and in the test vectors applied/to be applied at the previous/following capture phase (T_{i-1}^m /T_{i+1}^m).

In our approach, the ST vector ST_i^m to be charged in the SC *m* and applied to the CUT at the *i-th* capture phase is constructed based on the structure of test vectors T_{i-1}^m and T_{i+1}^m to be applied at the *(i-1)-th* and *(i+1)-th* capture phases. Assuming the presence of a generic PS, our solution exploits the fact that, during the shift phase preceding the *i-th* capture phase, test vectors T_{i-1}^m and T_{i+1}^m are given at proper outputs of the PS. Should some test vectors be not produced at the PS outputs, the PS could be easily modified to generate them.

Denoting by $ST_i^m(j)$, $T_{i-1}^m(j)$ and $T_{i+1}^m(j)$ the logic value of the *j-th* bit in test vectors ST_i^m, T_{i-1}^m and T_{i+1}^m, respectively, $ST_i^m(j)$ is chosen as follows:

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j), & if\ T_{i-1}^m(j) = T_{i+1}^m(j) \\ R, & if\ T_{i-1}^m(j) \neq T_{i+1}^m(j) \end{cases},$$

where *R* denotes a random bit. Therefore, in all bit positions *j* in which test vectors T_{i-1}^m and T_{i+1}^m present the same logic value, ST_i^m maintains the same logic value as in the previous test

vector T_{i-1}^m. Instead, in the bit positions *j* in which test vectors T_{i-1}^m and T_{i+1}^m differ, ST_i^m assumes a random logic value *R*. The bit *R* can simply come from one of the outputs of the LFSR, as suggested in [8].

Starting from the *(i-1)-th* capture phase (Fig. 3), the new test vector sequence in each scan chain *m* will be as follows:

$$T_{i-1}^m - ST_i^m - T_{i+1}^m - ST_{i+2}^m - T_{i+3}^m \ \ldots$$

Therefore, the number of bits changing logic value between following test vectors with the new sequence T_{i-1}^m - ST_i^m - T_{i+1}^m will be equal to, or smaller than, those with the original test sequence T_{i-1}^m - T_i^m - T_{i+1}^m of Conv-LBIST.

In this regard, it is worth reminding that the considered scan-flip-flops (Fig. 2) update their outputs only at capture phases, while maintaining them constant during the shift phases. Therefore, the AF between successive test vectors will determine the AF of the CUT at each capture cycle.

The presence of a random bit *R* in ST_i^m in the bit positions where T_{i-1}^m and T_{i+1}^m differ allows the new sequence T_{i-1}^m - ST_i^m - T_{i+1}^m to preserve the randomness of the original sequence [8]. Therefore, as shown in Section V, the number of test vectors required to achieve a target FC does not increase compared to the application of the original test sequence.

The maximum AF between following test vectors loaded in each SC in Conv-LBIST (AF_{con}^{sc}) is reduced to a half ($AF_{con}^{sc}/2$) by our approach. Consequently, denoting by AF_{1ST}^{tot} the maximum AF between any two successive test vectors applied to the CUT at successive capture phases, for our approach with 1 ST vector, it is:

$$AF_{1ST}^{tot} = AF_{con}^{tot}/2,$$

where AF_{con}^{tot} is the max AF obtained with Conv-LBIST.

B. Approach with N Substitute Test Vectors

In order to reduce further the AF during capture phases of scan-based LBIST, a higher number *N* of ST vectors, ST_i^m, $ST_{i+1}^m \ldots ST_{i+N-1}^m$, with $ST_{i+1}^m = \cdots = ST_{i+N-1}^m = ST_i^m$, can be used to replace, for each scan chain *m*, *N* original test vectors T_i^m up to T_{i+N-1}^m.

Similarly to the case of 1 ST vector, the ST vectors $ST_i^m \ldots ST_{i+N-1}^m$ to be applied at the *i-th* ... *(i+N-1)-th* capture phases are constructed based on the test vector T_{i-1}^m to be applied at the *(i-1)-th* capture phase, and the test vector T_{i+N}^m to be applied at the *(i+N)-th* capture phase.

Denoting by $ST_i^m(j)$, $T_{i-1}^m(j)$ and $T_{i+N}^m(j)$ the logic value of the *j-th* bit in test vectors ST_i^m, T_{i-1}^m and T_{i+N}^m, respectively, $ST_i^m(j)$ is determined as follows:

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j), & if\ T_{i-1}^m(j) = T_{i+N}^m(j) \\ R, & if\ T_{i-1}^m(j) \neq T_{i+N}^m(j) \end{cases},$$

where, as before, *R* denotes a random bit.

The number of bits changing logic value between successive test vectors with the new sequence T_{i-1}^m - ST_i^m - … - ST_{i+N-1}^m – T_{i+N}^m (Fig. 4) will be equal to, or smaller than in the original test sequence T_{i-1}^m - T_i^m - … - T_{i+N-1}^m - T_{i+N}^m of Conv-LBIST. The presence of a random bit *R* in ST_i^m in the bit positions where T_{i-1}^m and T_{i+N}^m differ allows the new sequence T_{i-1}^m - ST_i^m - … - ST_{i+N-1}^m – T_{i+N}^m to preserve the randomness of the original sequence in these bit positions [8]. As a result, as shown in Section V, the number of test vectors required by our approach to achieve a target FC is approximately the same as that in Conv-LBIST, even for the case of N=10 ST vectors.

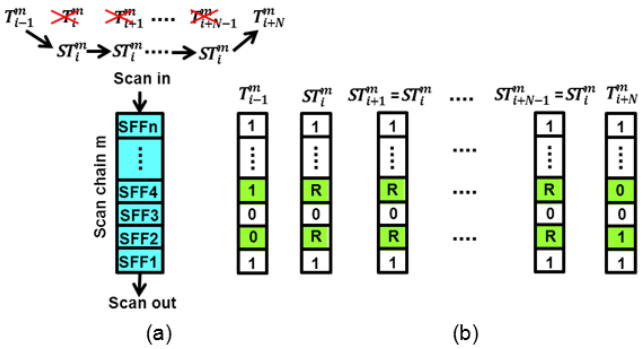

Fig. 4. Test vectors' selection of our approach with *N* ST vectors: (a) sequence of test vectors filling each scan chain; (b) ST vectors $ST_i^m \ldots ST_{i+N-1}^m$.

As represented in Fig. 5, we interleave the insertion of the *N* ST vectors, so that they are applied at different capture phases for the different SCs. Thus, between any two successive capture phases, the same ST vector is loaded in *(N-1)-out-of-(N+1)* scan chains, which consequently exhibit $AF^{sc} = 0$. Instead, *2-out-of-(N+1)* scan chains present a transition between an original test vector and a ST vector, thus presenting an $AF^{sc} = AF_{con}^{sc}/2$.

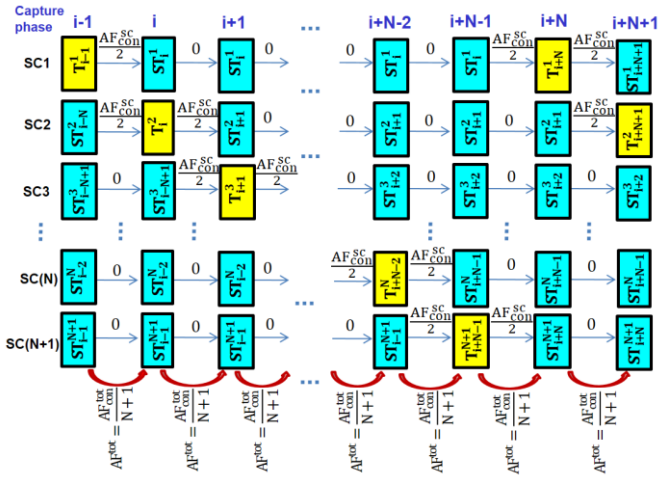

Fig. 5. Interleaved test vectors' application to the CUT and AF values for each capture phase, for the case with *N* ST vectors.

If the number of scan chains *s* is a multiple of *N+1*, the total AF between any two following test vectors is:

$$AF_{N\,ST}^{tot} = \sum_{m=1}^{s} AF^{sc\_m} = \frac{s}{N+1}\left(\frac{AF_{con}^{sc}}{2} + \frac{AF_{con}^{sc}}{2} + 0\right) = \frac{AF_{con}^{tot}}{N+1}, \quad (1)$$

where, as before, $AF_{con}^{tot} = sAF_{con}^{sc}$.

We have verified that, even if *s* is not a multiple of *N+1*, and *s>>N* (e.g., *s>10N*), that is if the number of SCs *s* is much higher than the number of ST vectors *N*, (1) gives a good

approximation of the $AF_{N\,ST}^{tot}$.

From (1) we can also derive that, with our approach, it is $AF^{tot} = AF_{con}^{tot}/3$ for *N=2*, $AF^{tot} = AF_{con}^{tot}/4$ for *N=3*, $AF^{tot} = AF_{con}^{tot}/5$ for *N=4*, and so on. As will be shown later, such reductions are achieved at no increase in the number of TVs needed to reach a target FC, and with a limited cost in terms of area overhead.

IV. Possible Implementation

To implement our approach, we assume the presence of a PS feeding the scan-chains of the CUT (Fig. 1). However, should a phase shifter not be present within the considered scheme, our approach can be implemented by adding an equivalent structure at the LFSR outputs.

A. Case of 1 Substitute Test Vector

Denoting by O^m ($m = 1..s$) the PS output feeding the scan chain *m*, the logic value $T_i^m(j)$ in the *j-th* position of the *i-th* test vector of the scan chain *m* is given by:

$$T_i^m(j) = O^m(\xi),$$

where $\xi = n(i-1)+j$ is the total number of shift CKs from the beginning of the test. This way, the logic values loaded in the *j-th* position of SC *m* in the shift phases before the *(i-1)-th*, the *i-th* and the *(i+1)-th* capture phases will be equal to the logic value present at the output O^m of the PS, after $\xi - n$, ξ, and $\xi + n$ shift CKs, respectively, counted from the beginning of the test. Thus, for each SC *m* and capture phase *i,* we can express the logic values present in the *j-th* position of the previous and the next test vectors ($T_{i-1}^m(j)$ and $T_{i+1}^m(j)$, respectively) as:

$$T_{i-1}^m(j) = O^m(\xi - n); \quad T_{i+1}^m(j) = O^m(\xi + n). \qquad (2)$$

Since the PS gives to its outputs many past/future values of each output O^m, we can determine the values of $O^m(\xi - n)$ and $O^m(\xi + n)$ from the current value present at two proper PS outputs. Therefore, there exist two PS outputs O^k and O^p, with $k \neq p \neq m$, such that:

$$O^m(\xi - n) = O^k(\xi); \quad O^m(\xi + n) = O^p(\xi). \qquad (3)$$

We exploit the relations in (2) and (3) to derive a low cost hardware implementation of our approach. As described in Section III.A, our approach forges the ST vector ST_i^m by comparing T_{i-1}^m and T_{i+1}^m. Thus, we can derive ST_i^m by simply comparing the outputs O^k and O^p of the PS at each shift CK *j*.

As an example, Fig. 6(a) shows a possible implementation of our proposed scheme, for the case in which the depth of the longest chain(s) is *n*. Our approach requires 2 multiplexers (M1 and M2) and an XOR gate for each scan chain *m*. M2 allows us to load in the scan chain *m* either: 1) the test vectors T_{i-1}^m and T_{i+1}^m generated by the PS during the shift phases before the *(i-1)-th* and *(i+1)-th* capture phases, by setting the selection signal *int1*=0; or 2) the ST vector ST_i^m provided by M1 during the shift phases before the *i-th* capture phase, by setting *int1*=1. Particularly, the signal *int1* is generated in such a way that it switches from 0 to 1 (and vice versa) at following capture phases. Fig. 6(b) depicts an example of *int1* generation, where FF1 and FF2 denote D flip-flops (FF). Initially, FF1 is set to 1 and FF2 is set to 0 (*int1* =0). Both FF1 and FF2 are clocked by the Scan Enable (SE) signal. Thus, at each SE rising edge, *int1* switches from 0 to 1 alternately.

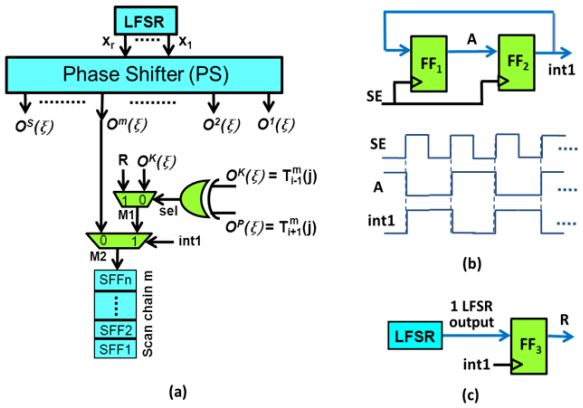

Fig. 6. Schematic representation of: (a) a possible implementation of our approach; (b) a possible scheme to generate signal *int1*; (c) a strategy to generate the random bit *R*.

The XOR gate compares the logic value at the PS output $O^k(\xi)$ (equal to $T_{i-1}^m(j)$) with the logic value at the PS output $O^p(\xi)$ (equal to $T_{i+1}^m(j)$) at each shift CK *j*. Thus, it is: *sel=0*, if $O^k(\xi) = O^p(\xi)$, indicating that $ST_i^m(j)$ should be equal to $O^k(\xi) = T_{i-1}^m(j)$; *sel=1*, if $O^k(\xi) \neq O^p(\xi)$, indicating that $ST_i^m(j)$ should be a random value *R*.

Finally, as described in [8], the bit *R* can be simply generated from any output of the LFSR. Since in our scheme we considered the same *R* value for the whole shift phase, we can simply generate *R* by sampling any output of the LFSR at the beginning of each shift phase. Fig. 6(c) shows a possible scheme to generate the bit *R*. One LFSR output feeds a FF (FF3), which is clocked by the *int1* signal. At each rising edge of *int1*, FF3 samples on *R* a new value present at the considered LFSR output, and it keeps it till the following *int1* rising edge. This way, the same *R* value is used during a whole shift phase. This strategy to generate *R* results in a highly unbalanced number of 0s or 1s in each ST vector, depending on whether *R* is 0 or 1. As also shown in [8], this feature increases the likelihood to detect hard to detect faults.

Let us illustrate, by means of a simple example, how our approach exploits the PS to generate the required test vectors, and signals $O^k(\xi)$ and $O^p(\xi)$ in the circuit in Fig. 6. We consider a 4 bit LFSR (with characteristic polynomial $p(x)=x^4+x+1$), and a PS with 4 inputs (the 4 LFSR outputs ($x_1(\xi)..x_4(\xi)$) and *s*=12 outputs ($O^1(\xi)..O^{12}(\xi)$) connected to 12 scan chains (providing $T_i^1(j)..T_i^{12}(j)$). For simplicity, we suppose that the longest scan chain is composed by *n=3* scan FFs, so that each shift phase requires 3 CK cycles.

The PS has been designed in order to provide, at every shift CK ξ: i) the current state of the LFSR (i.e., $x_1(\xi)..x_4(\xi)$) on $O^2(\xi)$, $O^5(\xi)$, $O^8(\xi)$, $O^{11}(\xi)$; ii) the state of the LFSR at 3 shift CKs before the current state (i.e., $x_1(\xi-3)..x_4(\xi-3)$) on $O^1(\xi)$, $O^4(\xi)$, $O^7(\xi)$, $O^{10}(\xi)$; iii) the state of the LFSR at 3 shift CKs after the current state of the LFSR (i.e., $x_1(\xi+3)..x_4(\xi+$

3)) on $O^3(\xi)$, $O^6(\xi)$, $O^9(\xi)$, $O^{12}(\xi)$.

The logic operations performed by the PS to compute $O^1(\xi)..O^{12}(\xi)$ as a function of the current state of the LFSR $(x_1(\xi)..x_4(\xi))$ are reported in the second column of Table I. As can be seen, all $O^m(\xi)$ signals are expressed as linear combinations of the present state of the LFSR, and can be computed by simple XOR trees.

TABLE I. PS PERFORMED FUNCTION AND GENERATED OUTPUTS.

$O^m(\xi) = T^m_i(j)$	PS Function	$O^m(\xi-3) = T^m_{i-1}(j) = O^k(\xi)$	$O^m(\xi+3) = T^m_{i+1}(j) = O^p(\xi)$
$O^1(\xi)$	$X_4(\xi)$	$O^{10}(\xi)$	$O^2(\xi)$
$O^2(\xi)$	$X_1(\xi)$	$O^1(\xi)$	$O^3(\xi)$
$O^3(\xi)$	$X_1(\xi)\oplus X_2(\xi)\oplus X_3(\xi)\oplus X_4(\xi)$	$O^2(\xi)$	$O^3(\xi)\oplus O^6(\xi)$
$O^4(\xi)$	$X_1(\xi)\oplus X_2(\xi)$	$O^4(\xi)\oplus O^{11}(\xi)$	$O^5(\xi)$
$O^5(\xi)$	$X_2(\xi)$	$O^4(\xi)$	$O^6(\xi)$
$O^6(\xi)$	$X_1(\xi)\oplus X_3(\xi)\oplus X_4(\xi)$	$O^5(\xi)$	$O^3(\xi)\oplus O^9(\xi)$
$O^7(\xi)$	$X_2(\xi)\oplus X_3(\xi)$	$O^4(\xi)\oplus O^7(\xi)$	$O^8(\xi)$
$O^8(\xi)$	$X_3(\xi)$	$O^7(\xi)$	$O^9(\xi)$
$O^9(\xi)$	$X_1(\xi)\oplus X_4(\xi)$	$O^8(\xi)$	$O^3(\xi)\oplus O^2(\xi)$
$O^{10}(\xi)$	$X_3(\xi)\oplus X_4(\xi)$	$O^7(\xi)\oplus O^{10}(\xi)$	$O^{11}(\xi)$
$O^{11}(\xi)$	$X_4(\xi)$	$O^{10}(\xi)$	$O^{12}(\xi)$
$O^{12}(\xi)$	$X_1(\xi)$	$O^{11}(\xi)$	$O^3(\xi)$

Our approach needs to identify $T^m_{i-1}(j)$ and $T^m_{i+1}(j)$ for each scan chain m (m=*1..12*) and at each shift CK j. Since it is n=3, to identify $T^m_{i-1}(j)$ we need to determine the value shifted-in the scan chain m at 3 previous shift CKs (i.e., $O^m(\xi-3) = O^k(\xi)$), while to identify $T^m_{i+1}(j)$ we need to determine the value shifted-in the scan chain m at 3 following shift CKs (i.e., $O^m(\xi+3) = O^p(\xi)$). The third and fourth columns of Table I report the PS outputs, or output combinations, giving $O^m(\xi-3) = O^k(\xi)$ and $O^m(\xi+3) = O^p(\xi)$, for each $O^m(\xi)$. From Table I, we can observe that the past/future values of $O^m(\xi)$ (i.e., $O^k(\xi)$ / $O^p(\xi)$), for m = 1, 2, 5, 8, 11 and 12, are equal to the values assumed by other outputs of the PS at the current shift CK ξ. Instead, for m = 3, 4, 6, 7, 9 and 10, the past/future values of $O^m(\xi)$ are not directly present on other outputs of the PS. However, as shown in Table I, they can be obtained as a linear combination of the current PS outputs. This mandates an extra area overhead (due to the required extra XORs), which is however negligible in realistic designs with a large number of PS outputs.

B. *Case of N Substitute Test Vectors*

In our scheme with N ST vectors, N original test vectors $T^m_i \ldots T^m_{i+N-1}$ are replaced by N identical ST vectors ($ST^m_i = \cdots = ST^m_{i+N-1}$) in each scan chain m. Therefore, on the SC m, we first load ST^m_i to be applied at the *i-th* capture phase, which is constructed based on T^m_{i-1} and T^m_{i+N}. Then, we load ST^m_{i+1} to be applied at the *(i+1)-th* capture phase, which is constructed based on $T^m_{(i+1)-2}$ and $T^m_{(i+1)+N-1}$. We proceed this way till the *(i+N-1)-th* capture phase.

Similarly to the case with 1 ST, to generate a ST vector at each *i-th* ... *(i+N-1)-th* capture phase between $T^m_{i-1}(j)$ and $T^m_{i+N}(j)$, we relate the values of the previous test vectors $T^m_{i-1} \ldots T^m_{(i+N-2)}$ and their respective future $T^m_{i+N} \ldots T^m_{i+1}$ to the values of the PS output O^m (at present *i-th* ... *(i+N-1)-th* shift phase) as follows: the previous test vectors can be determined as $T^m_{i-1}(j) = O^m(\xi-n) \ldots T^m_{(i+N-2)}(j) = O^m(\xi-\mathrm{N}n)$, while the future test vectors can be determined as $T^m_{i+\mathrm{N}}(j) = O^m(\xi+\mathrm{N}n) \ldots T^m_{(i+1)}(j) = \mathrm{O}^m(\xi+n)$. During each shift CK j, we can determine the logic value at $O^m(\xi-n)$ and $O^m(\xi+\mathrm{N}n) \ldots O^m(\xi-\mathrm{N}n)$ and $O^m(\xi+n)$ by using proper PS outputs. Should such outputs be not available, they can be generated by properly modifying the PS.

Fig. 7 shows a possible implementation of our scheme with N ST vectors. For each SC m, it requires two 2-input multiplexers (M1 and M2), two N-input multiplexers (M3 and M4) and an XOR gate.

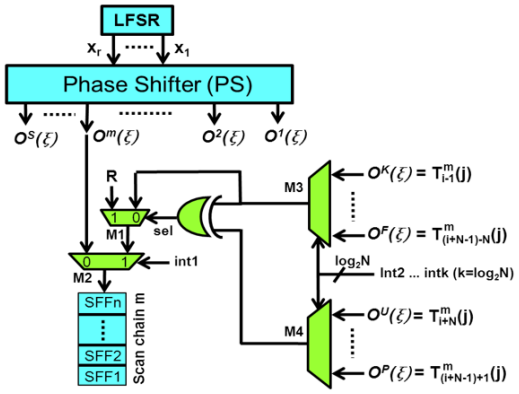

Fig. 7. Schematic representation of a possible implementation of our approach with N ST vectors.

The multiplexer M2 allows us to load on the scan chain m:

1) The original test vectors T^m_{i-1} and T^m_{i+N} generated by the PS, by setting *int1*=0, during the shift phases before the *(i-1)-th* and *(i+N)-th* capture phases;
2) The ST vectors $ST^m_i \ldots ST^m_{i+N-1}$ provided by multiplexer M1, by setting *int1*=1, during the shift phases before the *i-th* … *(i+N-1)-th* capture phases.

Instead, M3 and M4 enable the selection of XOR inputs. These are the PS outputs required to construct the ST vectors $ST^m_i \ldots ST^m_{i+N-1}$ to be applied at the *i-th* … *(i+N-1)-th* capture phases. As an example, in Fig. 7, M3 and M4 select as inputs for the XOR: $O^k(\xi)$ (generating $T^m_{i-1}(j)$), $O^u(\xi)$ (generating $T^m_{i+N}(j)$) … $O^f(\xi)$ (generating $T^m_{(i+N-1)-N}(j)$), $O^p(\xi)$ (generating $T^m_{(i+N-1)+1}(j)$). This way, at each shift CK j of the shift phase prior to the *i-th* … *(i+N-1)-th* capture phase, the XOR compares $O^k(\xi) = T^m_{i-1}(j)$ with $O^u(\xi) = T^m_{i+N}(j)$, ... $O^f(\xi) = T^m_{(i+N-1)-N}(j)$ with $O^p(\xi) = T^m_{(i+N-1)+1}(j)$. If the inputs of the XOR are equal, the XOR outputs *sel=0*, indicating that the logic value of bit $ST^m_i(j) \ldots ST^m_{i+N-1}(j)$ should be equal to $T^m_{i-1}(j) \ldots T^m_{(i+N-1)-N}(j)$). Instead, if the inputs of the XOR differ, it is *sel = 1*, indicating that the logic value of $ST^m_i(j) \ldots ST^m_{i+N-1}(j)$ should be a random value *R*.

As for the control signals *int1, int2,…, intk*, with *k= log2(N)*, they can be generated by expanding the shift register shown in Fig. 6(b) for the case of 1 ST vectors, to a shift register with *log2(N)+1* FFs. Finally, the random bit *R* can be generated by the same scheme as for the case with 1 ST vector (Fig. 6(c)).

V. Comparison

We compare our approach with Conv-LBIST [12] and the solutions in [9, 21]. We consider the PD reduction and the number of test vectors required to achieve a target FC as metrics for comparison. We consider the FC for stuck-at faults as in [9], and we evaluate the area overhead required by our approach over Conv-LBIST. Our approach has been validated logic level simulations, as the alternative solutions in [9, 21] that we consider for comparison purposes.

A. Comparison with Conv-Scan-Based LBIST

As for the effectiveness in reducing PD during scan-based LBIST, we have evaluated the maximum AF between any two following test vectors (to be applied at following capture phases), which is proportional to the CUT AF, thus also to its PD. Our approach has been implemented with up to 10 ST vectors. For each CUT, we have considered the maximum stuck-at FC achievable with Conv-LBIST as target stuck-at FC. The number of test vectors required to achieve such a FC has been evaluated by means of the Synopsys TetraMAX tool. Finally, the area overhead (AO) required by our approach over Conv-LBIST has been evaluated by the Synopsys Design Compiler tool. It should be noted that our approach requires no hardware modification of the considered scan flip-flops.

For comparison purposes, our approach has been applied to the largest four ISCAS'89 benchmarks considered in [9] (s38584, s38417, s13207 and s15850). For all circuits, we have used a 20-bit LFSR, with characteristic polynomial $p(x)=x^{20}+x^{17}+1$ [25]. As for the PS, it has been implemented in order to minimize area overhead, according to the rules in [10].

Figs. 8(a)-(d) show, for the four considered benchmarks, the AF of Conv-LBIST, as well as the AF and AO of our approach, as a function of the number of ST vectors. We can see that, for all benchmarks, our approach allows us to reduce noticeably the AF, thus also PD, with respect to Conv-LBIST. In this regard, it is worth noticing that the AF achieved by our solution reduces quickly as the number of ST increases for small number of ST vectors (i.e., from 1 ST to 5 ST), while it tends to saturate for more than 6 ST vectors. Particularly, with respect to the AF of Conv-LBIST, the AF achievable by our approach becomes approximately the 50% with 1 ST vector, the 33% with 2 ST vectors, the 25% with 3 ST vectors, and the 9% with 10 ST vectors.

Figs. 8(a)-(d) also report the relative AF reduction allowed by our approach over Conv-LBIST ($\Delta\mathbf{AF} = 100*(\mathbf{AF}_{OUR} - \mathbf{AF}_{\text{Conv-LBIST}}) / \mathbf{AF}_{Conv\text{-}LBIST}$) as a function of the number of ST vectors. We can observe that, for a number of ST vectors higher than 4, our approach enables an AF reduction higher than 80%. Moreover, we can note that, for all benchmarks, the AO of our approach over Conv-LBIST increases linearly with the number of ST vectors. A minimum of approximately 1.5% AO is achieved with 1 ST for s38584 benchmark, and a maximum of approximately 14% AO is reached with 10 ST vectors for the s13207 benchmark.

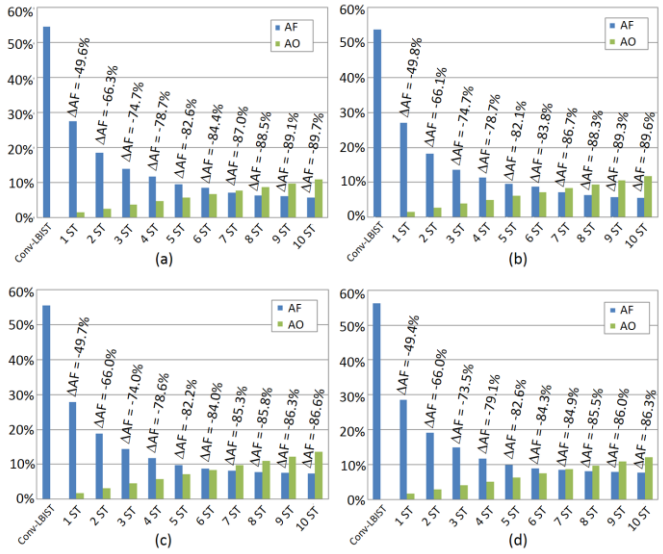

Fig. 8. Simulation results showing the AF of Conv-LBIST, as well as the AF and AO of our approach with up to 10 ST vectors for the considered benchmark circuits: (a) s38584; (b) s38417; (c) s13207; (d) s15850.

TABLE II
NUMBER OF TEST VECTORS (#TV) REQUIRED BY CONV-LBIST AND BY OUR SOLUTION TO ACHIEVE A TARGET FC.

Benchmark			*s38584*	*s38417*	*s13207*	*s15850*
# SCs			*59*	*67*	*28*	*25*
Target FC			*95.89%*	*95.53%*	*98.33%*	*94.00%*
Conv-LBIST	**#TV**		***32800***	***39104***	***30464***	***38112***
Our solution	1 ST	**#TV**	***32660***	***38667***	***30436***	***37217***
		Δ#TV	*-0.43%*	*-1.12%*	*-0.09%*	*-2.35%*
	2 ST	**#TV**	***32657***	***38587***	***30514***	***37357***
		Δ#TV	*-0.44%*	*-1.32%*	*0.16%*	*-1.98%*
	3 ST	**#TV**	***32660***	***38448***	***30601***	***37213***
		Δ#TV	*-0.43%*	*-1.68%*	*0.45%*	*-2.36%*
	4 ST	**#TV**	***32759***	***38627***	***30588***	***37486***
		Δ#TV	*-0.12%*	*-1.22%*	*0.41%*	*-1.64%*
	5 ST	**#TV**	***32790***	***38751***	***30607***	***37580***
		Δ#TV	*-0.03%*	*-0.90%*	*0.47%*	*-1.40%*
	6 ST	**#TV**	***32869***	***38699***	***30859***	***37604***
		Δ#TV	*0.21%*	*-1.04%*	*1.30%*	*-1.33%*
	7 ST	**#TV**	***32934***	***38755***	***30891***	***37616***
		Δ#TV	*0.41%*	*-0.89%*	*1.40%*	*-1.30%*
	8 ST	**#TV**	***32962***	***38872***	***30955***	***37838***
		Δ#TV	*0.49%*	*-0.59%*	*1.61%*	*-0.72%*
	9 ST	**#TV**	***32989***	***38904***	***31019***	***37854***
		Δ#TV	*0.58%*	*-0.51%*	*1.82%*	*-0.68%*
	10 ST	**#TV**	***32996***	***38917***	***31158***	***37866***
		Δ#TV	*0.60%*	*-0.48%*	*2.28%*	*-0.64%*

Table II reports, for each benchmark, the number of test vectors (#TV) required by Conv-LBIST and by our solution to achieve the target FC. It also reports the relative variation in the #TV required by our approach over Conv-LBIST ($\Delta\mathbf{\#TV} = 100*(\mathbf{\#TV}_{OUR} - \mathbf{\#TV}_{\text{Conv-LBIST}}) / \mathbf{\#TV}_{Conv\text{-}LBIST}$).

We can observe that, for all benchmarks, the #TV required by our solution with up to 10 ST vectors is very similar to that of the Conv-LBIST for the same FC. Therefore, our solution allows us to reduce considerably the AF (thus PD) compared to Conv-LBIST, with no increase in the number of test vectors (thus TT) required to achieve a target FC and with limited increase in area overhead.

B. Comparison to Alternative Solutions

We compare our solution with the alternative techniques in [9, 21]. For all solutions, we have evaluated: 1) the AF between following test vectors (which, as clarified before, determines the CUT AF, thus the PD, at each capture phase); 2) the number of test vectors (#TV) required to achieve the stuck-at FC reported in [9], here assumed as target FC for comparison purposes. They have been evaluated for the four benchmarks considered in the previous subsection. These are the benchmarks considered also in [9], to which we have also applied the approach in [21] for comparison purposes. It should be noted that the benchmarks in [21] have not been considered, since they are not available in the open literature.

The solution in [9] is implemented considering the scan-chains divided in groups of $n=2$ scan-chains [9], which enables 50% AF reduction with respect to Conv-LBIST, thus allowing us to achieve an AF similar to that obtained with our approach with 1 ST vector.

As for the solution in [21], we have implemented it considering the case of an AF reduction of 50% with respect to Conv-LBIST (i.e., a value of WTM = 25% in [21]), which is similar to that obtained with our approach with 1 ST vector.

The comparison results are reported in Tab. III. The AF and #TV relative variations are calculated as: $\Delta = 100*(OUR - [9,21])/[9,21]$. From Table III we can observe that the approaches in [9, 21] require a significantly higher number of test vectors (more than twice in most cases), than that required by our solution to achieve the same target FC. Additionally, our solution allows us to achieve a lower maximum AF.

TABLE III.
NUMBER OF TEST VECTORS (#TV) TO ACHIEVE A TARGET FC, AND MAXIMUM AF FOR OUR APPROACH WITH 1 ST VECTOR AND FOR THE SOLUTIONS IN [9, 21].

		s13207	s15850	s38417	s38584
Target FC (%) [9]		96.8	91.71	95.37	95.24
Solution in [9] with n=2	#TV	**54500**	**29500**	**80500**	**49000**
	AF (%)	30.7	31.9	27.9	28.9
Solution in [21] (WTM=25%)	#TV	**33618**	**31835**	**43449**	**37594**
	AF (%)	30.5	31.9	31.2	31.1
Our solution with 1 ST	#TV	**14006**	**2514**	**21534**	**18496**
	Δ#TV [9] (%)	**-74**	**-91**	**-73**	**-62**
	Δ#TV [21] (%)	**-58.9**	**-92.1**	**-50.4**	**-50.8**
	AF (%)	27.9	28.5	27.0	27.5
	ΔAF [9] (%)	-9.3	-10.8	-3.4	-4.7
	ΔAF [21] (%)	-8.5	-10.7	-13.5	-11.6

VI. CONCLUSIONS

We have presented a novel approach to reduce PD during at-speed test of sequential circuits with scan-based Logic BIST using the Launch-On-Capture scheme. The proposed solution enables designers to reduce the probability that the delay induced by PD exhibited during at-speed test is erroneously interpret as a delay fault, with consequent generation of a false test fail. This is achieved by reducing the activity factor of the CUT compared to conventional scan-based LBIST, by proper modification of the test vectors generated by the LFSR.

We have shown that, compared to conventional scan-based LBIST, our approach allows us to achieve a scalable PD reduction (ranging from the 50% to the 89%), with no drawback on the required number of test vectors to achieve a target FC and with limited costs in terms of area overhead (ranging from the 1.5% to the 14%). We have also shown that, compared to the solutions in [9, 21], our solution allows us to reduce significantly (more than 50%) the number of test vectors (thus test time) to achieve the same target FC.

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