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Talebzadeh, J. and Kale, I.

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Design of a Delayless Feedback Path Free 2nd-order Two-Path Time-Interleaved Discrete-Time Delta-Sigma Modulator- a New Approach

Jafar Talebzadeh and Izzet Kale
Applied DSP & VLSI Research Group
Department of Engineering
University of Westminster London, W1W 6UW, UK
Emails: Jtalebzadeh@gmail.com & kalei@westminster.ac.uk

***Abstract*—this paper presents the design procedure for a 2nd_order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator from a conventional single-loop 2nd-order Discrete-Time (DT) ΔΣ modulator through the use of time domain equations and time-interleaving concepts [1]. The resulting modulator is free from the delayless feedback path and has only one set of integrators. The delayless feedback path issue in Time-Interleaved (TI) ΔΣ modulators is a critical restriction for the implementation of TI ΔΣ modulators and is effectively eliminated through the use of the approach proposed in this paper. The DTTI ΔΣ modulator requires only three op-amps and two quantizers both of which work concurrently, in comparison to the single-loop DT counterpart that also deploys two op-amps. For an OverSampling Ratio (OSR) of 16 and a clock frequency of 640MHz, our simulation results show a maximum Signal-to-Noise Ratio (SNR) for the DTTI ΔΣ modulator to be 70.5dB with an input bandwidth of 20MHz which has 15dB improvement in comparison to its single-loop, single-path DT counterpart.**

Keywords*— *Time-Interleaved, ΔΣ modulator, Signal-to-Noise Ratio.

I. INTRODUCTION

Recent trends in the portable communication industry demand both high resolution and low power Analog-to-Digital Converters (ADCs). These requirements can be met by utilizing ΔΣ modulators which perform analog-to-digital conversion for relatively low bandwidth signals. Both the OSR and the technology restrict the deployable signal bandwidth of ΔΣ modulators.

Recently wideband applications require the ADCs with larger signal bandwidth. In order to increase the signal bandwidth the modulator can deal with, a variety of methods can be used such as: using higher sampling frequency, increasing the order of the modulator and the number of quantizer bits. However, each of them has a price and is restricted by technology deployed. Using above mentioned methods to increase OSR make the design of the modulator more complicated and may cause stability problem which require to be dealt with carefully.

One efficient and attractive way to increase the OSR, is to consider the time-interleaving approach through which parallelism can be incorporated in ADCs in order to increase the effective sampling rate [1]-[8]. This approach is a practical solution that does not necessitate state of art technologies.

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However, using straightforward time-interleaving technique for ΔΣ modulators results in a bit improvement in SNR performance of the whole modulator. As shown in [1] and [2], the time-interleaving can be successfully applied to ΔΣ modulators. A TI ΔΣ modulator deploys M identical cross-coupled modulators working concurrently and each running at a sampling rate of F_s. The effective sampling rate is the same as a single-loop ΔΣ modulator which operates at a sampling frequency of MF_s.

One set of integrators is shared between two paths in order to save power dissipation, silicon area and to eliminate the instability arising from DC offset mismatch between indivisual integrator sets.

This paper is organized as follows. In section II, a 2nd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator is derived from a 2nd-order conventional DT ΔΣ modulator by deploying the time domain equations. In section III, the delayless feedback path problem is discussed and our proposed solution is presented in detail in this section. In section IV, MATLAB simulation results are presented. Finally, conclusions are given in section V.

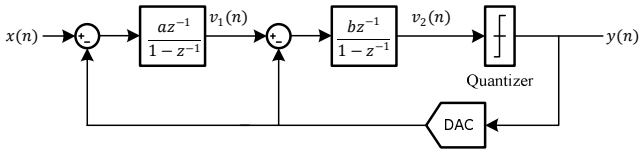

Figure 1: A 2nd-order conventional single-loop DT ΔΣ modulator.

II. DERIVATION OF TIME-INTERLEAVED ΔΣ MODULATOR

In order to derive a 2nd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator, the time-interleaving concept and the time domain equations of its conventional single-loop 2nd-order DT ΔΣ modulator counterpart as shown in Figure 1, are used [1]. The feedback loop of the DAC is assumed ideal and has unity transfer function ($H_{DAC}(z) = 1$). The time-domain equations defining the conventional single-loop 2nd-order DT ΔΣ modulator can be cast in the following way:

$$v_1(2n) = ax(n) \; - ay(n) + v_1(n-1) \quad (1)$$

$$v_2(2n) = bv_1(n) - by(n) + v_2(n-1) \quad (2)$$

$$y(n) \; = Q[v_2(n)] \quad (3)$$

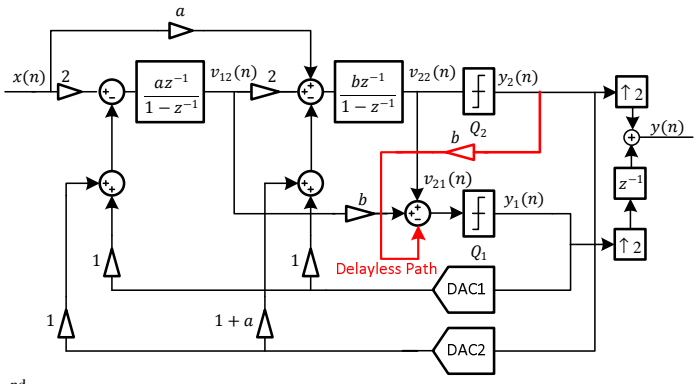

Figure 2: A two-path 2nd-order DTTI ΔΣ modulator with shared integrators and delayless feedback path highlighted.

Where $Q[.]$ represents the quantization function.

In order to derive the DTTI ΔΣ modulator, the time domain equations of the single-loop 2nd –order DT ΔΣ modulator are written for two consecutive time slots and are as (2n)th and (2n+1)th.

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (4)$$
$$v_2(2n) = bx(2n-1) - by(2n-1) + v_2(2n-1) \quad (5)$$
$$y(2n) = Q[v_2(2n)] \quad (6)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (7)$$
$$v_2(2n+1) = bx(2n) - by(2n) + v_2(2n) \quad (8)$$
$$y(2n+1) = Q[v_2(2n+1)] \quad (9)$$

A fast demultiplexer is used to distribute the input signal $x(n)$ between the two paths/channels. The demultiplexer operates at twice the clock frequency of each channel [1]. The input $x(n)$ is relabeled as follows:

$$x_1(n) = x(2n), \; x_2(n) = x(2n-1) \quad (10)$$

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n), \quad v_{12}(n) = v_1(2n-1) \quad (11)$$
$$v_{21}(n) = v_2(2n), \quad v_{22}(n) = v_2(2n-1) \quad (12)$$
$$y_1(n) = y(2n), \quad y_2(n) = y(2n-1) \quad (13)$$

To save power consumption and silicon area the input demultiplexer is removed and the input signal $x(n)$ is shared between two channels. Therefore equation (10) results in (14) as follows:

$$x_1(n) = x_2(n) = x(n) \quad (14)$$

The resulting equations are written as equations (15), (16), (17), (18) and (19) and the DTTI ΔΣ modulator shown in Figure 2 is derived directly from these equations [1]:

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \quad (15)$$
$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (16)$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \quad (17)$$
$$y_1(n) = Q[v_{21}(n)] \quad (18)$$
$$y_2(n) = Q[v_{22}(n)] \quad (19)$$

The dc offset mismatch of the two individual integrators set between channels in the DTTI ΔΣ modulator can cause instability which can be eliminated by sharing one set of integrators between the two channels [2]. A fast input demultiplexer which is a limiting factor for the performance of the DTTI ΔΣ modulators is necessary. However this input demultiplexer can be removed and the input signal simply shared between the two channels [5][6][10]. The Signal Transfer Function (STF) of the DTTI ΔΣ modulator exhibits some notches in its response at the following frequencies $0.5F_{clk}$, $1.5F_{clk}$, $2.5F_{clk}$, $3.5F_{clk}$, ... where F_{clk} is the clock frequency of the DTTI ΔΣ modulator resulting from the removal of the input demultiplexer. This modification and has no effect on the modulator's Noise Transfer Function (NTF) [5][6][10].

III. DELAYLESS FEEDBACK PATH ISSUE

The "delayless feedback path" problem makes the implementation of multi-path TI ΔΣ modulator impractical [4]. We have developed a new approach to circumvent this problem effectively with reduced complexity and the focus of this paper is on this approach. The root of the problem stems from equation (17) where $v_{21}(n)$ (the input of the quantizer Q1) is coupled directly to $y_2(n)$, dictating that the second quantizer (Q2) output has to connect to the input of quantizer (Q1) without any delay! We propose an approach based on an error correction technique to circumvent/eliminate this delayless feedback path. This is achieved by intentionally inducing an analog domain error by using the output of DAC2 as shown in Figure 3. The error is subsequently corrected to a great extent in the digital domain thereby circumventing/eliminating the delayless feedback path. A step by step mathematical analysis of the approach is exposed in the following lines to aid understanding. Furthermore a detailed event sequence diagram with the associated DAC outputs and the delay from the outputs of quantizers Q1 and Q2 that propagates through to the outputs of DAC1 and DAC2 as δ are shown in Figure 4. As a direct consequence it is clearly seen that the DAC2 output which is sampled at the nth time slot is

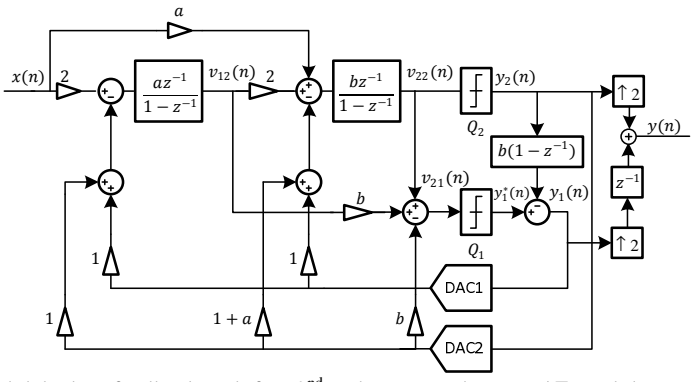

Figure 3: The proposed delayless feedback path free 2nd-order two-path DTTI ΔΣ modulator with shared integrators.

$y_2(n-1)$. However theory and the equations require that we should have $y_2(n)$. We can creatively overcome this problem by looking at the input and output of Q1, as depicted in Figure 2. The signal $v_{21}(n)$ is quantized through Q1 as follows:

$$y_1(n) = Q[v_{21}(n)] \tag{20}$$

By substituting (17) into (20) we arrive at equation (21):

$$y_1(n) = Q[bv_{12}(n) - by_2(n) + v_{22}(n)] \tag{21}$$

Equation (21) is rewritten by using the output of DAC2 in (22):

$$y_1(n) = Q[cv_{12}(n) - by_2(n-1) + v_{22}(n)] + by_2(n-1) - by_2(n) \tag{22}$$

We label the output of Q1 as $y_1^*(n)$ in (23):

$$y_1(n) = y_1^*(n) + by_2(n-1) - by_2(n) \tag{23}$$
$$error = b\Delta y = b(y_2(n) - y_2(n-1)) \tag{24}$$
$$Y_1(z) = Y_1^*(z) - b(1-z^{-1})Y_2(z) \tag{25}$$

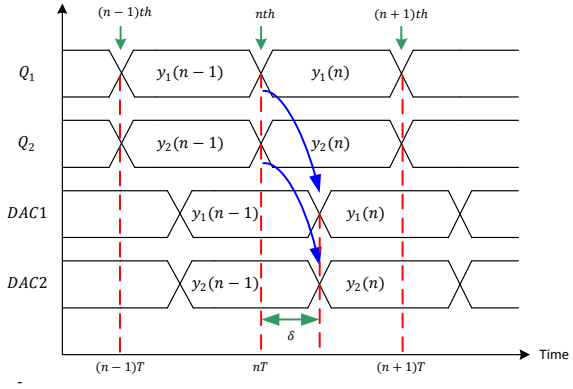

Figure 4: Sequence of events for the outputs of the quantizers and DACs for the DTTI.

Equation (23) illustrates $y_1^*(n)$ (the output of Q1) which contains the error depicted in equation (24) and as mentioned earlier needs to be corrected before applying it to the input of DAC1. The correction is performed in the digital domain by a first order differencer block $(1-z^{-1})$ as stipulated in (25). The first order differencer block only corrects the error in equation (23). It has no effect on targets and the signal or the quantization noise of our proposed 2nd-order two-path DTTI ΔΣ modulator which has shared integrators as shown in Figure 3. If the simple correction approach proposed above is not utilised the uncorrected error causes instability changing the modulator dynamics and increasing its order.

IV. SIMULATION RESULTS

A conventional single-loop 2nd-order single-path DT ΔΣ modulator with an OSR of 8 has been designed to operate with a clock frequency of 320MHz and a signal bandwidth of 20MHz and was modelled and simulated using SIMULINK. The modulator coefficients were chosen through the use of the sigma-delta toolbox [11] to be $a = 0.5$ and $b = 2.0$. The resulting 2nd-order two-path DTTI ΔΣ modulator has the same coefficients as the DT single-path, single-loop ΔΣ modulator as illustrated in Figure 3 with an OSR of 16 which operates from a clock frequency of 640MHz with a signal bandwidth of 20MHz. The single-loop, single-path 2nd order DT ΔΣ modulator DAC requires 4 bit resolution and as a consequence 15 comparators are chosen. The quantizer Q2 in DTTI ΔΣ modulator has 15 levels; however, the quantizer Q1 needs to have 31 levels due to the increase in the signal swing at the input of this quantizer. Therefore it will not lead to any SNR loss. After correcting the error as dictated by equation (13) in the digital domain, $y_1(n)$ will also need to be 4 bits in length.

The STF and NTF of the single-loop, single-path DT ΔΣ modulator of Figure 1 can be formulated as follows:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{26}$$
$$STF(z) = z^{-2} \tag{27}$$
$$NTF(z) = (1-z^{-1})^2 \tag{28}$$

Where $X(z)$ and $E(z)$ represents the z-transform of the input signal and quantization noise of the quantizer respectively. The STF and NTFs of the DTTI ΔΣ modulator of Figure 3 can be derived and formulated as follows:

$$Y(z) = Y_1(z^2)z^{-1} + Y_2(z^2) \tag{29}$$
$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \tag{30}$$

$$STF(z) = z^{-2}(1 + z^{-1}) \quad (31)$$
$$NTF_1(z) = z^{-1}(1 - z^{-1})^2 \quad (32)$$
$$NTF_2(z) = (1 - z^{-1})^2 \quad (33)$$

Where $STF(z), NTF_1(z)$ and $NTF_2(z)$ represent the signal transfer function from $x(t)$ to $y(n)$, the noise transfer function from $e_1(n)$ (quantization noise of Q1) to $y(n)$ and the noise transfer function from $e_2(n)$ (quantization noise of Q2) to $y(n)$ respectively. The terms in z^2 in (21) show the effect of the up-samplers in the modulator. The term in $(1 + z^{-1})$ from the $STF(z)$ of the DTTI ΔΣ modulator shows the effect of removing the input demultiplexer of the DTTI ΔΣ modulator causing some notches in the STF as explained earlier on in the paper and as described in [5][6][10]. Figure 5 shows the NTFs of the DT and the DTTI ΔΣ modulator. As can be seen, NTF of the DTTI ΔΣ modulator shape the quantization noise more than the NTF of the DT ΔΣ modulator.

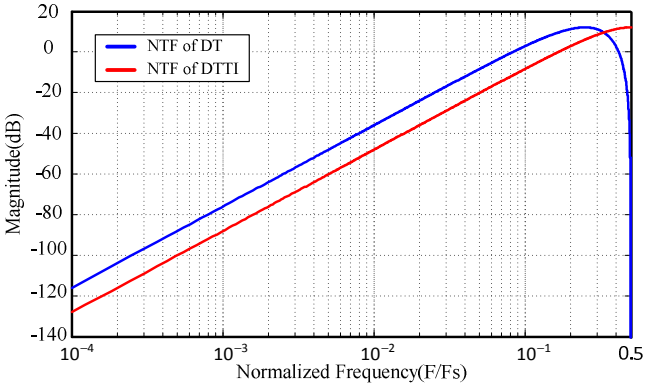

Figure 5: The NTFs of the DT and the DTTI ΔΣ modulator.

Figure 6 shows the comparison of the output spectra of the single-loop, single-path DT and the two-path DTTI ΔΣ modulators. As can be seen the two-path DTTI ΔΣ modulator output spectrum has more in-band noise shaping than its single-loop, single-path DT counterpart. The SNRs of the DT and the DTTI ΔΣ modulators for a single tone (sine) input signal having a frequency of 4.892MHz and an amplitude of -2dBFS with clock frequencies of 320MHz and 640MHz are 55.5dB and 70.5dB respectively. Therefore in this particular case, the SNR of the DTTI ΔΣ modulator shows a 15dB improvement in comparison to the DT one alone.

V. CONCLUSION

The design of a 2nd-order single-loop two-path DTTI ΔΣ modulator free from the delayless feedback path problem that can be extended to any-order multi-path DTTI ΔΣ modulator has been shown in this paper. The simulation results illustrate that the resulting DTTI ΔΣ modulator having an OSR of 16 and a clock frequency of 640MHz with a 20MHz signal bandwidth attains a maximum SNR of 70.5dB. This result suggests that the SNR is improved by 15dB in comparison to the maximum SNR of the conventional single-loop 2nd-order single-path DT ΔΣ modulator.

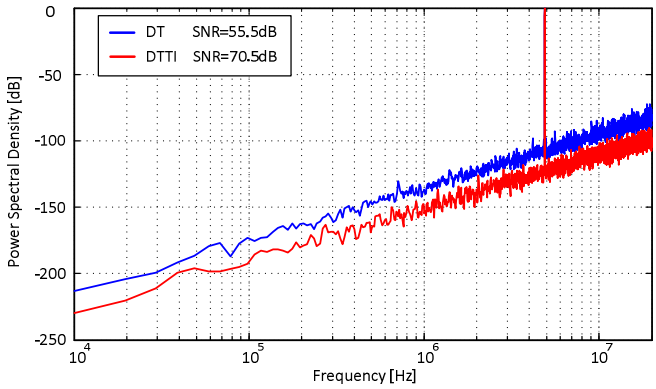

Figure 6: The output spectra of the conventional DT and the DTTI ΔΣ modulator for a 4.892MHz input sine signal with clock frequencies of 320MHz and 640MHz respectively.

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