Exploiting the bulk-driven approach in CMOS analogue amplifier design

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EXPLOITING THE BULK-DRIVEN APPROACH IN CMOS ANALOGUE AMPLIFIER DESIGN

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Declaration

I hereby declare that this thesis has been completed by myself and that the research documented is carried out entirely on my own. Where other sources of information have been used, they have been quoted. I have acknowledged all main sources of help.

No part of this thesis has been submitted in support of an application for any other degree.

Yasutaka Haga

To Hiromi

For her understandings, love and support

Acknowledgements

I am forever indebted to my advisor Professor Izzet Kale for his great guidance and support throughout the course of my PhD studies. He is the one who introduced me the bulk-driven approach when I was confused with what to work for in my MSc project. After achieving the MSc degree I was inspired to extend the study in my PhD research, however as I moved on I completely got stuck due to too many problems this design approach is having, and eventually I almost gave up the PhD because I thought that I chose the wrong subject. But Izzet was calm when I told him this feeling. He kept on advising my works and encouraging me. This thesis would not have been possible without him.

I am also grateful to my second advisor Professor Richard C. S. Morling and my research colleagues, Dr. Hashem Zare-Hoseini, Dr. Ediz Cetin, and Dr. Alper Ucar, for peer reviewing the conference papers which I published with Izzet. Their deep insights and suggestions certainly enabled me to further improve the works.

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My final and most heartfelt acknowledgement goes to my wife Hiromi. A new novel circuit block called the BDFVF (reported in Chapter 4 of this thesis), which in result became the gateway to success in completing my research work, was born while I was

going out with her. Ever since I married her, she has kept me in a good shape with her brilliant cooking skills. Also, her patience and understandings enabled me to complete my PhD work while our friends went travelling during holiday seasons. I am indeed delighted to dedicate this thesis to her.

Yasutaka Haga

Abstract

This thesis presents a collection of new novel techniques using the bulk-driven approach, which can lead to performance enhancement in the field of CMOS analogue amplifier design under the very low-supply voltage constraints. In this thesis, three application areas of the bulk-driven approach are focused – at the input-stage of differential pairs, at the source followers, and at the cascode devices.

For the input stage of differential pairs, this thesis proposes two new novel circuit design techniques. One of them utilises the concept of the replica-biased scheme in order to solve the non-linearity and latch-up issues, which are the potential problems that come along with the bulk-driven approach. The other proposed circuit design technique utilises the flipped voltage scheme and the Quasi-Floating Gate technique in order to achieve low-power high-speed performances, and furthermore the reversed-biased diode concept to overcome the issue of degraded input impedance characteristics that come along with the bulk-driven approach.

Applying the bulk-driven approach in source followers is a new type of circuit blocks in CMOS analogue field, in which to the author's best knowledge has not been proposed at any literatures in the past. This thesis presents the bulk-driven version of the flipped voltage followers and super source followers, which can lead to eliminating the DC level shift. Furthermore, a technique for programming the DC level shift less than the

threshold voltage of a MOSFET, which cannot be achieved by conventional types of source followers, is presented.

The effectiveness of the cascode device using the bulk-driven approach is validated by implementing it in a complete schematics design of a fully differential bulk-driven operational transcoductance amplifier (OTA). This proposal leads to solving the low-tranconductance problem of a bulk-driven differential pair, and in effect the open loop gain of the OTA exceeds 60dB using a 0.35μm CMOS technology.

The final part of this thesis provides the study result of the input capacitance of a bulk-driven buffer. To verify the use of the BSIM3 MOSFET model in the simulation for predicting the input capacitance, the measurement data of the fabricated device are compared with the post-layout simulation results.

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List of Acronyms

Name	*Definition*	*Section defined*
BDCCM	Bulk-Driven Cascoded Current Mirror	5.1.2
BDDRB	Bulk-Driven Double Replica-Biased	3.1.2
BDDP	Bulk-Driven Differential Pair	3.1.1, 5
BDFVDP	Bulk-Driven Flipped Voltage Differential Pair	3.2.3
BDFVF	Bulk-Driven Flipped Voltage Follower	3.2.3, 4.1.3
BDSSF	Bulk-Driven Super Source Follower	4.2.2
CMFB	Common-Mode Feedback	5.1.2
FVF	Flipped Voltage Follower	4.1.1
FVFDP	Flipped Voltage Follower pseudo Differential Pair	3.2.2
GBW	Gain-Bandwidth	3.2.4
ICMR	Input Common-Mode Range	2.1
ITRS	International Technology Roadmap for Semiconductor	1.1
JFET	Junction Field Effect Transistor	2.1
OTA	Operational Transconductance Amplifiers	1.4, 3, 5
PSRR	Power Supply Rejection Ratio	3.2.4, 5
QFG	Quasi-Floating Gate	3.2.3, 4.2.2
RBS	Replica-Biased Scheme	3.1.1
SR	Slew-Rate	3.1.1, 4.2.2
SSF	Super Source Follower	4.2.1
THD	Total Harmonic Distortion	4.1.4

List of Symbols and Common MOSFET Equations

As this thesis consists of various equations with many symbols, the meaning of variables and physical constants are listed below so that readers can refer easily. Also, common MOSFET equations and a general note about the symbol convention are provided. [SED11], [JOH97], [ALL02], [BAK08], [GRA01]

List of Symbols

Symbols used in this thesis	*Description*	*Units*
	Physical constants	
ε_0	Permittivity of free space = 8.854×10^{-14} F/cm	F/cm
ε_{Si}	Permittivity of silicon = $11.7\ \varepsilon_0 = 1.036 \times 10^{-12}$ F/cm	F/cm
ε_{OX}	Permittivity of $SiO_2 = 3.97\ \varepsilon_0 = 3.52 \times 10^{-13}$ F/cm	F/cm
k	Boltzmann's constant = 1.38×10^{-23} J/K	J/K
q	Charge of electron = 1.062×10^{-19} C	C
n_i	Intrinsic concentration of silicon = 1.45×10^{10} /cm^3 at 300°K	/cm^3
	Temperature parameters	
T	Temperature in degree Kelvin = 300°K at room temperature	K
V_t	Thermal voltage (= 25.9mV at room temperature) $V_t = \frac{kT}{q}$ *Note: In this thesis, the thermal voltage is represented by V_t (i.e. uppercase symbol with lowercase subscript), whereas the threshold voltage is represented by V_T (i.e. uppercase symbol with uppercase subscript).*	V

	Basic MOSFET parameters	
g_m	Transconductance of a gate-driven MOSFET	Ω^{-1}
g_{mb}	Transconductance of a bulk-driven MOSFET	Ω^{-1}
g_d	Transconductance seen from the drain of a MOSFET	Ω^{-1}
t_{ox}	Gate-oxide thickness (SPICE parameter = TOX)	m
C_{ox}	Gate-oxide thickness (SPICE parameter = TOX) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	F/m^2
μ	Carrier mobility (SPICE parameter = U0)	$cm^2/V \cdot s$
λ	Channel-length modulation coefficient (SPICE parameter = LAMBDA)	V^{-1}
	Threshold voltage parameters	
V_{T0}	Zero-bias threshold voltage (SPICE parameter = VT0)	V
N_A, N_D	Substrate doping (SPICE parameter = NSUB) N_A = Number of acceptors in the p-type semiconductor N_D = Number of donors in the n-type semiconductor	$/cm^3$
γ	$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}}$ = body-effect coefficient (or bulk-threshold) of p-type semiconductor $\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_D}}{C_{ox}}$ = body-effect coefficient (or bulk-threshold) of n-type semiconductor (SPICE parameter = GAMMA)	$V^{1/2}$
$2\lvert\Phi_F\rvert$	$2\lvert\Phi_F\rvert = -V_t \ln (N_A/n_i)$ = Fermi potential of a p-type semiconductor $2\lvert\Phi_F\rvert = V_t \ln (N_D/n_i)$ = Fermi potential of an n-type semiconductor (SPICE parameter = PHI)	V

	MOSFET Diode Parameters	
I_S	Body-junction saturation current density (SPICE parameter = JS)	A/m^2
C_{J0}	Zero-bias body-junction capacitance, per unit area over the drain/source region (SPICE parameter = CJ)	F/m^2
MJ	Grading coefficient, for area component (SPICE parameter = MJ)	
C_{JSW0}	Zero-bias body-junction capacitance, per unit length alongF/m the sidewall (periphery) of the drain/source region (SPICE parameter = CJSW)	F/m
MJSW	Grading coefficient, for sidewall component (SPICE parameter = MJSW)	
V_0	Built-in voltage of an open-circuit pn junction, also known as bulk junction potential or barrier potential (SPICE parameter = PB) $V_0 = V_t \ln(\frac{N_A N_D}{n_i^2})$	V
	MOSFET Dimension Parameters	
AS, AD	Areas for source and drain (SPICE parameter = AS, AD)	m^2
PS, PD	Perimeters for source and drain (SPICE parameter = PS, PD)	m
	MOSFET Gate-Capacitance Parameter	
C_{GSO}	Gate-source overlap capacitance, per unit channel width (SPICE parameter = CGSO)	F/m

MOSFET Equations

Large-signal operation

	Linear Region	Saturated Region
I_D	$I_D = \mu_0 C_{OX} \frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$	$I_D = \frac{\mu_0 C_{OX}}{2} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
V_T	$V_T = V_{T0} + \gamma(\sqrt{2\lvert\Phi_F\rvert + v_{SB}} - \sqrt{2\lvert\Phi_F\rvert})$	

Small-signal operation

	Linear Region	Saturated Region
$g_m = \frac{\partial i_d}{\partial v_{gs}}$	$\beta V_{DS} = \mu_0 C_{OX} \frac{W}{L} V_{DS}$	$\mu_0 C_{OX} \frac{W}{L}(V_{GS} - V_T)(1 + \lambda V_{DS})$ $= \sqrt{2\mu_0 C_{OX} \frac{W}{L} I_D (1 + \lambda V_{DS})}$
$g_{mb} = \frac{\partial i_d}{\partial v_{bs}}$	$\eta g_m = g_m \frac{\gamma}{2\sqrt{2\lvert\Phi_F\rvert + V_{SB}}}$	
$g_d = \frac{\partial i_d}{\partial v_{ds}}$	$\beta(V_{GS} - V_T - V_{DS})$	$I_D \lambda$
C_{gs}	$C_{gs} = \frac{2}{3} WLC_{OX} + WC_{GSO}$	
C_{bd}	$\frac{C_{j0}}{(1 - \frac{V_{BS}}{V_0})^{MJ}} AS + \frac{C_{jSW0}}{(1 - \frac{V_{BS}}{V_0})^{MJSW}} PS$	
C_{ds}	$\frac{C_{j0}}{(1 - \frac{V_{BD}}{V_0})^{MJ}} AS + \frac{C_{jSW0}}{(1 - \frac{V_{BD}}{V_0})^{MJSW}} PS$	
f_T	$\frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})}$	

Symbol Convention

Unless otherwise stated, the following symbol convention is used to represent signals in this thesis:

Represented Symbol	***Meaning***
Uppercase symbols with uppercase subscripts (e.g. I_D)	Bias or DC quantities (e.g. the DC portion of transistor drain current)
Lowercase symbols with lowercase subscripts (e.g. i_d)	Small-signal quantities (e.g. the incremental change in transistor drain current)
Lowercase symbols with uppercase subscripts (e.g. i_D)	Sum of bias and small-signal quantities (e.g. the total transistor drain current, i.e. $i_D = I_D + i_d$)

Chapter 1 Introduction

1.1 Moore's Law and More

Complementary Metal-Oxide Semiconductor (CMOS) technology is continuously downscaling to increase the number of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) to be integrated in a single chip. Intel co-founder Gordon E. Moore postulated the trend in 1965, which is known as Moore's Law, that the number of transistors per chip doubles roughly every 2 years [MOR65]. Along with this integration level trend, the cost-per-function is decreased and thus economic productivity and in effect overall quality of life are significantly improved through proliferation of computers, communication, and other industrial and consumer electronics [ITR10]. This miniaturisation trend, however, cannot be continued forever. Semiconductors are getting harder to downscale, and eventually the level of integration would not scale with Moore's Law anymore. Figure 1-1 shows how the International Technology Roadmap for Semiconductor (ITRS) draws the CMOS technology roadmap for the next decades.

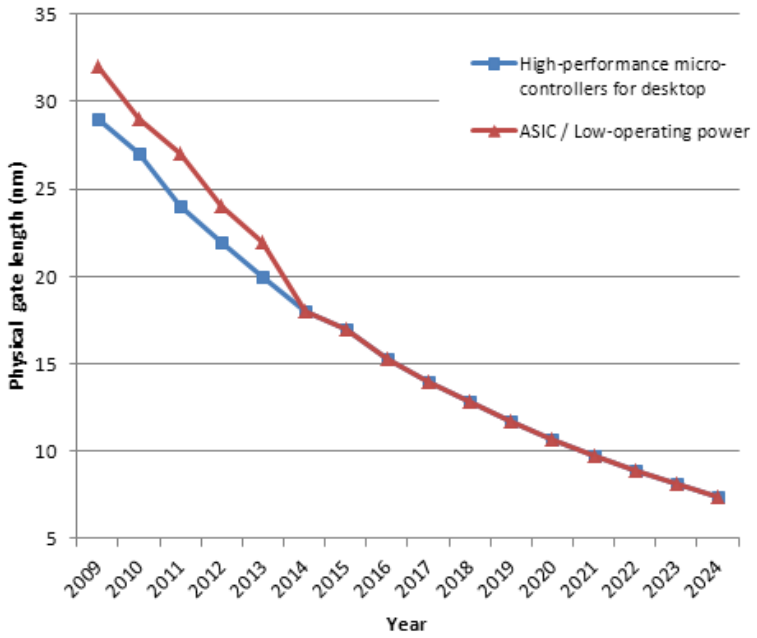


Figure 1-1 CMOS Technology Roadmap [ITR10]

In order to keep up responding to the requirements in the economy growth and improving the quality of life despite the scaling limits according to Moore's Law which would come in the next decade, the ITRS has addressed a new concept of research target called "Moore's Law and More". This concept is constructed by three sub-sets of focus area – *scaling, functional diversification,* and *beyond CMOS. Scaling* (which is also known as *more Moore*) refers to not only the continued shrinking of transistors but also includes non-geometrical process techniques such as study of new materials that affect the electrical performance of the chip, as well as design technologies that enable high performance, low power, high reliability, low cost, and high design productivity. *Functional diversification* (which is also known as *more than Moore*) aims to provide additional value, in particular non-digital functionalities (e.g. RF communication), to be migrated from the system board level into package-level (system-in-package, SiP) or chip-level (System-on-Chip, SoC). *Beyond CMOS* focuses on a "new switch" that can provide substantial functional scaling beyond that attainable by ultimately scaled CMOS. In the field of *Beyond CMOS*, the ITRS lists some examples like carbon-based nano-electronics, spin-based

devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system (NEMS) switches.

This CMOS technology trend introduces a new issue and consequently a motivation of new development in the area of CMOS analogue circuit design, which is described in the next section.

1.2 Supply Voltage Trend

Along with the scaling trend of CMOS technology, the ITRS set the target of research effort towards lowering of supply voltages, since small transistors suffer from reduced voltage breakdowns (which is known as hot carrier effect) [ITR10]. Figure 1-2 shows how the ITRS draws the roadmap of supply voltage reduction for analogue and digital systems.

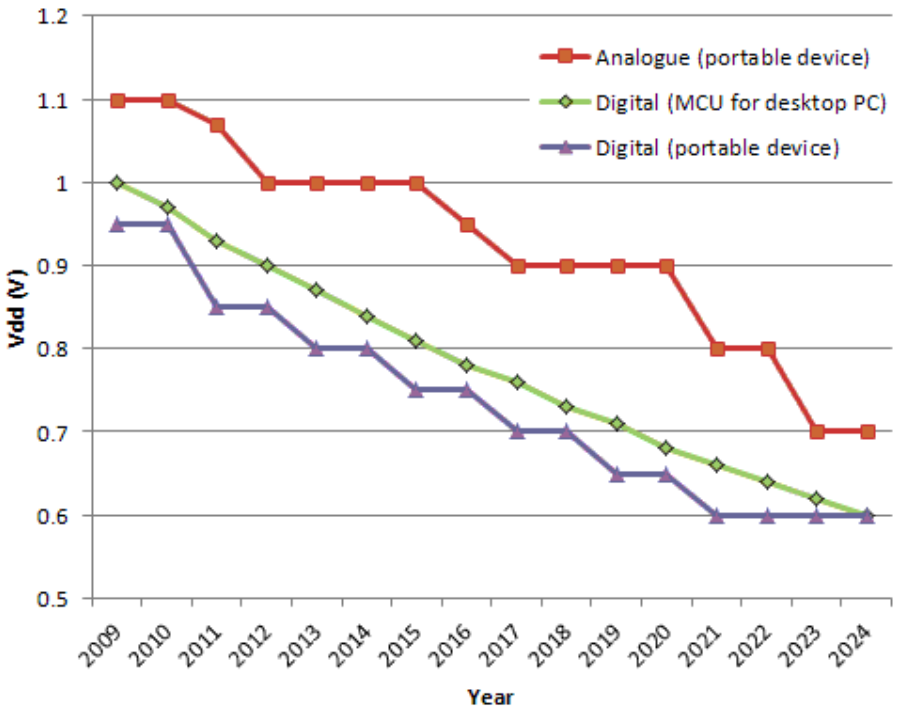


Figure 1-2 Supply Voltage Reduction Roadmap [ITR10]

With Figure 1-2, the ITRS describes that the supply voltage reduction for analogue systems will continue to lag that of digital systems by two or more generations, due to the fact that the threshold voltage for CMOS technology is not expected to be decreased drastically. In digital systems, a threshold voltage too close to zero would cause appreciable leakage current to flow into logic devices even when they are off, which would result to increased power dissipation as the leakage current gets multiplied by the number of logic devices integrated in the digital system [ALL02]. Thus, from this reason the threshold voltage cannot be significantly reduced, which causes an issue from analogue circuit designers' viewpoint since conventional design techniques cannot fit into the ITRS roadmap. There is a need for new development of analogue circuit design techniques to overcome this dilemma.

1.3 Rail-to-Rail Analogue Voltage Buffer and the Bulk-Driven Approach

One particular example where new circuit design techniques are needed for low-voltage systems is analogue voltage buffers. Voltage buffers, which are usually constructed with an operational amplifier (op-amp) in unity-gain voltage configuration as illustrated in Figure 1-3(a), are essential building blocks for applications where the weak signal needs to be delivered to a large capacitive or a small resistive load without being distorted. In order to maximise the dynamic range under the low supply voltage constraint, rail-to-rail input and output stages are required for those op-amps.

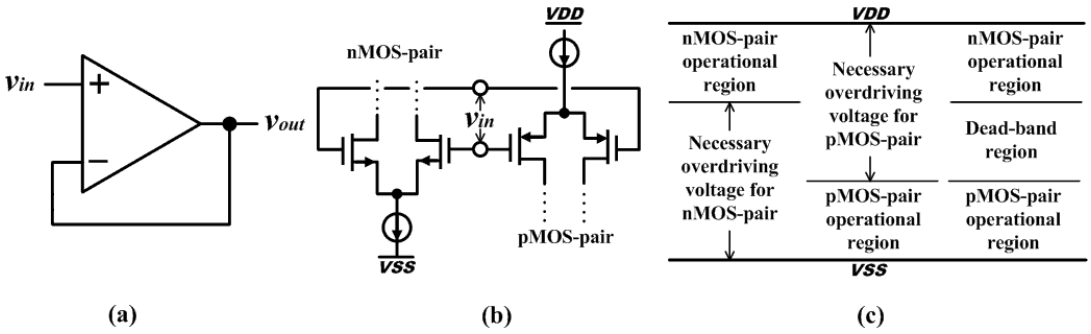


Figure 1-3 (a) Op-amp in unity-gain configuration, (b) complementary differential pair, and (c) illustration describing dead-band region under low-supply voltage condition

For the input stage, the conventional circuit design approach for achieving rail-to-rail operation has been to utilise both p-type (pMOS) and n-type (nMOS) of the differential pairs as shown in Figure 1-3(b). However, as illustrated in Figure 1-3(c), the supply voltage being too low would cause a dead-band of the operational area where neither pMOS nor nMOS pairs can detect the input. In order to operate with this conventional circuit design approach, its supply voltage needs to be much greater than $2V_T + 2V_{DSmin}$, where V_T is the threshold voltage of the MOSFET and V_{DSmin}, is the minimum required voltage of drain-to-source voltage of the MOSFET. Considering that V_T varies by the bulk (or body) biasing voltage, the chip (or junction) temperature, and the process variation for the CMOS technology, a new circuit design approach such that the rail-to-rail operation can be achieved with a supply voltage near V_T is rather in favour for the ITRS roadmap.

A candidate of circuit design techniques that can achieve rail-to-rail input operation with low supply voltages is the bulk-driven approach, which utilises the bulk of the MOSFET instead of the gate for applying the signal. Figure 1-4 illustrates this approach. With this technique the amount of supply voltage can be reduced to near V_T, however many drawbacks have been reported in [BLA98]. The author's research work solely focuses on the bulk-driven approach in order to develop new circuit design techniques that can overcome those drawbacks.

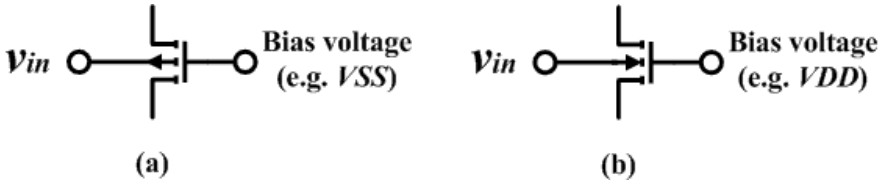


Figure 1-4 (a) pMOS bulk-driven device, and (b) nMOS bulk-driven device

1.4 Research Objective and Thesis Outline

The research theme reported in this thesis is the bulk-driven approach. The research objective is to develop new circuit design techniques using the bulk-driven approach that can overcome many of those drawbacks which have been reported by literatures, and furthermore invent new ways application areas of the bulk-driven approach that can lead to performance enhancement in the field of CMOS analogue amplifier design. This thesis is structured as follows:

Chapter 2 provides a general overview of the bulk-driven approach. The device physics, operation principle and mathematical modelling, and drawbacks of this circuit design approach are discussed.

Chapter 3 focuses on the circuit design techniques of rail-to-rail input stage for analogue amplifiers using the bulk-driven approach. This chapter reviews previous works and proposes a novel new circuit design technique that solves the issues of nonlinearity and latch up. Furthermore, another new circuit design technique that can achieve low-power high-speed performances whilst minimise the issue of low-input resistance large input capacitance of the bulk-driven approach is also proposed.

Chapter 4 presents a new invention of designing source followers using the bulk-driven approach, which in author's best knowledge has not been proposed in

literatures before. A new design technique of source followers such that the DC level shift can be freely programmed is proposed in this chapter.

Chapter 5 proposes a new way of utilising the bulk of the cascode devices at the output stage of Operational Transconductance Amplifiers (OTA), which leads to enhanced output resistance without having any additional hardware in the core part of the OTA.

Chapter 6 focuses on the study of the input capacitance of a bulk-driven buffer. To verify the use of the BSIM3 MOSFET model in the simulating for predicting the input capacitance, the measurement data of the fabricated device compared with the simulated results using the extracted netlist of the postlayout design.

Chapter 7 is the concluding session of this research work. The summary of this work and the author's recommendations for further work are provided.

Lastly, Appendix A provides the copies of the author's publications, Appendix B provides the supplementary information to Chapter 6 (including the SPICE code used for the simulation, the IC layout of the whole die and the bonding diagram, more snapshots of the microphotograph, and the used test board for the measurement), and Appendix C lists the logs of the measurement results of the input capacitance of the fabricated bulk-driven buffer presented in Chapter 6.

1.5 List of the Author's Publications

The author's research works documented in this thesis are based on the following publications:

[HAG05] Y. Haga, H. Zare-Hoseini, L. Berkovi, and I. Kale, "Design of a 0.8 Volt Fully Differential CMOS OTA Using the Bulk-Driven Technique", *IEEE Proc. International Symposium in Circuits and Systems*, 2005, pp. 220 – 223

[HAG06] Y. Haga, R. C. S. Morling, and I. Kale, "A New Bulk-Driven Input Stage Design for sub 1-volt CMOS Op-Amps", *IEEE Proc. International Symposium in Circuits and Systems*, 2006, pp.1547 – 1550

[HAG09A] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp.2717 – 2720

[HAG09B] Y. Haga and I. Kale, "CMOS Buffer Using Complementary Pair of Bulk-Driven Super Source Followers", *IEEE Electronic Letters*, Vol. 45, Issue 18, 2009, pp. 917 – 918

[HAG09C] Y. Haga and I. Kale, "Class-AB Rail-to-Rail CMOS Buffer with Bulk-Driven Super Source Followers", *IEEE European Conference on Circuit Theory and Design*, 2009, pp. 695 – 698

[HAG10] Y. Haga and I. Kale, "Bulk-Driven Flipped Differential Pair", *IEEE Proc. PhD Research in Microelectronics and Electronics*, 2010

[HAG11] Y. Haga and I. Kale, "Bulk-Driven DC Level Shifter", *IEEE Proc. International Symposium in Circuits and Systems*, 2011, pp.2039-2042

The knowledge contributions of the above publications are summarised in the next section.

1.6 Knowledge Contributions

The work presented in this thesis, which includes several novel proposals of circuit design techniques that utilise the bulk-driven approach, is solely developed by the author. The novelties of these developed techniques, which greatly help enhancing performances in the CMOS analogue amplifier design field, are described below:

Applying the proposal at the input stage of CMOS analogue amplifiers not only leads to providing rail-to-rail operation at extremely low supply voltage condition, but also improves the linearity and furthermore enhances the latch up immunity [HAG06]. In fact there are several previously proposed works that improve the linearity of the bulk-driven approach, however in the author's best knowledge there is no publication of the technique that can enhance the latch up immunity.

This thesis also presents another input stage design technique utilising the bulk-driven approach, which achieves low-power high-speed performances and helps reducing the input capacitance [HAG10]. A new concept of utilising a reversed-biased diode with the bulk-driven MOSFET is introduced.

Applying the bulk-driven approach in source follower design is a complete new way of circuit design techniques. The bulk-driven approach allows the DC level shift to be freely programmed, which has not been possible to do with conventional source followers [HAG09A], [HAG09B], [HAG09C], [HAG11].

Utilising the bulk-driven approach in the cascode devices of the OTA is also a complete new design method, which leads to increasing the output resistance and

hence enhancing the open-loop gain of the OTA without the need of any extra hardware in the core part of the OTA [HAG05].

With the above contributions to knowledge, the author aims to make for the readers of this thesis to realise that the bulk-driven approach has many new possible ways to be applied in CMOS analogue amplifier design for further performance improvement, and to encourage for new researchers to continue with developing modified techniques of the bulk-driven approach.

1.7 Impact of this Work

This last section of the Chapter aims to demonstrate the impact of this research work.

During the research activities, the author noticed that the work reported in this thesis has been cited by several institutions' works. Section 1.7.1 shows the list of citations to the author's publications which the author is aware of.

The BDFVDP reported in Chapter 3 of this thesis, which is the work the author published in [HAG10], received the Gold Leaf Certificate from PhD Research In Microelectronics and Electronics (PRIME). In Section 1.7.2, the scanned copy of the received award is shown.

1.7.1 The List of "Referred" Publications

The List of Citations to [HAG05]

[AGG09] B. Aggarwal and M. Gupta, "Low-Voltage Cascode Current Mirror based on Bulk-Driven MOSFET and FGMOS techniques", *IEEE Proc. International Conference on Advances in Recent Technologies in Communication and Computing*, 2009, pp. 474 – 477

[BAU07] F. Bautista, S. O. Martínez, G. Dieck, and O. Rossettoy, "An ultra-low voltage high gain operational transconductance amplifier for biomedical applications", *Workshop on Design and Architectures for Signal and Image Processing (DASIP)*, 2007, Grenoble: France

[CAR09] J. M. Carrillo, R. Pérez-Aloe, J. M. Valverde, and J. F. Duque-Carrillo, "Compact Low-Voltage Rail-to-Rail Bulk-Driven CMOS Opamp for Scaled Technologies", *IEEE Proc. European Conference on Circuits Theory and Design*, 2009, pp. 263 – 266

[CAR10] J. M. Carrillo, G. Torelli, R. Pérez-Aloe, J. M. Valverde, and J. F. Duque-Carrillo, "Single-pair bulk-driven CMOS input stage: A compact low-voltage analog cell for scaled technologies" *Integration*, *the VLSI Journal*, 2010, Vol.43, Issue 3, pp. 251 – 257, Elsevier

[CAR11] J. M. Carrillo, G. Torelli, M. A. Domínguez, and J. F. Duque-Carrillo, "On the input common-mode voltage range of CMOS bulk-driven input stages", *International Journal of Circuit Theory and Applications*, 2011, 39, pp. 649 – 664, Wiley Online Library

[CHA10] C. Chanapromma and K. Daoden, "A CMOS Fully Differential Operational Transconductance Amplifier Operating in Sub-threshold Region and Its Application", *IEEE Proc. International Conference on Signal Processing Systems*, 2010, pp. V2-73 – V2-77

[HE06] X-Y He, K-P Pun, C-S Choy, and C-F Chan, "A 0.5V Fully Differential OTA with Local Common Feedback", *IEEE Proc. International Symposium on Circuits and Systems*, 2006, pp. 1559 – 1562

[KHA10] H. Khameh and H. Shamsi, "A Sub-1V High-Gain Two-Stage OTA Using Bulk-Driven and Positive Feedback Techniques", *IEEE Proc. European Conference on Circuits and Systems for Communications*, 2010, pp. 103 – 106

[LAY08] K. D. Layton, D. T. Corner, and D. J. Corner, "Bulk-driven gain-enhanced fully-differential amplifier for VT + 2Vdsat operation", *IEEE Proc. International Symposium on Circuits and Systems*, 2008, pp. 77 – 80

[LI10] Y. Li, C. C. Y. Poon, and Y-T Zhang, "Analog Integrated Circuits Design for Processing Physiological Signals", *IEEE Reviews in Biomedical Engineering*, 2010, Vol. 3, pp. 93 – 105

[PAN09] S-W Pan C-C Chuang C-H Yang and Y-S Lai, "A novel OTA with dual bulk-driven input stage", *IEEE Proc. International Symposium on Circuits and Systems*, 2009, pp. 2721 – 2724

[RAI10] G. Raikos and S. Vlassis, "0.8 V Bulk-Driven Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, 2010, 63, pp. 425 – 432, Springer

[ROH10] H. Roh, H. Lee, Y. Choi, and J. Roh, "A 0.8-V 816-nW delta–sigma modulator for low-power biomedical applications", *Analog Integrated Circuits and Signal Processing*, 2010, 63, pp. 101 – 106, Springer

[TAI06] C-F Tai, J-L Lai, and R-J Chen, "Using Bulk-driven Technology

Operate in Subthreshold Region to Design a Low Voltage and Low Current Operational Amplifier", *IEEE Proc. International Symposium on Consumer Electronics*, 2006, pp. 1 – 5

[ZAB07] S. A. Zabihian, and R. Lotfi, "Ultra-Low-Voltage, Low-Power, High-Speed Operational Amplifiers Using Body-Driven Gain-Boosting Technique", *IEEE Proc. International Symposium on Circuits and Systems*, 2007, pp. 705 – 708

The List of Citations to [HAG06]

[CAR11] J. M. Carrillo, G. Torelli, R. Pérez-Aloe, J. M. Valverde, and J. F. Duque-Carrillo, "On the input common-mode voltage range of CMOS bulk-driven input stages", *International Journal of Circuit Theory and Applications*, 2011, 39, pp. 649 – 664, Wiley Online Library

[LI10] Y. Li, C. C. Y. Poon, and Y-T Zhang, "Analog Integrated Circuits Design for Processing Physiological Signals", *IEEE Reviews in Biomedical Engineering*, 2010, Vol. 3, pp. 93 – 105

[RAI10] G. Raikos and S. Vlassis, "0.8 V Bulk-Driven Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, 2010, 63, pp. 425 – 432, Springer

The List of Citations to [HAG09A]

[KHA11] F. Khateb, N. Khatib, and D. Kubánek, "Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascade

OTA", *Microelectronics Journal*, 2011, 42, pp. 622 – 631, Elsevier

[RAI10] G. Raikos and S. Vlassis, "0.8 V Bulk-Driven Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, 2010, 63, pp. 425 – 432, Springer

[YOD10] A . Yodtean, P. Isarasena, and A. Thanachayanont, "0.8-µW CMOS Bulk-Driven Linear Operational Transconductance Amplifier in 0.35-µm Technology", *IEEE Proc. Asia Pacific Conference on Circuits and Systems*, 2010, pp. 784 – 787

The List of Citations to [HAG09B]

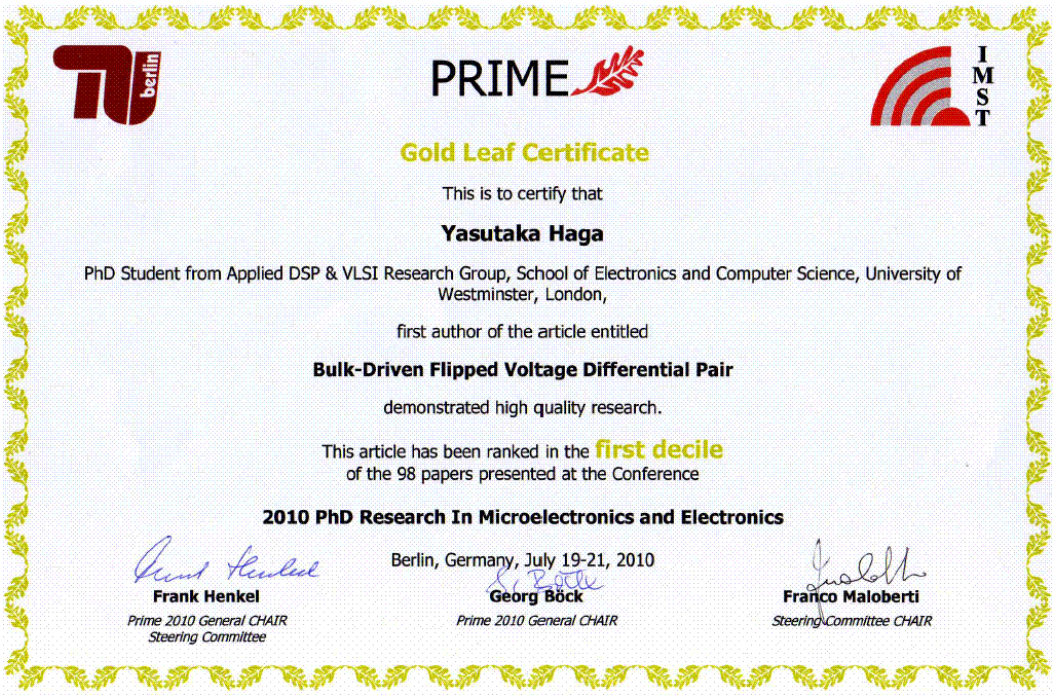
[URB11] C. Urban, J. E. Moon, and P.R. Mukund, "Scaling the Bulk-Driven MOSFET into Deca-Nanometer Bulk CMOS Processes", *Microelectronics Reliability Journal*, 2011, 51, pp. 727 – 732, Elsevier

The List of Citations to [HAG09C]

[KUM11] M. Kumar and G. Kumar, "Optimization Techniques for Source Follower Based Track-and-Hold Circuit for Wireless High Speed Wireless Communication", *AIRCC International Journal of VLSI design & Communication Systems*, 2011, Vol.2, No. 1, pp. 45 – 59

[MAR11] A. L. Martin, J. M. A. Miguel, L. Acosta, J. Ramírez-Angulo, and R. G. Carvajal, "Design of Two-Stage Class AB CMOS Buffers: A Systematic Approach", *ETRI Journal*, 2011, Vol.33, No.3, pp. 393 - 400

1.7.2 The Scanned Copy of the Gold Leaf Certificate Awarded by PRIME'10



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Chapter 2 Characterising the Bulk-Driven Approach

This chapter provides an overview of the bulk-driven approach, which is essential to be understood in prior to assessing the bulk-driven circuit design. The benefit of the bulk-driven approach, the device realisation in CMOS technology, and the drawbacks are thoroughly discussed.

2.1 The Benefit of Utilising the Bulk-Driven Approach

The benefit of the bulk-driven approach can be easily realised by simulating its transconductance characteristics and comparing with the gate-driven approach. Figure 2-1 shows the simulated plot of the gate-driven and the bulk-driven nMOS transistors using a 0.35µm CMOS technology.

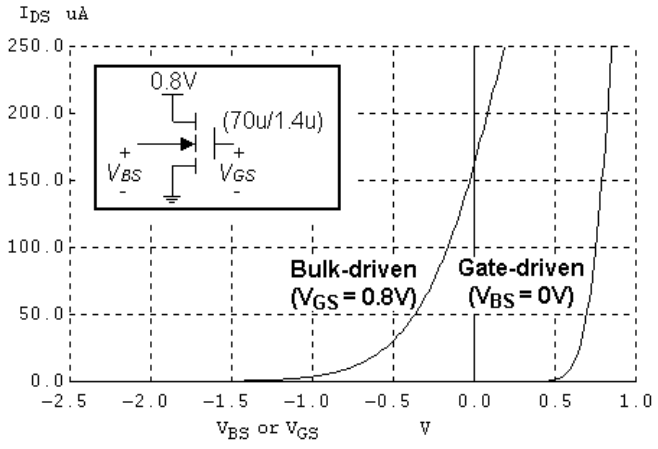


Figure 2-1 Simulating transconductance characteristics of gate-driven and bulk-driven nMOS transistors using a 0.35µm CMOS technology

As can be seen in Figure 2-1, to operate the gate-driven MOS transistor in the active region, the gate-to-source voltage needs to be greater than the threshold voltage (which is approximately 0.6 volts in this case). On the other hand, the bulk-driven MOS transistor behaves in a similar fashion to a depletion MOS transistor or a Junction Field Effect Transistor (JFET). Therefore, with the zero-bias voltage at the input node, the transistor is still in the active region.

This characteristic is the key benefit we use in designing low-supply voltage op-amps and other analogue circuits, as the bulk-driven device allows an extension in its input range on the negative side and hence leads to improving the Input Common-Mode Range (ICMR).

2.2 Realising the Bulk-Driven Device in CMOS Technology

This section describes how a bulk-driven device is realised in CMOS technology, which is an important topic to be covered before discussing the drawbacks of the bulk-driven approach. Case studies of the realisation in n-well type and in twin-well type of CMOS technologies are discussed.

2.1.1 Bulk-Driven Device Realised in N-Well CMOS Technology

In semiconductor market today n-well CMOS technologies are more popular than p-well types, since n-types ones allows the substrate to be connected to the ground instead of the supply voltage, which is in more favour by circuit designers [SAN06], [YTT03]. Thus, it is essential to discuss the realisation of a bulk-driven device in n-well CMOS technology.

In n-well CMOS technology, pMOS can be bulk-driven. Figure 2-2 illustrates the cross sectional view of how the pMOS bulk-driven device can be realised in an n-well CMOS technology.

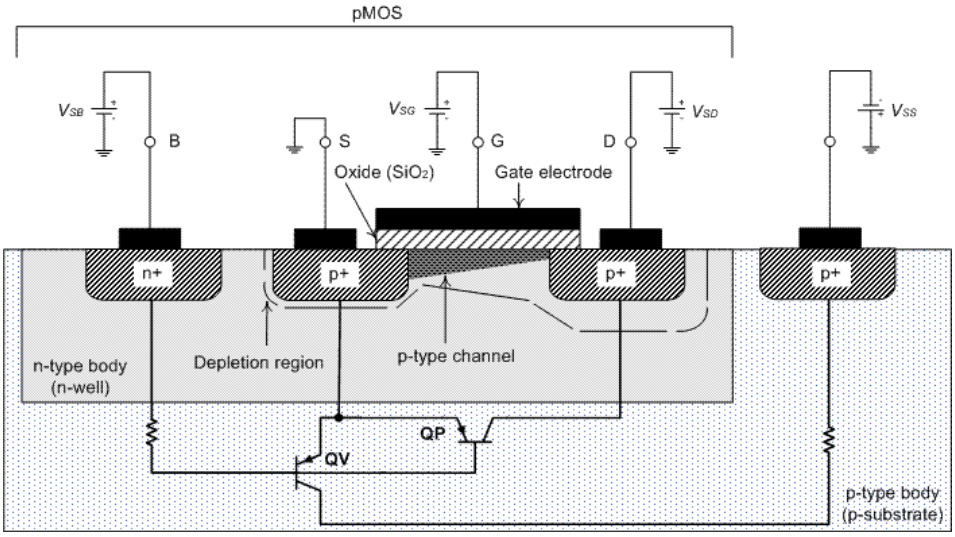


Figure 2-2 Cross sectional view of a bulk-driven pMOS device in an n-well CMOS technology

The operation principle of a bulk-driven device is simple to follow. The voltage at the bulk affects the depletion region depicted in Figure 2-2, which in effect controls the channel and hence the drain current. Let's suppose that the pMOS device formed in the n-well in Figure 2-2 is in linear region, and thus the depth of the p-type channel is narrower at the drain than the source, as shown in the sketch. As the voltage potential at the bulk of the pMOS device is increased above the source, the depletion region becomes widened and hence the p-type channel reduces its overall depth, and eventually the channel is pinched off at the drain end so that the pMOS device becomes saturated [ALL02].

The behaviour of the reduced channel depth can be alternatively described that the overvoltage of the pMOS device is decreased when the bulk voltage increases above the source voltage V_{SB} [SED11]. However, since the gate voltage of the pMOS

device V_{SG} remained unchanged, the threshold voltage V_T increased instead. This V_T behaviour can be mathematically modelled by:

$$V_T = V_{T0} + \gamma(\sqrt{2|\Phi_F| + V_{SB}} - \sqrt{2|\Phi_F|}) \quad (2\text{-}1)$$

where V_{T0} is the threshold voltage at zero-bias (i.e. V_{SB}=0), γ is the body-effect coefficient, and $2|\Phi_F|$ is the Fermi potential, which are all dependent of the CMOS technology. Hence in summary, with the bulk-driven approach the drain current is controlled by varying V_T instead of V_{SG}.

From Figure 2-2 it is important to realise the parasitic bipolar effect, which are denoted as QP and QV in the sketch, since this parasitic effect contributes to one of the severe drawbacks of the bulk-driven approach. More detail discussions of this drawback is covered in Section 2.3.

Finally, it is worth adding a comment that a bulk-driven transistor is often said to be in *depleted-mode* [BLA96] since the voltage potential at the bulk affects the shape of the depletion region. However, in terms of device physics the actual MOS transistor that is dealt with is enhancement type, thus this discussion may cause confusion by first-time learners of the bulk-driven approach.

2.1.2 Bulk-Driven Device Realised in Twin-Well CMOS Technology

Since twin-well CMOS technology is also available today, it is also worth discussing how a bulk-driven device can be realised in this technology. The cross section view is sketched in Figure 2-3.

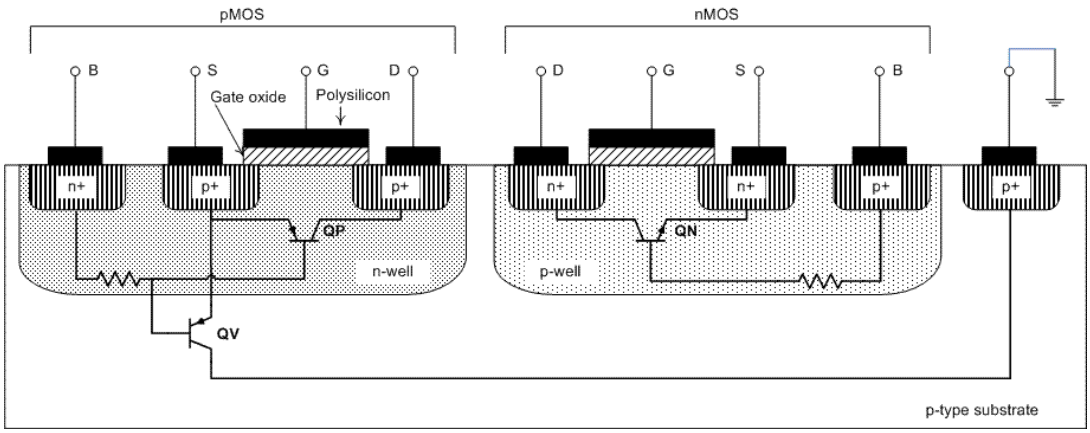


Figure 2-3 Cross sectional view of twin-well CMOS technology

In the previous section it was discussed that only pMOS can be bulk-driven in n-well technology. In twin-well technology, on the other hand, nMOS device can also be bulk-driven since the device has an isolated body (bulk) in p-well instead of the common p-substrate.

As can be observed from Figure 2-3, the parasitic bipolar effect for the pMOS formed in twin-well technology remains in identical manner as the pMOS device formed in n-well technology. This is because, in either case, the n-well is formed in p-substrate. In contrast, with the nMOS there is only one type of bipolar effect denoted by QN. This is because p-well and p-substrate are not related by pn-junction effect since they both have the p-type of polarity.

It is worth noting that this technology allows separate optimization of the nMOS and pMOS transistors [SED11], and therefore many submicron processes are based on this technology. As mentioned before, with this technology both pMOS and nMOS devices can be bulk-driven. However for fabless semiconductor companies where the fabrication needs to be outsourced, there might be a case that the foundry allows layout designers to draw only n-well layers but not p-well layers [MOS11], which consequentially means that layout designers cannot assign nMOS devices to be

individually bulk-driven. This matter has to be identified before starting the circuit design.

2.3 Drawbacks Introduced with the Bulk-Driven Approach

In Section 2.1 the benefit of the bulk-driven approach has been described that the transistor can be utilised in depleted-mode similar like JFET. However, many associated drawbacks have been reported in [BLA98]. This section thoroughly discusses these drawbacks, as they are essential to be understood in prior to assessing the bulk-driven circuit design.

2.3.1 Transconductance Reduction

One significant disadvantage of the bulk-driven approach is that the transconductance of a bulk-driven MOSFET g_{mb} is substantially less than a gate-driven MOSFET g_m. As can be realised from Figure 2-1, the slope of the bulk-driven MOSFET (= g_{mb}) is much gentle than the slope of the gate-driven MOSFET (= g_m). The g_{mb}/g_m ratio, η, can be expressed by

$$\eta = g_{mb} / g_m = \frac{\gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} \tag{2-2}$$

where $2|\Phi_F|$ is the Fermi potential, γ is the body-effect coefficient, and V_{BS} is the bulk-to-source voltage of the MOSFET. This ratio η is thus dependent to V_{BS}, but it is typically around 0.1 to 0.3 [SED11].

2.3.2 Transconductance Variation

It can be also noted from Equation (2-2) that g_{mb} (= η g_m) is dependent to V_{BS}, which causes a substantial transconductance variation when a bulk-driven MOSFET is applied in a differential pair design.

2.3.3 Process Related

As discussed in Section 2.2, the polarity of the bulk-driven MOS transistor is process related because *wells* are required to isolate bulk-terminals. In case of n-well CMOS technology, only pMOS devices can be bulk-driven. For applications where both pMOS and nMOS devices are required, a twin-well technology is needed.

2.3.4 Degraded Latch up Immunity

As can be observed from Figure 2-2 and 2-3, CMOS technologies consist of parasitic bipolars. If for instance any of those bipolars, in particular vertical bipolars QV, are turned on, then there would be a short-circuit path between positive and negative supply rails. In digital systems this is known as a latch up effect, which may cause destructive breakdown of the chip.

To minimise this unwanted effect to happen, the forward-bias voltage of the bulk of the MOSFET must be kept as small as possible in order not to strongly turn on the parasitic bipolars [BLA98].

2.3.5 Degraded Input Impedance Characteristics

With the bulk-driven approach, the input impedance characteristics become worse due to the parasitic bipolars. The resistive and input capacitive characteristics of the bulk-driven input are thoroughly discussed below:

Input Resistance

As illustrated in Figure 2-2, the bulk of the MOSFET is the base terminal of the parasitic bipolar. Therefore some appreciable input current i_B may flow. i_B can be expressed by

$$i_B = I_S[\exp(\frac{qv_{BS}}{kT}) - 1] \tag{2-3}$$

where I_s is the pn-junction current, which is also known as the scale current when the voltage across the pn-junction v_{BS} is zero, k is the Boltzmann constant (=1.38 x 10^{-23}JK^{-1}), T is the temperature in Kelvin, and q is the charge of an electron (=1.602 x 10^{-19}C). I_s can be expressed by

$$I_S = A_S q n_i^{\,2}(\frac{D_P}{L_P N_D} + \frac{D_n}{L_n N_A}) \tag{2-4}$$

where A_S is the active area of the source of the MOSFET, N_A and N_D are the doping concentrations of the acceptors and donors respectively, L_n and L_p are the diffusion length of holes and electrons respectively, D_p and D_n are the diffusion constant of holes and electron respectively, and n_i is the number of free electrons and holes in a unit volume of intrinsic temperature at a given temperature (≈1.5 x 10^{10} carriers/cm^3 at room temperature).

Input Capacitance

The capacitance of the bulk-driven device can also be understood from the study of bipolar devices. As illustrated in Figure 2-2, the bulk-driven input consists of two

types of bipolars, QP and QV, which are classified as a lateral bipolar and a vertical bipolar, respectively.

From the bipolar characteristics modelling for QP, the source-to-bulk depletion capacitance $C_{sb\text{-}depletion}$ can be expressed by

$$C_{sb-depletion} = \frac{CJ_{nwell-p+}}{(1-\frac{V_{SB}}{V_0})^{MJ_{nwell-p+}}} AS + \frac{CJSW_{nwell-p+}}{(1-\frac{V_{SB}}{V_0})^{MJSW_{nwell-p+}}} PS \quad (2\text{-}5)$$

where $CJ_{nwell\text{-}p+}$ is the zero-bias (i.e. V_{SB}=0) body-junction capacitance per unit area over the drain/source region, $CJSW_{nwell\text{-}p+}$ is the zero-bias body-junction capacitance per unit length along the sidewall of the drain/source region, $MJ_{nwell\text{-}p+}$ and $MJSW_{nwell\text{-}p+}$ are the grading coefficient for area and sidewall components respectively, V_0 is the body-junction built-in potential, and AS and PS are the area and the perimeters of the source region of the MOSFET respectively. As can be realised from this equation, forward-bias (i.e. V_{SB}>0) operation of a bulk-driven MOSFET causes an increase in $C_{sb\text{-}depletion}$.

Furthermore, from the study of bipolar characteristics, the diffusion capacitance $C_{sb\text{-}diffusion}$ is introduced when the bulk is in forward-biased. $C_{sb\text{-}diffusion}$ can be expressed by

$$C_{sb-diffusion} = \frac{\tau_T}{V_t} i_B \quad (2\text{-}6)$$

where τ_T is the mean transit time of the junction and V_t is the thermal voltage (≈26mV at room temperature).

On the other hand, the pn-junction formed between n-well and p-substrate is never forward-biased since the most negative voltage is connected at the p-substrate. Hence

only depletion capacitance is introduced across this pn-junction. This junction capacitance, namely well-to-substrate capacitance C_{ssub}, can be expressed by

$$C_{ssub} = \frac{CJ_{nwell-psub}}{(1-\frac{V_{SB}}{V_0})^{MJ_{nwell-psub}}} A_{nwell} + \frac{CJSW_{nwell-psub}}{(1-\frac{V_{SB}}{V_0})^{MJSW_{nwell-psub}}} P_{nwell} \quad (2\text{-}7)$$

where $CJ_{nwell\text{-}psub}$ is the zero-bias (i.e. $V_{nwell\text{-}psub}$=0) body-junction capacitance per unit area over the n-well and p-substrate region, $CJSW_{nwell\text{-}psub}$ is the zero-bias body-junction capacitance per unit length along the sidewall of the n-well and p-substrate region, $MJ_{nwell\text{-}psub}$ and $MJSW_{nwell\text{-}psub}$ are the grading coefficient for area and sidewall components respectively, V_0 is the body-junction built-in potential, and A_{nwell} and P_{nwell} are the area and the perimeters of the n-well respectively.

In summary, the total capacitance of the bulk C_b is given by

$$C_b = C_{bs\text{-}depletion} + C_{bs\text{-}diffusion} + C_{ssub} \quad (2\text{-}8)$$

The C_b is significantly greater than the gate-to-source capacitance C_{gs}, given by

$$C_{gs} \approx \frac{2}{3} WLC_{OX} + WC_{GSO} \quad (2\text{-}9)$$

where W and L are the width and the length of the MOSFET respectively, C_{OX} is the oxide capacitance, and C_{GSO} is the gate-to-source overlap capacitance per unit channel width.

2.3.6 Reduced Bandwidth

Utilising bulk-driven devices also causes in speed reduction. For a gate-driven MOSFET in saturated region, its transitional frequency, $f_{T,\ gate\text{-}driven}$, is given by

$$f_{T,\ gate\text{-}driven} \approx \frac{g_m}{2\pi C_{gs}} \quad (2\text{-}10)$$

At the frequency beyond $f_{T,\ gate\text{-}driven}$, the device no longer provides signal gain. In a case of a bulk-driven MOSFET in saturated region, its transitional frequency $f_{T,\ bulk\text{-}driven}$ can be approximated by

$$f_{T,\ bulk\text{-}driven} \approx \frac{g_{mb}}{2\pi(C_{bs}+C_{ssub})} = \frac{\eta g_m}{2\pi(C_{bs}+C_{ssub})} \tag{2-11}$$

By dividing Equation 2-11 by Equation 2-10, the following relationship can be obtained:

$$f_{T,bulk-driven} = \frac{\eta C_{gs}}{C_{bs}+C_{ssub}} f_{T,gate-driven} \tag{2-12}$$

As discussed in Section 2.3.1 and 2.3.3, η is typically around 0.1 to 0.3 and $(C_{bs}+C_{ssub}) > C_{gs}$. Thus in summary, the speed performance becomes significantly slow with the bulk-driven approach.

2.3.7 Noise

The noise performance also becomes severe with the bulk-driven approach. The channel noise current of a MOSFET $\overline{di^2_{DS}}$ is given by

$$\overline{di^2_{DS}} = 4kT(\frac{2}{3}g_m)df \tag{2-13}$$

where k is the Bolzmann's constant (1.381 x 10^{-23} J/K), T is the temperature in Kelvin, and 2/3 is the coefficient factor for long-channel MOSFET. The equivalent input noise voltage of a gate-driven MOSFET $\overline{dv^2_{ieq\_gate\text{-}driven}}$ can be worked out by dividing Equation (2-13) with g_m^2, which turns out to

$$\overline{dv^2_{ieq\_gate-driven}} = 4kT(\frac{2}{3})\frac{1}{g_m}df \tag{2-14}$$

and the equivalent input noise voltage of a bulk-driven MOSFET $\overline{dv^2_{ieq\_bulk\text{-}driven}}$ can be worked out by dividing Equation (2-13) with $g_{mb}{}^2$,

$$\overline{dv^2_{ieq,bulk-driven}} = 4kT(\frac{2}{3})\frac{g_m}{g^2_{mb}}df = 4kT(\frac{2}{3})\frac{1}{g_m}\frac{1}{\eta^2}df = \frac{1}{\eta^2}\overline{dv^2_{ieq,gate-driven}} \qquad (2\text{-}15)$$

Thus in summary, $\overline{dv^2_{ieq\_bulk\text{-}driven}}$ is $1/\eta^2$ times larger than $\overline{dv^2_{ieq\_gate\text{-}driven}}$.

2.3.8 New Layout Design Techniques

From the layout design viewpoint, bulk-driving a MOSFET brings a new challenge especially when a matched pair of the devices is needed (e.g. for differential pair applications) because the n-well needs to be separated per every device. Consequently, the conventional common-centroid layout technique is not possible for matching. To the author's best knowledge, the layout techniques of a bulk-driven pair have not been reported in publications yet. Hence, the layout designers must develop their own layout techniques with no (or very little) references to achieve precise matching as possible.

2.4 Chapter Conclusion

In this chapter an overview of the bulk-driven approach has been presented. A bulk-driven MOSFET acts like a JFET-like transistor and therefore allows the ICMR to achieve rail-to-rail operation and thus the dynamic range can be expanded under the low supply voltage constraint. However, due to the device physics of CMOS technology, this approach also introduces many drawbacks. Each drawback is thoroughly examined in this chapter.

In order to utilise the bulk-driven approach in CMOS analogue circuit design, novel design techniques need to be developed to overcome those drawbacks.

Chapter 3 Bulk-Driven Differential Pairs

Differential pairs are perhaps mostly widely used two-transistor subcircuits in analogue circuit design [GRA01]. In CMOS analogue circuit design, a differential pair consists of two MOSFETs that are coupled at their sources. Hence a differential pair is also referred as a source-coupled pair [BAK08]. In many literatures, the concept of differential pairs is taught after studying single-ended amplifiers in order to emphasise the high immunity of the signal to noise and interferences [RAZ01], [SAN06], [SED11], [BAK08], [GRA01], [ALL02], [JOH97].

This chapter reports on the author's achievements relating to the development of new circuit design techniques of a bulk-driven differential pair, in order to overcome the drawbacks described in Chapter 2 as much as possible. Two types of a bulk-driven differential pair are proposed in this chapter, which the author has named them as Bulk-Driven Double Replica-Biased (BDDRB) input stage [HAG06] and Bulk-Driven Flipped Voltage Differential Pair (BDFVDP) [HAG10].

A Comment Concerning the Naming Convention – "bulk-driven" or "body-driven"?

It is worth reviewing the publications concerning the invention of a bulk-driven differential pair. According to [YAN00], A. Guzinski *et al* invented a "body-driven" differential pair in 1987 for the Operational Transconductance Amplifier (OTA) design [GUZ87]. In 1991, the invented pair was used in an OTA-C filter of a CMOS telephone circuit in [DIE91]. The original purpose of the invented pair was to yield the small transconductance and to improve linearity. (Interestingly, there are few

circuit blocks where the small transconductance characteristic is appreciated.) Later on, B. Blalock *et al* studied the depletion characteristics of the "bulk-driven" MOSFET and proposed a "bulk-driven" differential pair in an operational amplifier design to achieve rail-to-rail input common-mode range (ICMR) under the supply voltage as low as 1-volt [BLA98].

From this historical background, two different names appeared to describe the same circuit block – "body-driven" and "bulk-driven" differential pair, named by Guzinski *et al* and Blalock *et al*, respectively [BIA99]. In this thesis, the author shall use the same name used by Blalock *et al* throughout, i.e. "bulk-driven", since the research objective was to develop new circuit design techniques that utilise the depletion characteristics of the MOSFET and overcome the drawbacks identified by Blalock *et al* in [BLA98]. In another words, this research work is the further improvement of [BLA98].

A Comment Concerning MOSFET symbol

From this Chapter and on, many transistor-level circuit diagrams are presented. Therefore it is worth taking a moment to comment concerning MOSFET symbols beforehand. In many literatures [RAZ01], [SAN06], [SED11], [BAK08], [GRA01], [ALL02], [JOH97], a MOSFET symbol is simplified to a three-terminal device, since in most circuits the bulk of pMOS and nMOS devices are tied to the positive supply rail (VDD) and the negative supply rail (VSS, or GND if it is the least voltage potential), respectively. The simplified symbols for pMOS and nMOS transistors are depicted in Figure 3-1(a) and (b), respectively. For MOSFET where the bulk connection needs to be explicitly identified, the symbols shown in Figure 3-1(c) and (d) are often used for the pMOS and nMOS transistors, respectively.

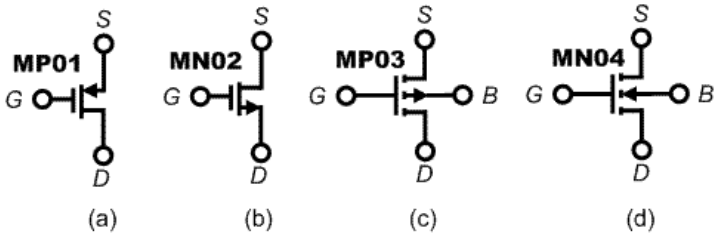


Figure 3-1 MOSFET symbols for (a) pMOS (its bulk tied to VDD and not shown), (b) nMOS (its bulk tied to VSS and not shown), (c) pMOS (its bulk shown explicitly), and (d) nMOS (its bulk shown explicitly)

In this thesis, the symbols shown in Figure 3-1(a) and (b) are used to represent pMOS and nMOS transistors, respectively, and for bulk-driven devices Figure 3-1(c) and (d) are used to represent pMOS and nMOS transistors, respectively. In addition, all transistors are identified as MP and MN in the circuit diagrams to represent the pMOS and nMOS transistors, respectively, so that the readers can easily realise the polarity of the transistors.

3.1 Bulk-Driven Double Replica-Biased Input Stage

3.1.1 Introduction

The primary concern of utilising a bulk-driven device in a differential pair is that its transconductance g_{mb} is dependent to the bulk-to-source voltage V_{BS}. g_{mb} can be expressed by

$$g_{mb} = \frac{g_m \gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} \tag{3-1}$$

where g_m is the transconductance of the gate-driven MOSFET, γ is the body-effect coefficient, and $2|\Phi_F|$ is the Fermi potential. In differential pair applications, it is essential that its effective transconductance $g_{m(eff)}$ is nearly constant over the rail-to-

rail ICMR, as the large variation introduces signal distortion and creates difficulty in the frequency compensation of the multi-stage op-amps [HOG92], [WU94].

So far three proposals are available for improving the $g_m(eff)$ variation of the Bulk-Driven Differential Pair (BDDP) – the complementary BDDP [BLA00], the Replica-Biased Scheme (RBS) [BLA00], and the feedback techniques [BAH00]. The complementary BDDP technique utilizes the complementary behaviour of the pairs to reduce the $g_m(eff)$ variation. However, a special CMOS technology (e.g. a twin-well process) is required for the implementation. The proposed RBS by [BLA00], as illustrated in Figure 3-2, biases the gates of the pair to keep $V_{BS1,2} = 0$ so that the g_{mb} becomes constant. The problem that the authors of [BLA00] identify is, however, it is impossible for the coupled-source voltage V_S to follow over the rail-to-rail input $V_{B1,2}$. Thus the g_m is constant over only a portion of the rail-to-rail ICMR. The feedback technique senses the input common-mode voltage (V_{ICM}) and adjusts the tail current to reduce the g_m variation; however, this causes the Slew Rate (SR) to become V_{ICM} dependent. Typically, a constant-SR of a constant-g_m input stage is desired for consistent large-signal behaviours over the rail-to-rail V_{ICM} [SON08], [CAR03].

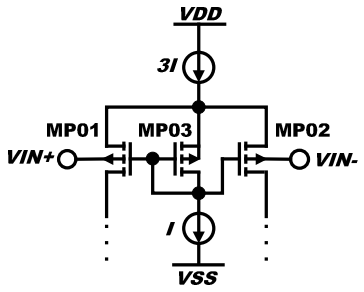


Figure 3-2 The bulk-driven RBS proposed in [BLA00]

This section presents a new bulk-driven rail-to-rail input stage using a standard single-well (n-well in this case) CMOS process. This input stage achieves almost constant-$g_m(eff)$ and constant-SR, working with a wide supply voltage ranging from

sub 1-volt (V_{T0}+3V_{DSsat}) to the maximum allowed by the CMOS process, and also eliminates the latch-up problem.

3.1.2 Proposal

The idea of our bulk-driven input stage comes from utilizing two pairs of the RBS to cover all portions of the rail-to-rail ICMR. Figure 3-3 illustrates the topology of our approach, which we call the Bulk-Driven Double Replica-Biased (BDDRB) input stage [HAG06].

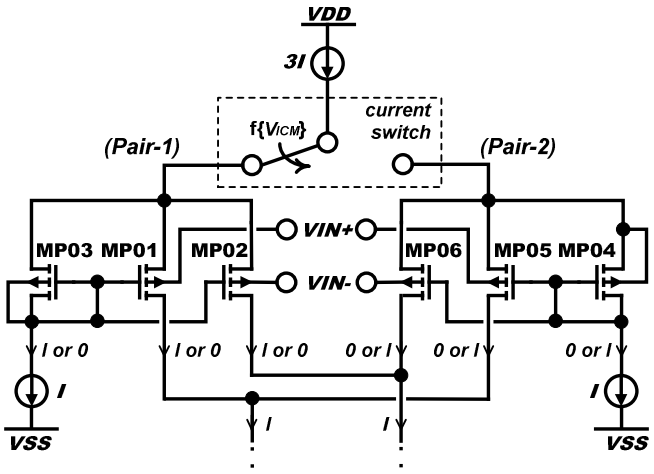


Figure 3-3 Topology of the BDDRB input stage

The BDDRB input stage consists of pair-1 (MP01~MP03) and pair-2 (MP04~MP06), which are assigned for the low and high portions of the ICMR, respectively, and a current switch.

The device sizes of pair-1 are all the same, and the same dc current runs through each device when the pair is selected. This leads MP03 to be the replica of the input pair, and $V_{BS1,2}$ to be equal to V_{GS3} (= constant). The same argument goes to pair-2 except that $V_{BS5,6}$ would be zero instead. The pair-1 would be operational for the ICMR between VDD-V_{SDsat}-V_{SG3} and VSS+V_{DSsat}, and for pair-2 the operational range would

be between $VDD\text{-}V_{SDsat}$ and $VSS\text{+}V_{DSsat}\text{+}V_{SG4}$. To maximize the ICMR a current switch is implemented so that the effective ICMR would be between $VDD\text{-}V_{SDsat}$ and $VSS\text{+}V_{DSsat}$.

Operation Principle

Figure 3-4(a) illustrates how the BDDRB input stage can be realized as a transistor circuit. Again, MP01~MP03 (pair-1) and MP04~MP06 (pair-2) are the replica-biased input pairs for the low and high portions of the ICMR, respectively. MP09~MN12 form a current switch and work as a function of V_{ICM}. This input stage is configured such that it normally operates with pair-1. When V_{ICM} becomes high and causes V_{SG9} to be greater than the threshold voltage ($|V_{T0}|$), the switch deactivates pair-1 and activates pair-2 instead. Conversely, when V_{ICM} becomes low and causes $V_{SG9} < |V_{T0}|$, pair-1 turn on and pair-2 turns off. The bias-voltage, V_{SWITCH}, controls the crossover voltage between the two points.

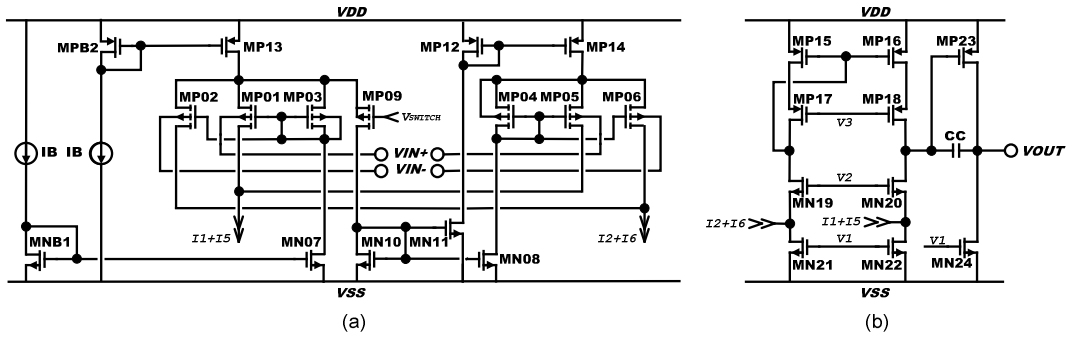


Figure 3-4 An application example of the BDDRB input stage in a folded-cascode two-stage op-amps (a) the BDDRB input stage, and (b) a folded-cascode two-stage op-amps

To verify the operation of the BDDRB input stage, it was necessary to implement it in an op-amp. For this we chose a folded-cascode two-stage op-amp, as illustrated in Figure 3-4(b), to present as an application example.

3.1.3 Simulation Results

Using the BSIM3 MOSFET models of a 0.18μm CMOS process, the op-amp of Figure 3-4 has been simulated in the typical mode with a supply voltage of 0.8-volt and a load resistance and capacitance of 1MΩ and 5pF, respectively. Table 3-1 shows the summary of the simulation results.

Table 3-1 Simulation Results of the Overall Performance of the Proposed Op-amp in Figure 3-3

Characteristics	**Simulated Results**
Open-loop DC gain	60dB
Unity-gain frequency	0.6MHz
Phase margin	58°
ICMR	0.6V
Total current consumption	61~74μA (V_{ICM} dependent)
SR	SR+ = 1.0V/μs, SR- = -0.5V/μs
Output voltage swing	0.6V
Common-mode rejection ratio	63dB
Power Supply Rejection Ratio (PSRR)	PSRR+ = 58dB, PSRR- = 79dB
Input referred noise voltage	160nV/√Hz (white noise only)
Total harmonic distortion, A_{VCL}=+1V/V	0.014% (-77.1dB) for 0.6Vp-p, 1kHz sine wave 0.093% (-60.6dB) for 0.6Vp-p, 10kHz sine wave
Setup: *VDD* = 0.8V, *VSS* = 0V, *Vswitch* = *VDD* - 0.5V, C_L = 5pF, R_L=1MΩ	

The simulation confirmed the rail-to-rail ICMR operation (VDD-$V_{SDsat14}$ to VSS+$V_{Dssat07}$ precisely). Figure 3-5 and Figure 3-6(a) show the simulation results of the open-loop gain frequency response and the effective tail current of the op-amp in Figure 3-4, which indicate that both characteristics are nearly V_{ICM} independent. Figure 3-6(b) gives the simulation results of $g_{m(eff)}$ of the op-amp versus V_{ICM}.

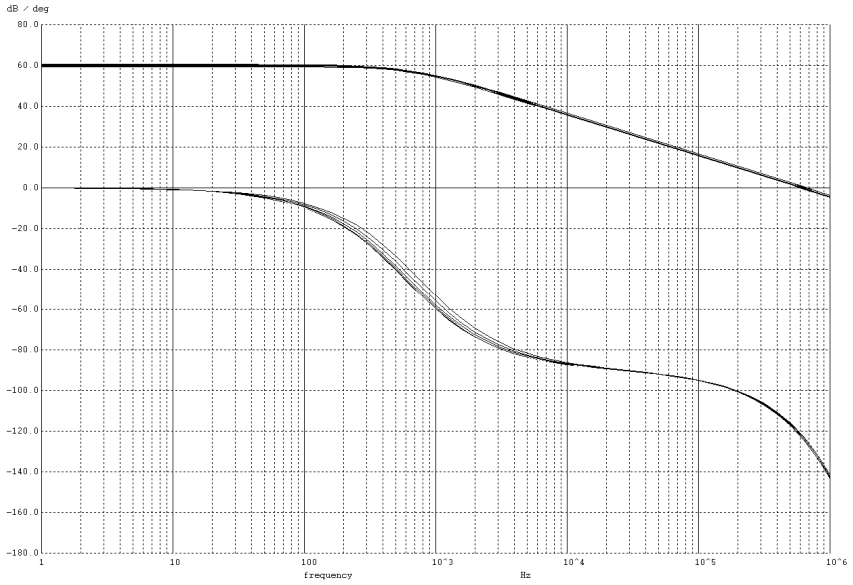
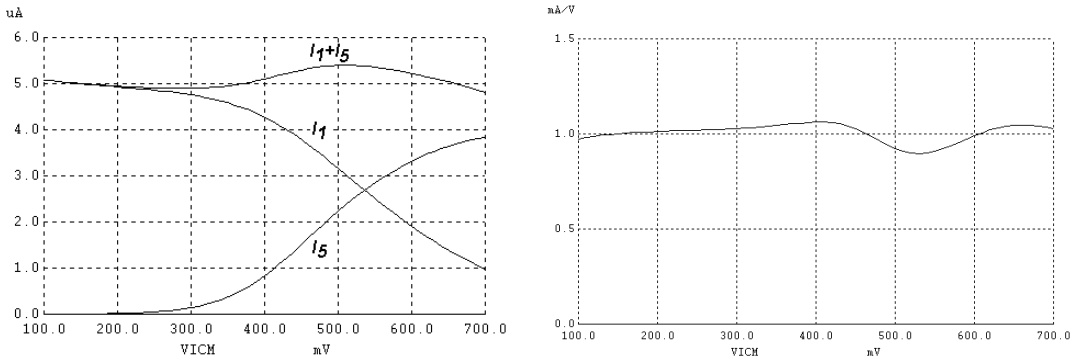


Figure 3-5 Simulated frequency response of the op-amps for V_{ICM} varying from 0.1 to 0.7V with a 0.1V step



(a) (b)

Figure 3-6 Simulated plots for (a) tail current versus V_{ICM} and (b) $g_m(eff)$ versus V_{ICM}

Figure 3-6(b) indicates that the g_m variation is approximately 10% over the rail-to-rail ICMR operation. This variation peaks at the transition point between the two pairs, i.e. when the pairs are partially on and off. It is worth noting that the source-to-bulk voltage of the input pairs (V_{SB1} and V_{SB5}) changes at the transition stage, which should also have created a major impact in the g_m variation according to [HOG92]. Figure 3-7 shows the simulation results of V_{SB1} and V_{SB5} versus V_{ICM}.

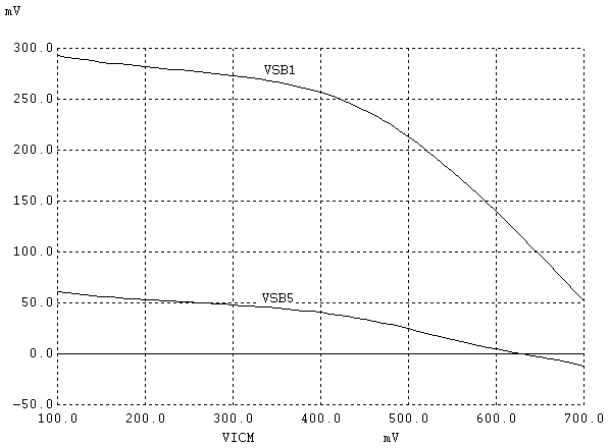


Figure 3-7 Simulated V_{SB1} and V_{SB5} versus V_{ICM}

Advantages and Disadvantages

An important practical advantage of the BDDRP input stage is that it requires no special CMOS process. Other advantages are $g_m(eff)$ and SR of the op-amp remain relatively constant with respect to V_{ICM}, and the circuit is immune from latch-up. Conventional BDDP techniques require very low supply voltage [BLA98], otherwise the rail-to-rail ICMR operation would cause the bulk terminals to be strongly forward-biased. With the BDDRB input stage, the bulk-to-source voltages remain as the same condition as the replica device regardless of the supply voltage condition. For confirmation, we simulated the circuit of Figure 3-4 with a 3-volt power supply and observed that the rail-to-rail ICMR operations did not result an increase in the supply current consumption.

However, the rest of the disadvantages of a bulk-driven MOSFET remain unchanged. The g_{mbs} is low (resulting relatively low gain-bandwidth products and poor noise performance), and also the conventional layout matching techniques cannot be applied because of the circuit structure.

The input impedance is also known to be another disadvantage of a bulk-driven MOSFET. However, this is controllable by circuit designers as it is directly related to its source-to-bulk voltage. Reducing the forward-bias of the bulk-terminal results in increased input resistance and decreased source-to-bulk and source-to-drain capacitances (C_{sb} and C_{sd}). With the BDDRB input stage, this can be easily achieved by decreasing the source-to-bulk voltage of the replica device (V_{SB3} of Figure 3-4(a), which is equivalent to V_{SG3}). Figure 3-8 illustrates the simulation results of the input impedance measurements for the op-amp in Figure 3-4.

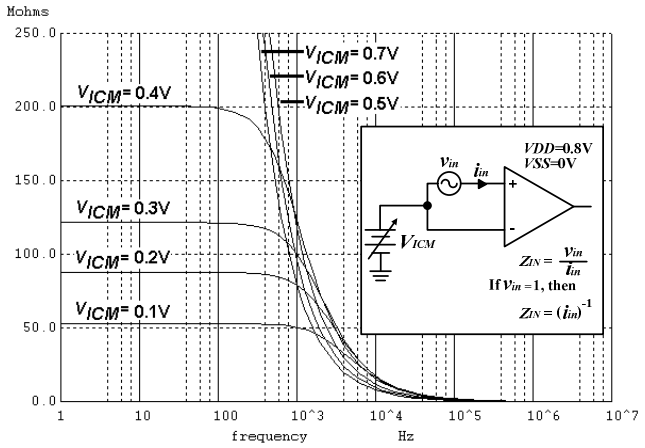


Figure 3-8 Simulation results of the circuit-level input impedance characteristic

3.1.4 Section Conclusion

In this section a new approach for the bulk-driven input stage called BDDRP to achieve rail-to-rail ICMR operation has been presented. This approach leads the operational supply voltage to be from under 1-volt to the maximum allowed by the CMOS process used, as well as completely removing the latch-up problem. SPICE simulations indicate that $g_{m(eff)}$ is nearly constant (within 10%) over the entire ICMR whilst the effective tail current remains almost unchanged. The additional hardware implemented to achieve this performance is only a replica circuit for each pairs and a current switch.

3.2 Bulk-Driven Flipped Voltage Differential Pair

3.2.1 Introduction

The BDDRP proposed in the previous section consists of a novel circuit design technique that can efficiently overcome the non-linearity and the latch up problems, however it still does not solve the issue of the degraded input impedance characteristics of a bulk-driven MOSFET, in particular the increased input capacitance caused by the diffusion capacitance and the well-to-substrate capacitance as described in Chapter 2.

This section reports the author's achieved work on development of a new circuit design technique that can particularly solve the issue of the degraded input impedance of a BDDP.

3.2.2 Design Approach

Low-Power Differential Pair

In prior to developing a new BDDP, at first the author reviewed previous works of a differential pair that achieves low-power high-performance, and drew an attention to a novel circuit block called Flipped Voltage Follower Pseudo Differential Pair (FVFDP) which was proposed by Carvajal *et al* in [CAR05]. Figure 3-9(a) and (b) illustrates the transistor realization of the FVFDP, and the simulated plot with I_B set to 1μA using a 0.35μm CMOS process.

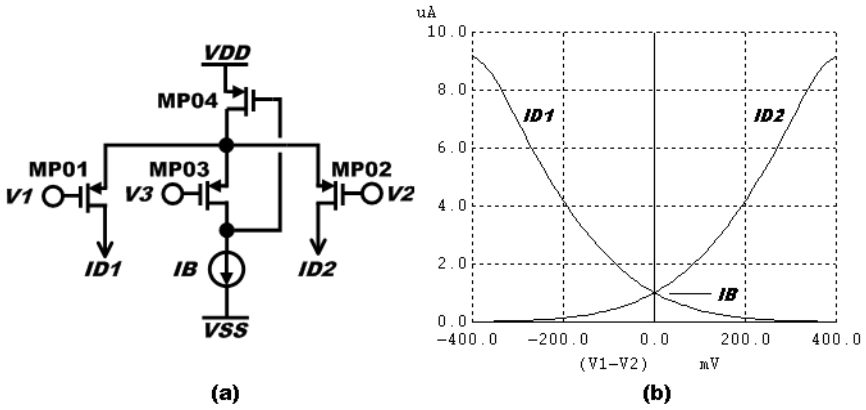


Figure 3-9 (a) (pMOS) FVFDP proposed in [CAR05], and (b) simulating the DC transfer characteristics using a 0.35µm CMOS process

In Figure 3-9(a), V_1 and V_2 are the differential input, and V_3 is the common-mode voltage of V_1 and V_2, i.e. $(V_1+V_2)/2$. As can be observed from Figure 3-9(b), when no differential signal is applied (i.e. $V_1=V_2=V_3$, steady condition) the drain current of MP01 and MP02 (I_{D1} and I_{D2}) become equal to I_B, and when the differential signals are applied then I_{D1} and I_{D2} can become much larger than the twice of I_B. This low-static high-dynamic power performance is not possible to achieve with a conventional differential pair.

For the development of the new BDDP design, the author selected the FVFDP as the base. This section reports a new circuit design technique that bulk-drives the FVFDP so that rail-to-rail low-power high-driving performances can be all achieved, but without facing the issue of the degraded input impedance characteristics caused by the bulk-driven MOSFET.

A Bulk-Driven MOSFET with the Reverse-Biased Diode

In order to avoid the issue of the degraded input impedance characteristics of a bulk-driven MOSFET, the author came up with an idea of utilising a reverse-biased diode. Figure 3-10(a) and (b) illustrate the circuit diagram of a bulk-driven pMOS device

connected with the reverse-biased diode, and a sketch of a diode realized in CMOS technology, respectively.

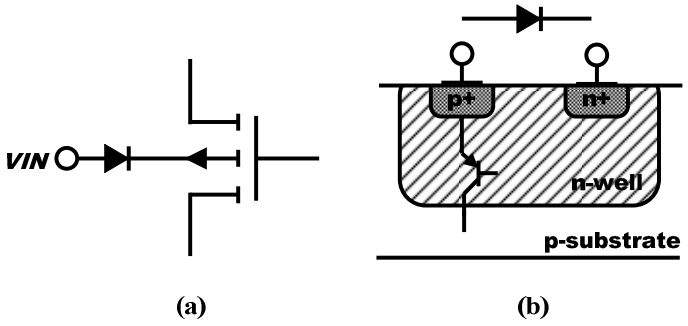


Figure 3-10 (a) a bulk-driven pMOS device with the reversed-biased diode, and (b) a diode realised in CMOS technology

Figure 3-11 shows the simulated plot of the DC sweep analysis of Figure 3-10(a) using a 0.35 μm CMOS process, where the transistor width and length are 2μm and 1.4μm, and source, drain, and gate voltages of the pMOS device are fixed at 0V, -0.2V, and -0.8V, respectively. For the diode the minimum size is used. As can be observed from the plot, only a few pico-ampere of the DC input current I_{IN} flows at any operation point of the input voltage V_{IN}, since the body-diode of the pMOS and the added diode are in reversely connected to each other and thus only the leakage current passes through. Consequently, the source-to-bulk voltage V_{SB} of the PMOS does not become strongly forward-biased since the forward current of the diode is extremely small. It is worth noting that the added diode does not become strongly forward-biased either, so that the parasitic vertical bipolar illustrated in Figure 2(b) remains off.

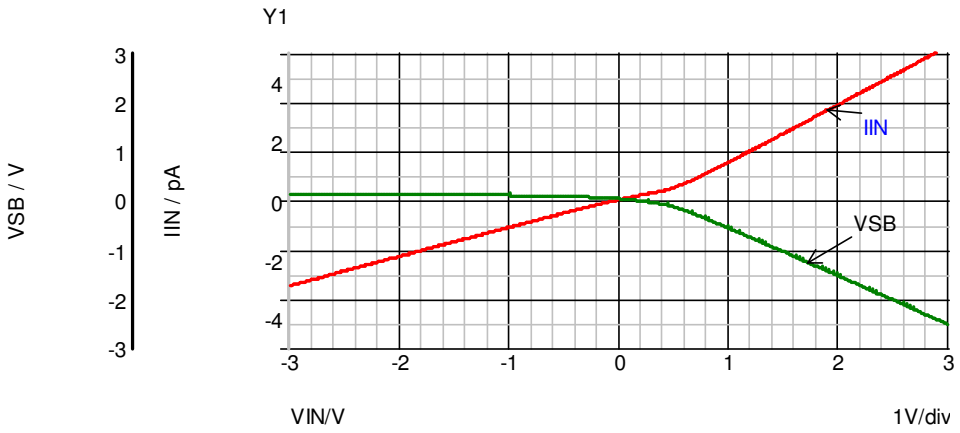


Figure 3-11 Simulated I_{IN} and V_{SB} of Figure 2(a)

Interestingly, with Figure 3-10(a) the input at V_{IN} is fed into p+ implant, whereas it would have been n+ implant for a conventional bulk-driven MOSFET. This means that V_{IN} indirectly sees the pn-junction (from n-well to p-substrate), and thus the effective input capacitance can be significantly reduced.

In results the input resistance and capacitance can both be drastically improved with this approach, the author further worked on with this approach to come up with a new proposal of BDDP design, which is described in the next subsection.

3.2.3 Proposal

Based on the analysis shown in the previous section, the author proposes a rail-to-rail low-power operational amplifier (op-amp) using a new design technique which we named as Bulk-Driven Flipped Voltage Differential Pair (BDFVDP). Figure 3-12 illustrates the circuit diagram of the proposal.

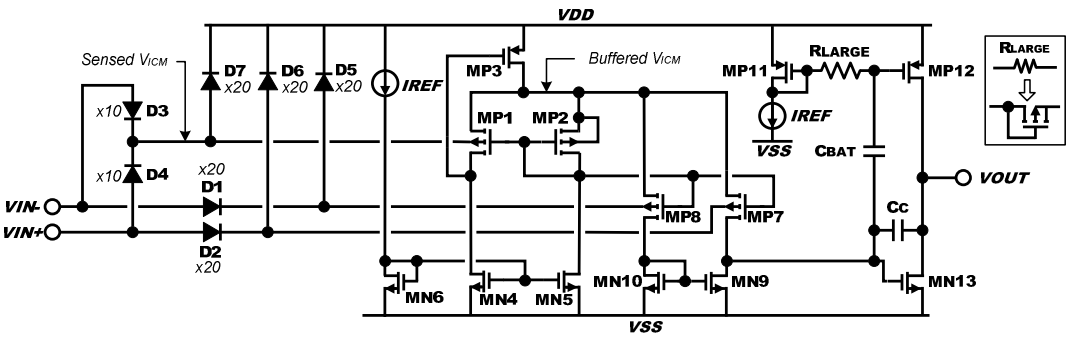


Figure 3-12 Proposed CMOS buffer using Bulk-Driven Flipped Voltage Differential Pair

The operation principle of the circuit in Figure 3-12 is simple to follow. From MP1 to MN5 form a circuit block called Bulk-Driven Flipped Voltage Follower (BDFVF) [HAG09]. MP1 and MP2 are equally sized and biased with identical drain current with MN4 and MN5. Since the bulk-terminal of MP2 is physically shorted to the coupled source node (i.e. V_{SB2}=0), MP1 becomes the replica of MP2, and hence the source-to-bulk voltage of MP1 becomes virtually shorted (i.e. V_{SB1}≈0). In another words, the coupled source voltage follows the bulk input voltage of MP1. If MP3 is sized wide enough such that it is in linear region, then the coupled source node becomes low impedance and hence it becomes the buffered signal of the bulk input of MP1. In the design of the proposed op-amp, BDFVF is utilized to buffer the common-mode signal of the differential input V_{ICM}.

From MP7 to MN10 forms the first stage of the operational amplifier. The input devices of this stage are bulk-driven, and when the differential signals V_{IN+} and V_{IN-} are identical then the drain current of the input devices, I_{D7} and I_{D8}, settle to the bias current I_{REF}. When large differential signals are applied, then i_{D7} and i_{D8} can become much greater than twice the current of I_{REF}, since the coupled source node has very low impedance and MP3 can supply a source current that is bigger than 2 x I_{REF}.

From MP11 to MN13 forms the second stage of the operational amplifier, which has been converted to class-AB operation using the Quasi-Floating Gate (QFG) technique [LOP09]. As can be observed, the gate of MP12 is connected to the gate of MP11 with a large resistor R_{LARGE}, and also to the gate of MN9 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow through R_{LARGE} and therefore the gate voltage of MP12 and MP11 are the same, and thus the static drain current I_{D12} is I_{REF}. In terms of AC characteristics, a high pass filter is formed at the gate of MP12 with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, and therefore MP12 achieves not only static but also dynamic operation, which in turn leads to class-AB operation. It is remarkable to realize that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, thus a low cutoff frequency can be achieved with a moderately small capacitance of C_{BAT}.

From D1 to D4 are the reverse-biased diodes to the bulk-driven devices. D3 and D4 are used to detect for V_{ICM}. In Figure 3, those diodes have been sized to 20 times of the minimum size of the diode for D1 and D2, and 10 times for D3 and D4, to prevent from further reduction of the transconductance as possible. The transconductance of a bulk-driven MOSFET with the reverse-biased diode g_{mb_VR} can be expressed as:

$$g_{mb\_VR} = \alpha\, g_{mb} \tag{3-2}$$

where α is the attenuation factor of the signal and g_{mb} is the transconductance of the bulk-driven MOSFET. α can be expressed as:

$$\alpha = C_{diode} / (C_{diode}+C_{db}) \tag{3-3}$$

where C_{diode} is the junction capacitance of the reverse-biased diode, and C_{SB} is the source-to-bulk capacitance of the MOSFET. C_{diode} given by

$$C_{diode} = C_{j0\_diode} / (1+V_R/V_0)^{0.5} \tag{3-4}$$

where C_{j0_diode} is the zero-biased junction capacitance of the reverse-biased diode, V_R is the reversed-biased DC voltage, and V_0 is the built-in bulk junction potential. Similarly,

$$C_{sb} = C_{jo\_mosfet} / (1+V_{SB}/V_0)^{0.5} \quad (3\text{-}5)$$

where C_{jo_mosfet} is the zero-biased junction capacitance of the MOSFET, and V_{SB} is the source-to-bulk DC voltage.

3.2.4 Simulated Results

To verify the proposed solution of Figure 3-12, we designed it using a 0.35um CMOS process to operate with a 1.8V supply voltage. This section provides simulated results using the BSIM3 MOSFET models.

DC-Sweep Analysis

This subsection provides the simulation results of the DC-sweep analysis. Figure 3-12 has been setup in a unity-gain configuration with a 1.8V supply voltage, and the input voltage V_{IN} is swept from rail to rail. Figure 3-13 shows the simulated behaviour of the source-to-bulk voltage of the bulk-driven device MP7 V_{SB7} and the potential difference between the output V_{OUT} and V_{IN}.

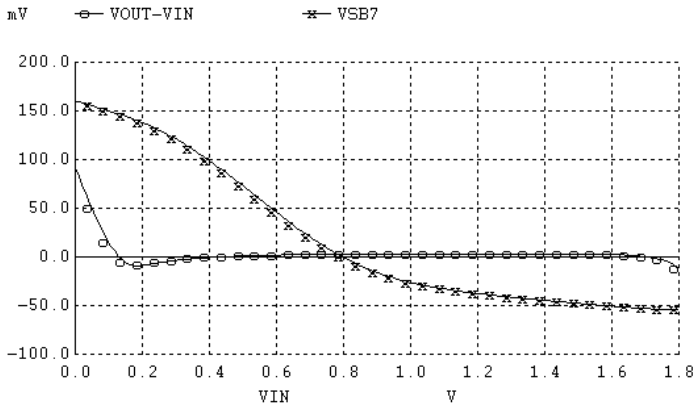


Figure 3-13 Simulated V_{OUT}-V_{IN} and V_{SB7} of Figure 3-12 in unity-gain configuration

As can be noticed from Figure 3-13, V_{SB7} does not become strongly forward biased which indicates that latch up does not occur, and $V_{OUT} - V_{IN}$ remains small which confirms that the proposed buffer is operational in rail-to-rail.

Figure 3-14 is the simulated plot of the input DC current I_{IN} of the same setup. It indicates that only ±30pA of DC current flows from rail to rail, suggesting that the input resistance would be as large as 30GΩ. This superior result is expected since the diodes are connected in reverse-bias to the body-diode of the MOSFET.

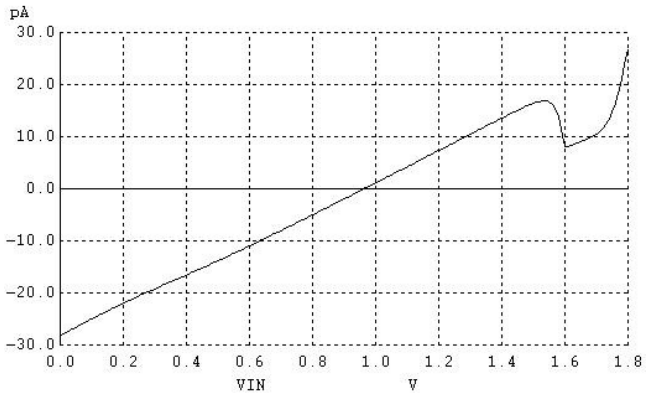


Figure 3-14 Simulated I_{IN} of Figure 3-12 in unity-gain configuration

Transient Analysis

This subsection provides the simulation results of the transient analysis. Figure 3-12 has been setup in a unity-gain configuration with a 1.8V supply voltage and a capacitive load of 5pF, and a step input from 0.2V to 1.6V and vise versa is applied. Figure 3-15 is the simulated plot of the input voltage v_{IN}, the output slew rate v_{OUT}, and the transient behavior of the source-to-bulk voltage of the bulk-driven device MP7, v_{SB7}. The key observation of Figure 3-15 is the v_{SB7} behavior when a large step-down input is applied. Appreciating to the protection capability of the diodes from D5

to D7, v_{SB7} does not even instantaneously become forward biased by more than 0.3V and therefore the latch up problem has been prevented.

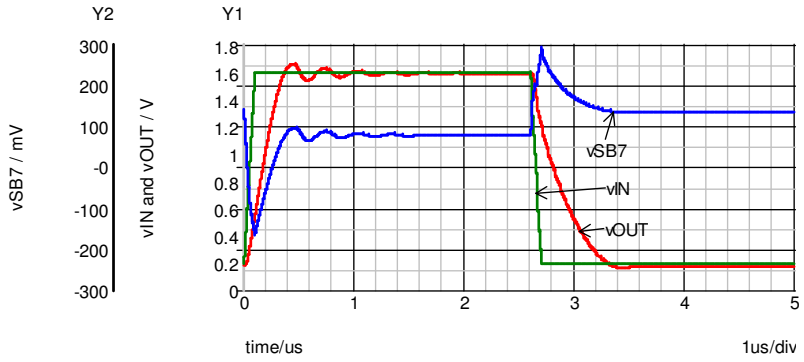


Figure 3-15 Simulated v_{SB7} and slew rate of v_{out} of Figure 3-12 in unity-gain configuration with CL=5pF (v_{IN} stepping between 0.2V and 1.6V)

Figure 3-16 is the simulated transient analysis plot of the input and output instantaneous current, i_{IN} and i_{OUT}, indicating that i_{IN} never achieves more than 1µA and i_{OUT} current reaches over 20µA. This suggests that the i_{IN} would always be in the nano-ampere range for an AC input slower than the Gain-Bandwidth (GBW), which proves the effectiveness of the Figure 3-12. This low i_{IN} has been achieved because the well-to-substrate capacitance is indirectly seen by the input and also the effective input capacitance has been lowered by the attenuation factor α.

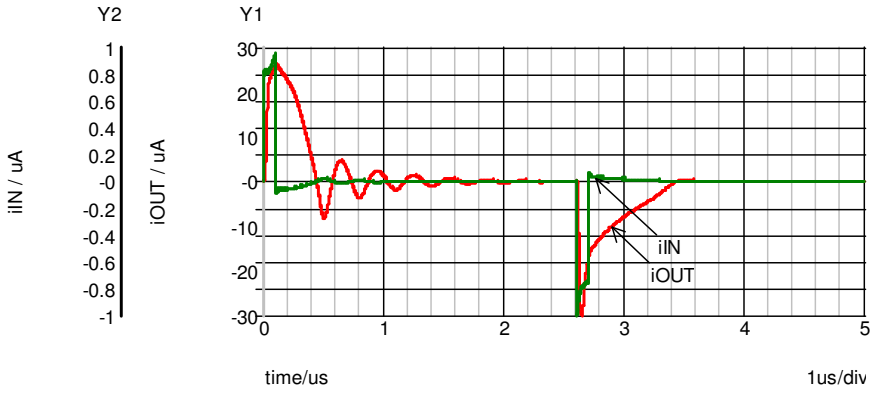


Figure 3-16 Simulated i_{IN} and i_{OUT} of Figure 4 in unity-gain configuration with CL=5pF (v_{IN} stepping between 0.2V and 1.6V)

Observation

To further observe our proposal of Figure 3-12, we designed another CMOS buffer as shown in Figure 3-17 for comparison purposes. This circuit block is the gate-driven type of Figure 3-12, and all transistors are sized identically. Table 3-2 shows the summary of the overall performance of the two circuit blocks.

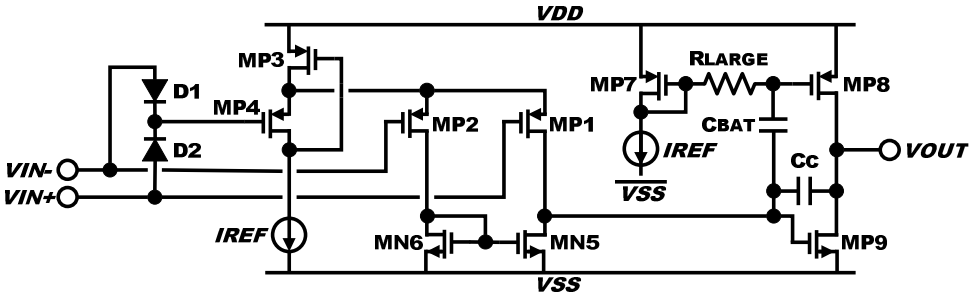


Figure 3-17 Gate-driven Flipped Voltage Differential Pair

Table 3-2 Simulated Results of the Overall Performance

Parameter		Simulated results	
		Figure 3-17	**Figure 3-12**
Open-loop gain A_{OL}		60dB	50dB
Gain bandwidth (GBW) at CL=5pF		9MHz	3MHz
Total static current consumption *ICC*		7μA	9μA
Slew Rate (SR) at CL=5pF		SR+=5.2V/μs SR-=7V/μs	SR+=5.2V/μs SR-=2.3V/μs
Input referred noise			
V_{IN}=*VDD*	1/f @1kHz	MP1& MP2 in cut off	11μV/√Hz
	Wideband	70μV/√Hz	600nV/√Hz
V_{IN}=0.9V	1/f @1kHz	9μV/√Hz	15μV/√Hz
	Wideband	600nV/√Hz	600nV/√Hz
V_{IN}=*VSS*	1/f @1kHz	1.5μV/√Hz	22μV/√Hz
	Wideband	100nV/√Hz	600nV/√Hz
Total Harmonic Distortion (A_{CL}=1, 1.4Vpp sinewave)			
	CL=5pF @100kHz	1.4Vpp	-40dB
	CL=10pF @100kHz	Operation not	-33dB
	CL=5pF @200kHz	achievable	-33dB
	CL=5pF @300kHz		-27dB
Unless stated, the set up condition is: *VDD*=1.8V, *VSS*=0V, V_{IN}=0.9V, C_L=5pF			

As expected, the open-loop gain A_{OL} and the GBW of the bulk-driven one is smaller and slower in comparison to the gate-driven one due to reduced transconductance of the input device, however A_{OL}=50dB GBW (at CL=5pF) = 3MHz is relatively efficient for the total static current consumption of only 9μA. It is important to realize that the input referred noise of Figure 3-12 is moderately independent to the input condition since no transistors change the operation region. This property suggests that the single-pair approach is worthy of further improving than the double-pair approach which changes the operation region.

On the other hand, there is a significant drawback with the proposal that the A_{OL} is not constant to V_{ICM}, where the dominant root cause is that α in Equation (3-2) varies significantly with the reverse voltage of the diode.

3.2.5 Section Conclusion

In this section a new low power consumption high-speed op-amp has been proposed. The new circuit block consists of a FVFDP and a QFG type of class-AB second stage, which delivers high-speed at 3MHz GBW operation for a 5pF load whilst maintaining the static current consumption as small as 9μA. This paper also addresses the latch up problem by having reverse-bias connected diodes to the body diode of the bulk-driven MOSFET, so that only the diode's leakage current flows and forward biasing of the diodes can be prevented.

3.3 Chapter Conclusion

In this chapter two types of new BDDP, called BDDRB and BDFVDP, have been proposed. The BDDRB input stage uses the RBS so that the effective transconductance becomes almost constant over the entire ICMR and hence solves the non-linearity and latch up issues. On the other hand, with the BDFVDP low-power high-speed operation can be achieved with the use of FVFDP and QFG techniques, and also solves the issue of degraded input impedance characteristics by utilising the reverse-bias connected diodes. For both BDDRB and BDFVDP, the hardware implementation is simple.

From this work, it is evident that circuit designers can contribute to solving many of the device physics limitations of a bulk-driven MOSFET described in Chapter 2. At least, the non-linearity and latch up issues can be solved by controlling the DC voltage across the bulk and the source of the MOSFET, and the degraded input capacitance concern can become less affected by indirectly applying the signal to the bulk (e.g. with a diode). With the use of novel circuit design techniques that were previously proposed by other authors, for instance FVFDP and QFG techniques, low-power high-speed performances can be achieved too.

Chapter 4 Bulk-Driven Source Followers

Source followers are one of the fundamental circuit blocks that are introduced by many literatures of analogue IC design [RAZ01], [SAN06], [SED11], [BAK08], [GRA01], [ALL02], [JOH97]. In most cases they are discussed in the section of single stage amplifier design, and sometimes they are referred with different names, such as common drain amplifiers, voltage buffers, or voltage followers. These circuit blocks are particularly applied for DC level shifting purposes, for instance, at the input stage of operational amplifiers to achieve rail-to-rail operation [CAR03], [SHE09], [HAG08], and in current mirrors to reduce the voltage headroom consumption of the input device [RAM94]. Other types of applications include sensing the common-mode signal of fully differential amplifiers [BAN88], and cutting off the unwanted feed-forward path of the compensation circuits in multi-stage amplifiers [TSI76]. There is even a recent study which provides the high-frequency harmonic distortion analysis of source followers using a large-signal model, in order to derive an optimisation design technique for wide-bandwidth low-distortion operation [FAN05]. As its applications are very wide, there are many journals and conference papers published today relating to this field.

This chapter reports the achievement of the author's research work relating to source followers. In many conventional design techniques, cascaded complementary source followers (i.e. shift-up and -down level shifters being cascaded) are often utilised in order to eliminate the DC level shift [FAN05]. This chapter demonstrates that the bulk-driven approach leads to constructing the source followers with much simpler

hardware, and allows the DC level shift not only to be eliminated but even programmable.

From the next section, new circuit blocks which the author has given the names as bulk-driven flipped voltage follower, bulk-driven super source follower, and bulk-driven DC level shifter are proposed and thoroughly discussed.

4.1 Bulk-Driven Flipped Voltage Follower

4.1.1 Introduction

Source followers are often used as voltage buffers, which play an essential role in driving large capacitive loads at high speeds. The ideal performance of a voltage buffer is not only to drive the large load as fast as possible but also with minimal power consumption, which means that the buffer needs to have high slew rate and low static power consumption. Furthermore the input capacitance of the buffer would also need to be as small as possible so that the weak signal input is not affected under any circumstances. Today, it is evident that the Flipped Voltage Follower (FVF) proposed by Carvajal *et al* in [CAR05] is one of the closest to the ideal voltage buffer, as many recent proposals are utilizations and/or modifications of the FVF [PAD06], [PAD07], [MAN08], [RAM06].

Recently, the new version of the class-AB FVF that is free from the DC level-shift has been proposed by Ramirez-Angulo *et al* [RAM06]. This section proposes a much simpler technique which can eliminate the DC level shift and convert into class AB

operation, whilst preserving the advantages of the FVF approach – low-power consumption with high-power drive.

4.1.2 Previous Essential Works

This section covers a brief review of voltage followers and the bulk-driven MOSFETs used in a differential pair, which have been utilized to form the essential part of the proposal.

Voltage Followers

Figure 4-1 illustrates two types of voltage followers. Figure 4-1(a) is the conventional type of a voltage follower. The input device MP01 is biased with the drain current of *IREF*, therefore the gate-to-source voltage $V_{GS\,\mathrm{MP01}}$ becomes constant if the body-effect is neglected, and therefore the output voltage V_{OUT} is equal to V_{IN} + $V_{GS\,\mathrm{MP01}}$. Figure 4-1(b) illustrates the FVF, in which V_{OUT} is also shifted up by $V_{GS\,\mathrm{MP01}}$ from V_{IN}, however, in contrast to Figure 4-1(a), the beauty of the FVF is that it has current sourcing and sinking capabilities at the output, which can lead to delivering both high-power driving as well as low-power consumption simultaneously.

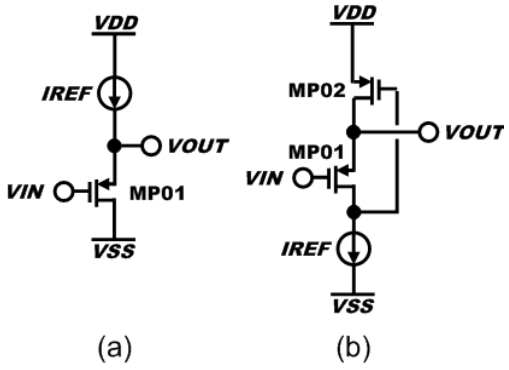


Figure 4-1 Voltage followers (a) common-drain amplifier (voltage follower) and (b) FVF proposed in [CAR05]

Bulk-driven MOSFETs used in differential pairs

In low-voltage rail-to-rail operational amplifier designs, there exists a design technique called the bulk-driven approach. The traditional design technique for rail-to-rail operational amplifiers is the deployment of complementary differential pairs with the tail current being controlled with current switches to keep the transconductance g_m constant [HOG92]. However, due to the fact that the mobility ratio of the complementary pairs (μ_n/μ_p) is process and temperature dependent, causing the g_m variation to deviate by approximately 12% [CAR03], there exist circuit topologies which use only a single type of the differential pair, where one of them is the bulk-driven one. Figure 4-2(a) illustrates a bulk-driven differential pair that uses p-type devices only.

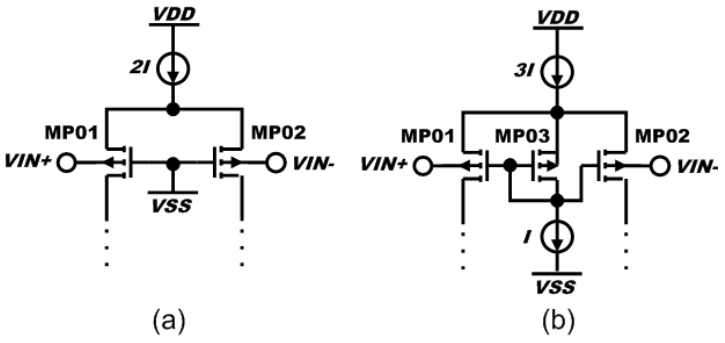


Figure 4-2 Bulk-driven differential pair (a) pMOS input pair and (b) the replica-biased scheme proposed in [BLA00]

The primary problem of Figure 4-2(a), however, is that the transconductance of a bulk-driven MOSFET g_{mb} is dependent on the bulk-to-source voltage V_{BS}. The level-1 model of the g_{mb} is given by:

$$g_{mb} = \gamma\,(2\beta I_{DS})^{0.5} / 2\,(2|\Phi_F| - V_{BS})^{0.5} \qquad (4\text{-}1)$$

where γ is the bulk-threshold parameter, β is the small-signal transconductance parameter, I_{DS} is the drain current, and $2|\Phi_F|$ is the surface potential.

To overcome the concern of g_{mb} dependency over the V_{BS}, Blalock *et al* [BLA00] proposed the Replica-Biased Scheme (RBS) as illustrated in Figure 4-2(b). The pMOS device identified as MP03 is the replica device biasing the gates of the pair. Since the bulk of MP03 is shorted with its source, the V_{BS} of the pair is kept at zero.

The author has noted the advantage from Blalock's approach namely that the condition of $V_{BS} = 0$ is kept constant, meaning $V_B = V_S$, and chose to apply this to the FVF illustrated in Figure 4-1(b) to remove the DC level shift.

4.1.3 Proposal

Figure 4-3 illustrates the proposal of the modified FVF, which the author has named as "Bulk-Driven Flipped Voltage Follower (BDFVF)". As mentioned previously this is the FVF for which the input device has been modified to a bulk-driven MOSFET biased by the replica circuit to eliminate DC level shift.

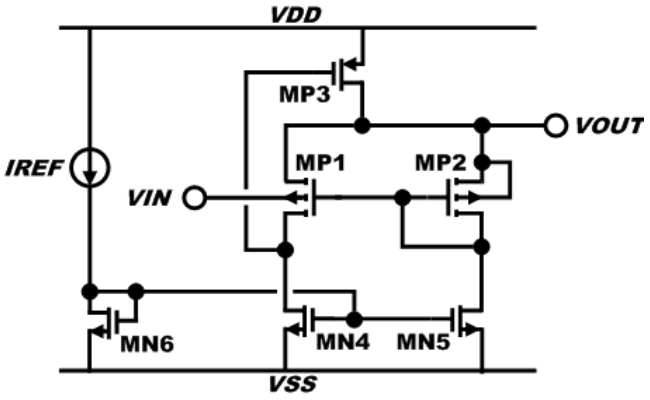


Figure 4-3 Bulk-driven flipped voltage follower (class-A)

The operation principle of the BDFVF of Figure 4-3 is very simple to follow. MP1, MP3, and MN4 form the FVF. MP1 is the input device, which its bulk is utilized to feed the input. MP2 and MN5 are the replica devices for MP1 and MN4 respectively.

Note that the bulk of MP2 is physically shorted to its source, which is the output node. Since the gate of MP1 is biased with the diode-connected MP2, as well as the drain current of MP1 and MP2 are equally set to *IREF*, V_B and V_S of MP1 becomes virtually shorted (i.e. $V_{BS\text{MP1}} = 0$), and in effect the output voltage V_{OUT} becomes equal to V_{IN}.

The proposal of Figure 4-3 works well, however since it is class-A type, there is a limitation in its sink capability to 2*IREF*, which leads to poor pull capability in driving large loads at high speed. To overcome this problem, the circuit of Figure 4-3 can be modified to class-AB type as shown in Figure 4-4.

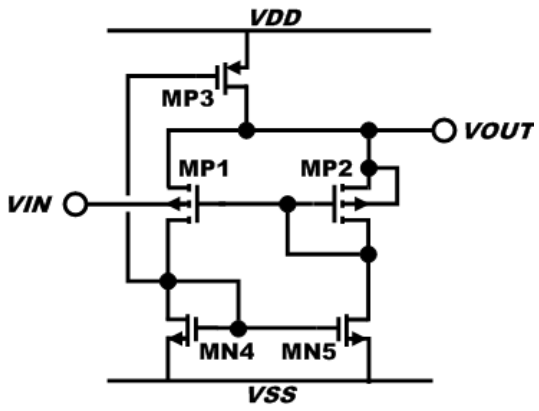


Figure 4-4 Proposed class-AB bulk-driven flipped voltage follower

The difference of Figure 4-4 from Figure 4-3 is that only MN4 has been modified to diode-connected instead of the constant bias to *IREF*. In this way, MP1 and MP2 can also have the same drain current and hence the replica-biased scheme remains valid. This simple change has led to significant improvement in the sink capability of the output without the need of widening MN4 or MN5 or increasing *IREF*. In the next section, simulation results are provided.

4.1.4 Simulated Results

A. Overall Performance

Using the BSIM3 MOSFET models of a 0.35μm CMOS process, the BDFVF of Figure 4-4 is verified by simulation. Table 4-1 shows the simulation results summarising the overall performance.

Table 4-1 Simulation Results of the Overall Performance of the Class AB DBFVF Circuit of Figure 4-4

Parameter	**Simulated results**
3dB frequency	2.8MHz
Total current consumption (when IL=0)	2.5μA
Slew rate (VDD=2V, VSS=0V, CL=10pF, VIN=1V↔2V)	1.9V/μs
PSRR+ / PSRR-	41.7dB / 42.0dB (dc to 100kHz)
1/*f* noise at 1kHz	880nV/√Hz
THD (Vpp=0.8V VDD=1.5V, VSS=0V, CL=10pF)	0.0747% when f=1kHz 0.0794% when f=100kHz 0.501% when f=500kHz
Input voltage range (VDD=2V, VSS=0V)	1V to 2V for offset ≤ 10mV
Load regulation	±15μA for offset ≤ 10mV
Input current	1.5pA
Input capacitance	9.3fF
Unless stated, the set up condition is: VDD=1.2V, VSS=0V, VIN=1V, CL=10pF, IL=0μA	

Figure 4-5 illustrates the simulated plot of V_{OUT} versus V_{IN} with the setup of VDD = 2V and VSS = 0V. The simulation results indicate that the offset between V_{OUT} and V_{IN} was 10mV for the input range from 1V to 2V.

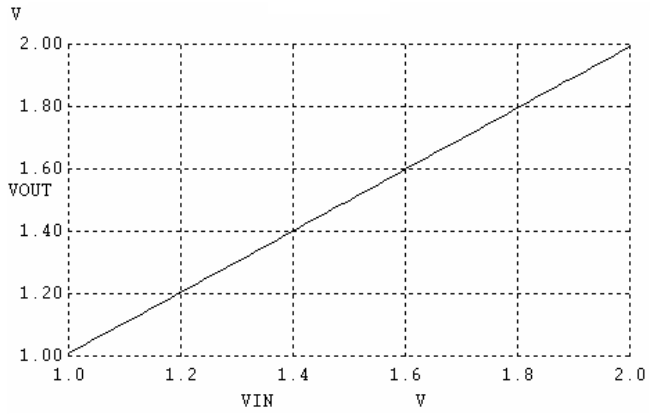


Figure 4-5 V_{OUT} vs V_{IN} (*VDD*=2V, *VSS*=0V)

Figure 4-6 illustrates the simulated plot of V_{OUT} with a sinusoidal V_{IN} input with 0.8V peak-to-peak magnitude and 500kHz frequency, and with the setup of *VDD* = 2V, *VSS* = 0V, and CL = 10pF. The simulation results indicate that the Total Harmonic Distortion (THD) was 0.5%.

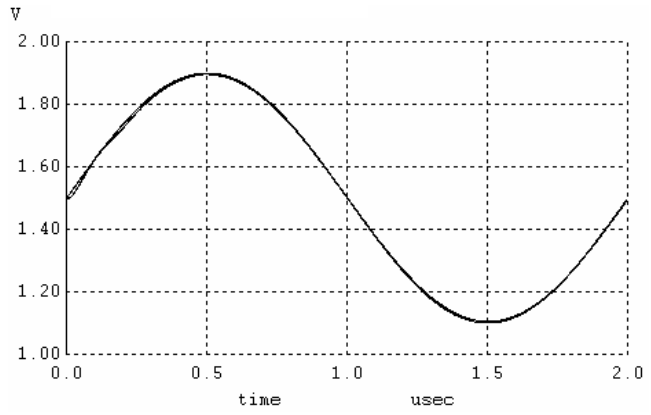


Figure 4-6 V_{OUT} and V_{IN} with 0.8Vpp 500kHz sinusoidal input (*VDD*=2V, *VSS*=0V, CL=10pF)

Figure 4-7 illustrates the simulated plot of V_{OUT} regulation capability against the load current I_L. With the setup of *VDD* = 1.5V, *VSS* = 0V, and V_{IN} =1V, the simulation results indicate that V_{OUT} kept on regulated within 10mV until the load current reaches to ±15μA.

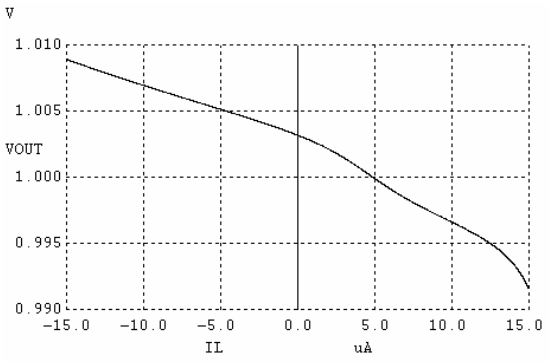


Figure 4-7 Load regulation (*VDD*=2V, *VSS*=0V, V_{IN}=1V)

B. Input impedance

Using bulk-driven MOSFETs in a differential pair of the operational amplifier is known to be a disadvantage in input current and capacitance [BLA98]. This sub-section describes that the theoretical overview as well as the simulated results to state that this disadvantage is not the case with the BDFVF.

Input current

With a bulk-driven MOSFET as an input device, the input signal is fed into the pn-junction of the MOSFET. The current through the pn-junction $I_{D\text{pn}}$ is modelled by Equation 4-2:

$$I_{D\text{pn}} = I_S \exp(V_D/V_t) \tag{4-2}$$

where I_s is the pn-junction current, which is also known as the scale current, when the voltage across the pn-junction V_D is zero. V_t is the thermal voltage, which is modelled as

$$V_t = kT/q \tag{4-3}$$

where k is the Boltzmann constant (=1.38 x 10^{-23}JK^{-1}), T is the temperature in Kelvin, and q is the charge of an electron (=1.602 x 10^{-19}C). At room temperature, V_t is approximately 26mV.

I_s can be described as in Equation (4-4):

$$i_S = A_S q n_i^2 \left(\frac{D_P}{L_P N_D} + \frac{D_n}{L_n N_A}\right) \tag{4-4}$$

where A_S is the active area of the source of the MOSFET, N_A and N_D are the doping concentrations of the acceptors and donors respectively, L_n and L_p are the diffusion length of holes and electrons respectively, D_p and D_n are the diffusion constant of holes and electron respectively, and n_i is the number of free electrons and holes in a unit volume of intrinsic temperature at a given temperature (≈1.5 x 10^{10} carriers/cm^3 at room temperature).

In the case of a bulk-driven differential pair, the input current is expected to be large because of the bulk being forward-biased. On the other hand for BDFVF, a large input current is not expected since the aim is to achieve a virtual short between the input and output. The simulated results of the offset behaviour and the input current are shown in Figure 4-8 and 4-9 respectively.

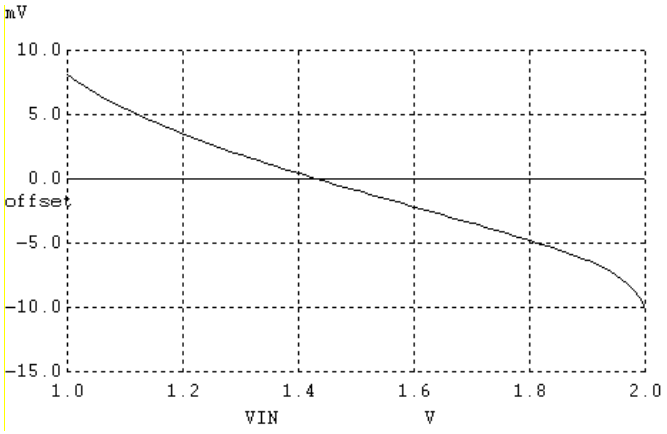


Figure 4-8 Offset voltage

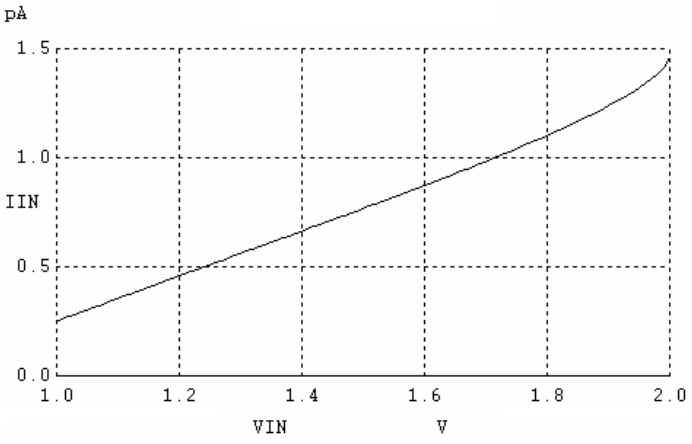


Figure 4-9 Input current (*VDD*=2V, *VSS*=0V)

The simulated result of Figure 4-9 shows that the input current remains at less than 1.5pA.

Input capacitance

The depletion capacitance of the pn-junction C_j can be modelled by Equation 4-5:

$$C_{sb-depletion} = \frac{CJ_{nwell-p+}}{(1-\frac{V_{SB}}{V_0})^{MJ_{nwell-p+}}} AS + \frac{CJSW_{nwell-p+}}{(1-\frac{V_{SB}}{V_0})^{MJSW_{nwell-p+}}} PS \qquad (4\text{-}5)$$

where $CJ_{nwell\text{-}psub}$ is the zero-bias (i.e. $V_{nwell\text{-}psub}$=0) body-junction capacitance per unit area over the n-well and p-substrate region, $CJSW_{nwell\text{-}psub}$ is the zero-bias body-junction capacitance per unit length along the sidewall of the n-well and p-substrate region, $MJ_{nwell\text{-}psub}$ and $MJSW_{nwell\text{-}psub}$ are the grading coefficient for area and sidewall components respectively, V_0 is the body-junction built-in potential, and A_{nwell} and P_{nwell} are the area and the perimeters of the n-well respectively. In the case of a bulk-driven differential pair, the input capacitance is expected to be large because of the bulk being forward-biased. On the other side for BDFVF, a large input capacitance is not expected since the aim is to achieve a virtual short between the input and output and hence only the depletion capacitance is introduced (i.e. the

diffusion capacitance can be avoided). To affirm this theoretical consideration further, the simulation condition as shown in Figure 4-10 was used.

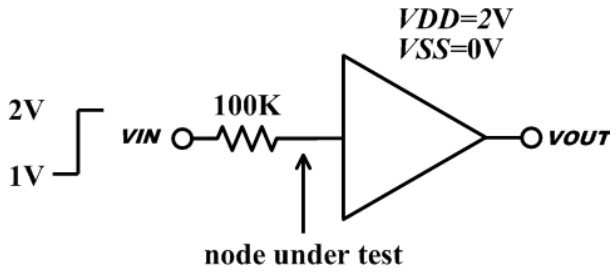


Figure 4-10 Simulation setup for the input capacitance

The simulated plot of the setup in Figure 4-10 is given in Figure 4-11.

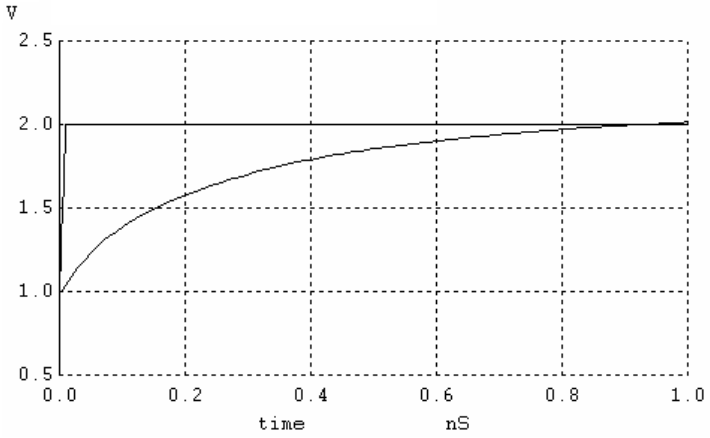


Figure 4-11 Simulation results for the Figure 10 setup

From Figure 4-11, the time constant τ was found to be 0.93ns. Hence, the input capacitance was determined as 9.3fF (τ=RC).

4.1.5 Section Conclusion

A new type of FVF called BDFVF has been presented. This proposal utilizes a bulk-driven MOSFET with the replica-biased scheme as the input device to eliminate the DC level shift. The theoretical overview of the input current and capacitance has been provided, and the simulation results showed that the input current and capacitance are in the pico-amp and femto-Farad ranges. The attractive and

advantageous performances of the FVF, such as high-power driving and low-power consumption were retained. The BDFVF is a powerful block of the FVF family which is free of level shift.

4.2 Bulk-Driven Super Source Follower

4.2.1 Introduction

The BDFVF proposed in the previous section leads to achieving small input capacitance so that the weak signal input can remain unaffected, and also a high slew-rate performance so that the output signal can remain driven with large capacitive loads, while the static power consumption can remain low. In overall, the BDFVF is a strong candidate in buffer applications.

Based on this work the author has undertaken further studies and discovered that the same circuit design technique can be applied to Super Source Followers (SSF) as well. This section proposes a circuit modification technique of a SSF, and its application example that can achieve not only power-efficient (low-power high-speed) performance with a low input capacitance but also an additional feature of rail-to-rail operation.

4.2.2 Previous Essential Works

This subsection briefly describes the previous works [GRA01] [LOP09] [RAM04] [HAG09A] using Figure 4-12, which the author has utilised to form the core part of our proposed CMOS buffer – a class-AB bulk-driven super source follower (BDSSF).

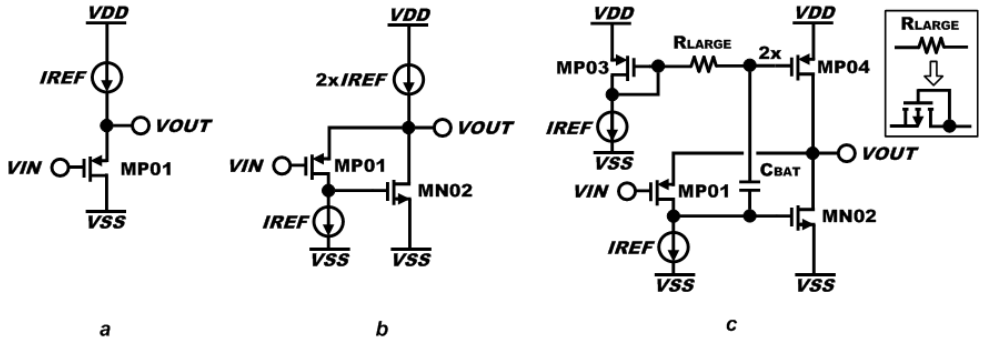


Figure 4-12 (a) class-A source follower, (b) class-A SSF, and (c) class-AB SSF proposed by Lopez-Martin *et al* [LOP09]

Figure 4-12(a) illustrates a conventional pMOS source follower, widely used as a level-shifted voltage buffer. If the body-effect is neglected, then the output voltage V_{OUT} follows the input voltage V_{IN} with an upward DC shift, i.e. $V_{OUT} = V_{IN} + V_{SG\text{MP01}}$, where $V_{SG\text{MP01}}$ is the source-to-gate voltage of the transistor MP01. In case of an nMOS source follower, V_{OUT} is instead shifted down from V_{IN}. This conventional source follower is widely used, however the drawback is that it is sensitive to resistive loads. Since the drain current of MP01 is affected by the output current, the DC-level $V_{SG\text{MP01}}$ cannot be kept constant. To overcome this concern, there exists a buffer which is often referred to as a Super Source Follower (SSF) [GRA01], as shown in Figure 4-12(b). The topology of Figure 4-12(b) is the same as Figure 4-12(a), but since the drain current through MP01 is biased with a constant current I_{REF} and is independent of the output current, $V_{SG\text{MP01}}$ is also held constant against the output current. Today, many published proposals using this SSF can be found.

Recently, A.J. Lopez-Martin *et al* emphasized in their work in [LOP09] that despite the output becoming much insensitive to resistive loads with the SSF, the Slew-Rate (SR) remains in class-A operation. In the case of a pMOS SSF as shown in Figure 4-12(b), the positive SR is limited to I_{REF}/C_L, where C_L is the load capacitance. Hence

increasing I_{REF} leads to one possible approach for the SR improvement, but at a cost of larger static power consumption. To avoid this trade-off, A.J. Lopez-Martin *et al* proposed a class-AB SSF in [LOP09] by using a quasi-floating gate (QFG) technique presented in [RAM04]. Their proposed circuit diagram is depicted in Figure 4-12(c).

In Figure 4-12(c), the gate of MP04 is weakly connected to the gate of MP03 with a large resistor R_{LARGE}, and also to the gate of MN02 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow across R_{LARGE} and therefore the gate voltage of MP03 and MP04 are the same. Thus the static power dissipation between Figure 4-12(b) and Figure 4-12(c) remains the same. In terms of AC characteristics, a high pass filter is formed with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, when observed from the gate of MN02 to the gate of MP04. Thus the ac element of the signal at the gate of MN02 can propagate to the gate of MP04, which in turn achieves class-AB operation without introducing any extra static current consumption. Furthermore, it is remarkable to realize in [LOP09] and [RAM04] that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, which leads to achieving a low cutoff frequency $1/(2\pi R_{LARGE}C_{BAT})$ with a moderately small capacitance of C_{BAT}. In [LOP09], A.J. Lopez-Martin *et al* discuss the C_{BAT} value in terms of attenuation factor α ($\approx 1/(1+C_{GS4}/C_{BAT})$). A C_{BAT} greater than 5 times C_{GS4} leads $\alpha > 0.83$, which is enough to propagate almost all frequencies except the DC component of the signal.

4.2.3 Class-AB Bulk-Driven Super Source Follower

Figure 4-13(a) illustrates the bulk-driven version of the SSF, which is the same type of circuit-design technique that was proposed in Section 4.1. As can be observed, the

input is connected to the bulk terminal of MP01 instead of its gate. MP02 is the replica of the input device MP01, i.e. MP02 and MP01 having equal transistor sizing and are biased with the identical drain current and the gate voltage. Since the bulk-terminal of MP02 is directly shorted to its source-terminal, MP01 tends to replicate the conditions of MP02 and hence the source-terminal follows the input voltage with no DC voltage in between, thus $V_{OUT} = V_{IN}$. Remarkably, the input capacitance C_{IN} of this type of buffer can be small because of the small junction capacitance of MP01. The expression of the junction capacitance of a MOSFET C_j can be simplified from Equation (4-5), which is given by

$$C_j = C_{j0} / (1+ (V_{SB} / V_0)^{0.5}) \quad (4\text{-}6)$$

where C_{j0} is the zero-bias (V_{SB}=0) junction capacitance, V_{SB} is the bulk-to-source voltage, and V_0 is the bulk junction potential. Since V_{SB} of MP01 in Figure 4-13(a) is designed to be zero, the junction capacitance of MP01 is constant at C_{j0}. The simulated value of C_{IN} is discussed in the next subsection.

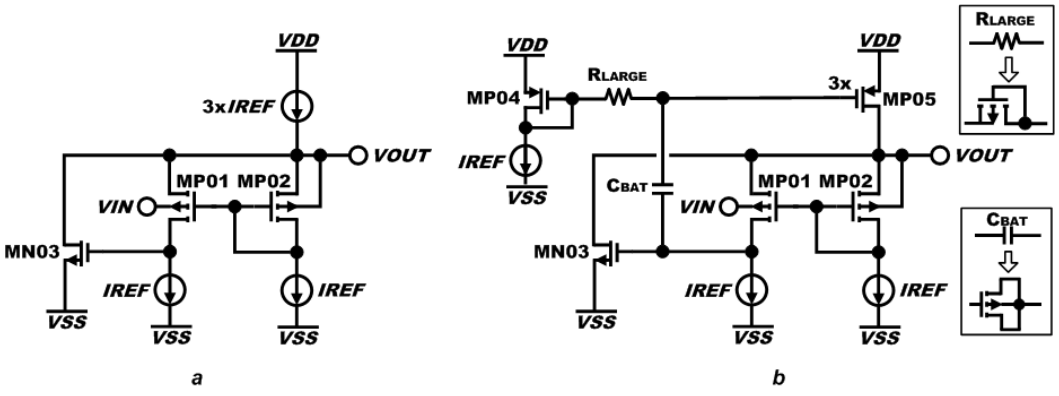


Figure 4-13 BDSSF (a) class-A operation, and (b) converting into class-AB operation using the QFG technique proposed by Ramìrez-Angulo *et al* [LOP09] [RAM04]

Figure 4-13(b) shows a class-AB BDSSF, where the class-AB operation has been implemented to Figure 4-13(a) with the same technique proposed by A.J. Lopez-Martin *et al* in [LOP09]. However, the author has chosen a modified approach for implementing the C_{BAT}. Ramìrez-Angulo *et al* stated the significance of the QFG

technique in [RAM04] that the actual value of C_{BAT} does not need to be highly accurate, as long as even a low frequency signal can be coupled. Owing to and appreciating this fact, the author attempted to eliminate the need for a poly-poly capacitor, and chose to form the C_{BAT} with a MOSFET as shown in Figure 4-13(b).

Application Example - Rail-to-Rail Class-AB CMOS Buffer

As an application example of the BDSSF, this block has been utilised in order to propose a rail-to-rail power-efficient CMOS voltage buffer. Figure 4-14 illustrates the circuit diagram of the proposal.

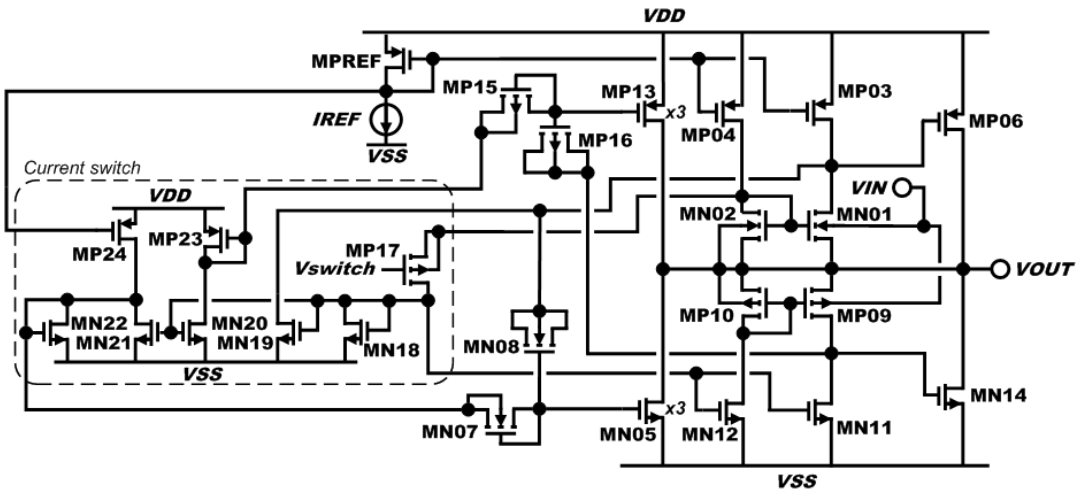


Figure 4-14 Class-AB rail-to-rail CMOS analogue buffer using a complementary pair of BDSSF

The operation principle of Figure 4-14 is as follow. From MN01 to MN08 and from MP09 to MP16 form a nMOS-type and pMOS-type of the BDSSF, respectively, and from MP17 to MP24 forms a current switch. The *Vswitch* at the gate of MP17 determines the switching point between the two types of follower. When V_{IN} (and thus V_{OUT}) is close to *VSS* the pMOS follower is active while the nMOS follower is off, and when V_{IN} moves towards *VDD*, V_{OUT} and the drain voltage of MN02 also increase and eventually MP17 turns on to reduce the drain current of MN01, MN02 and MN05 (i.e. to shut off the nMOS follower) and instead to increase the drain

current of MP09, MP10 and MP13 (i.e. to activate the pMOS follower) to continue the buffer operation.

4.2.4 Simulated Results

Using a 0.35μm CMOS process, the circuit of Figure 4-14 has been designed to operate at 1.8V supply voltage and simulated with the BSIM3 MOSFET models. Table 4-2 shows the simulation results summarizing the overall performance.

Table 4-2 Simulated results of the overall performance of Figure 4-14

Parameter	**Simulated Results**
-3dB frequency	6MHz
Static current dissipation	5μA to 8μA for V_{IN} sweeping between *VDD* and *VSS*
Slew rate	SR+ = 9.3V/μs, SR- = 13.7Vμs
Input capacitance	17fF
THD	-52dB (1.6Vpp@100kHz, CL=10pF) -50dB (1.6Vpp@100kHz, CL=22pF) -47dB (1.6Vpp@100kHz, CL=47pF) -46dB (1.6Vpp@100kHz, CL=68pF)
Simulated condition: *VDD*=1.8V, *VSS*=0V, *VSW*=0.9V, CL= 10pF	

From Table 4-2 it is apparent that the proposed buffer of Figure 4-14 meets the demands which were discussed in Section 4.2.1. The input capacitance is as small as 17fF, the SR is very high such that the buffer can deliver a 1.6Vpp 100kHz signal with a total harmonic distortion as low as -46dB when the capacitive load is as large as 68pF, whilst the static current consumption remains under 8μA. Figure 4-15 is the simulated results of DC-sweeping the V_{IN}, which indicates that the offset remains small throughout the rail-to-rail operation.

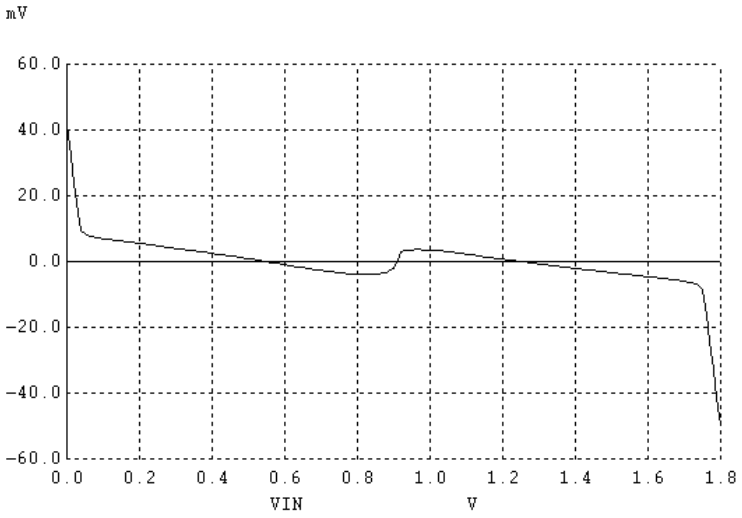


Figure 4-15 Simulated results of the DC offset voltage versus V_{IN} (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 4-16 indicates the simulated results of the static current dissipation with DC sweeping the V_{IN} between *VDD* and *VSS*.

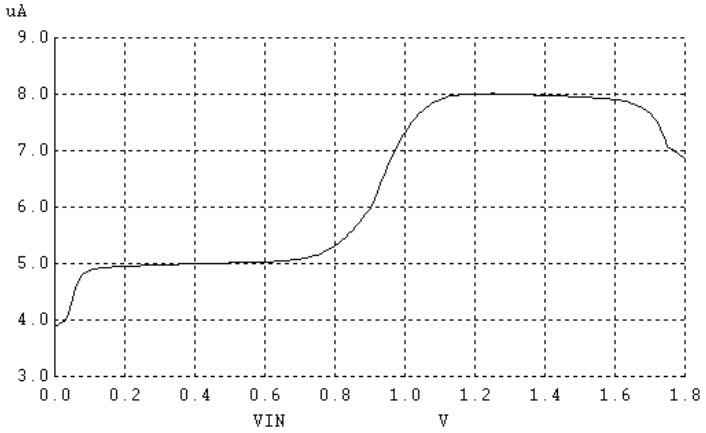


Figure 4-16 Simulated results of the static current dissipation (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 4-17 illustrates the simulated results of the V_{OUT} and the I_{OUT} with V_{IN} having 1.6V peak-to-peak 100kHz sine wave signal and a capacitive load CL of 68pF.

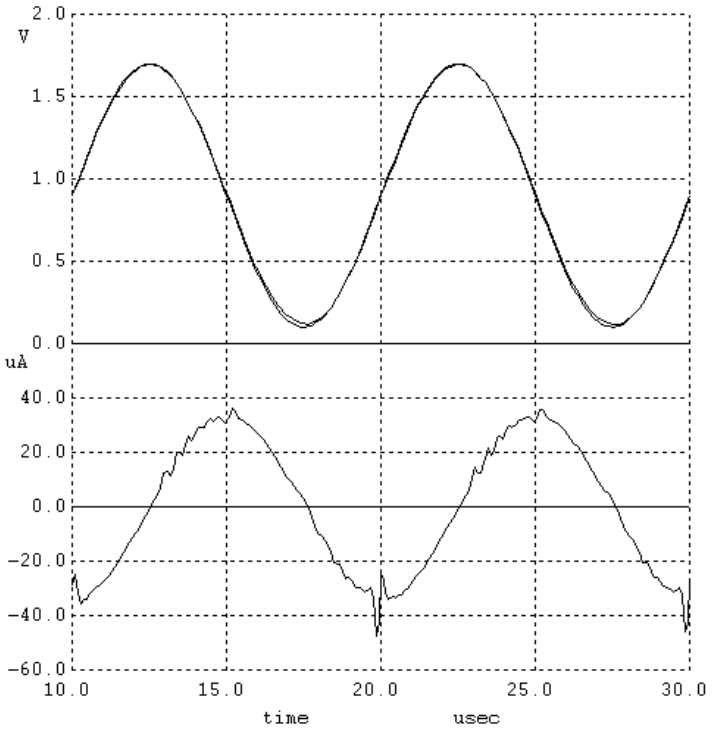


Figure 4-17 V_{OUT} vs V_{IN} and I_{OUT} with V_{IN} = 1.6Vpp 100kHz sinewave and CL =68pF (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 4-16 and Figure 4-17 show clearly that the goal of excellent power efficiency is achieved – during the static mode the current dissipation of the proposed buffer remains under 8μA, whereas I_{OUT} can be pushed and pulled to approximately ±40μA during the dynamic V_{IN} so that the Total Harmonic Distortion (THD) of V_{OUT} can be as small as -46dB even the CL is as large as 68pF.

To verify the input capacitance of the proposed buffer shown in Figure 4-14, the simulation condition as shown in Figure 4-18 has been set up.

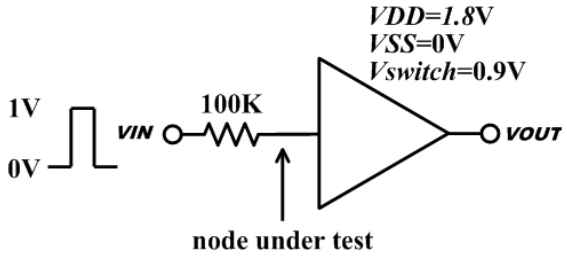


Figure 4-18 Simulation setup for the input capacitance of Figure 4-13

The simulated plot of the setup in Figure 4-18 is given in Figure 4-19.

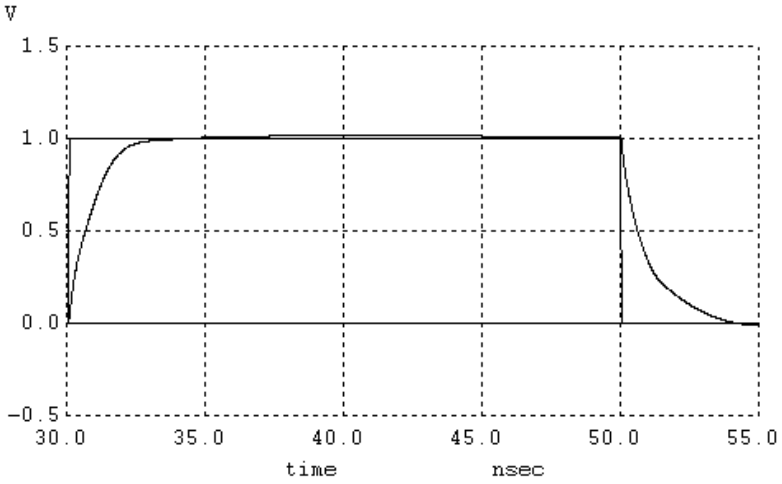


Figure 4-19 Simulation results for the Figure 4-18 setup

From Figure 4-19, the time constant τ was found to be 1.7ns. Hence, the input capacitance was determined as 17fF (τ=RC).

4.2.5 Section Conclusion

A new circuit block called BDSSF and a new type of CMOS buffer using the complementary pair of BDSSF have been presented. Utilizing the bulk-driven MOSFETs with the replica-biased scheme and the QFG techniques into the buffer enabled us to have a few femto-Farad range of the input capacitance so that the weak input signals are minimally affected, whilst delivering the signal without much distortion even if the capacitive load is very large. The static current consumption can remain small too. The proposed buffer can become a serious contender for portable electronics needing to deliver weak analogue signals into large capacitive loads with as little distortion as possible.

4.3 Bulk-Driven DC Level Shifter

4.3.1 Introduction

The BDFVF and the BDSSF proposed in Section 4.1 and 4.2, respectively, lead to achieving small input capacitance so that the weak signal input can remain unaffected, and also a high slew-rate performance so that the output signal can remain driven with large capacitive loads, while the static power consumption can remain low. In overall, both BDFVF and BDSSF are strong candidates in buffer applications.

Based on these works the author has undertaken further studies and discovered that BDFVF and BDSSF can lead to not only eliminating the DC level shift, but in fact the amount of the constant DC level can be easily programmed. The detail description of this new finding is given in the next subsection.

As to move on further, current mirrors, which are widely used for biasing and as active loads in analogue amplifiers, have been considered. Suppose that the current mirrors need to be operational in a low-voltage system. Under the limited supply voltage available, the designers must firstly confront the large voltage headroom consumed at the input device. One popular approach that can overcome this problem is by utilising a DC level shifter in-between the drain and the gate of the input device [RAM94], [RAJ02]. Figure 4-20 shows a couple of examples of CMOS circuit diagrams to describe this approach.

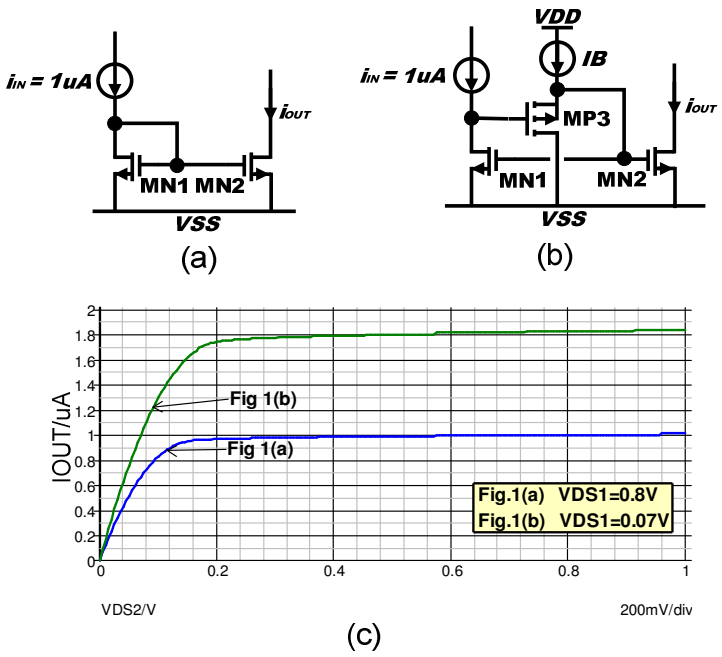


Figure 4-20(a) Simple current mirror with I_{IN}=1µA, (b) with a DC level shifter, and (c) the V_{DS2} DC-sweep simulated results

Figure 4-20(a) and (b) depict a simple nMOS current mirror and utilisation of a DC level shifter, respectively, and Figure 4-20(c) shows the simulated results of the two blocks using the BSIM3 MOSFET models of a 0.35µm CMOS process. From Figure 4-20(c), it is clear that a significant offset in the DC current is observed for Figure 4-20(b). This is because the circuit block formed by MP3 and *IB* generates a DC level shift upward by more than the threshold voltage of MP3 and causes MN1 to leave the saturated region and enter into the linear region. To avoid this undesirable side effect, a DC level shifter that can be programmed to operate at a level less than the threshold voltage of a MOSFET is rather in favour of the novel technique, which to the best knowledge of the author has not been reported in any open literature of today's circuit design techniques.

This section provides the detail investigation report of utilising the BDSSF that can overcome the concern mentioned above.

4.3.2 Proposal

The design objective in this section, which is to have a constant DC level shift less than the threshold voltage of a MOSFET, is simple to achieve by utilising the BDSSF of Figure 4-13(a) and (b). The source to bulk terminal of MP01, V_{SB1}, becomes reverse-biased by having a wider transistor width for MP01 and/or reducing its drain current I_{DS1}. The operation principle can be understood using the conventional square law model of a MOSFET. Whether the transistor size or the drain current of MP01 changes, this device maintains as the replica of MP02 and thus it operates in the saturated region. Let's suppose that MP01 is sized to have a relatively long length to minimize the effect of the channel length modulation, so that its drain current I_{DS1} can be approximated by:

$$I_{DS1} = (\mu_p C_{OX}/2)\ (W1/L1)\ (V_{SG1}-V_{T1})^2 \qquad (4\text{-}7)$$

where μ_p is the surface mobility of the pMOS transistor, C_{OX} is the capacitance of the gate oxide, W1, L1, V_{SG1}, V_{T1} are the width, the length, the source-to-gate voltage, and the threshold voltage of MP01, respectively. If for instance W1 is increased and/or I_{DS1} is decreased, then the overdrive voltage V_{SG1}-V_{T1} needs to be decreased to satisfy the above equation. However, since V_{SG1}, which is identical to the source-to-gate voltage of MP02, remains unchanged, V_{T1} needs to be increased. V_{T1} can be expressed by:

$$V_{T1} = V_{T0} + \gamma\ \{(2|\Phi_F|+V_{SB1})^{0.5} - (2|\Phi F|)^{0.5}\} \qquad (4\text{-}8)$$

where V_{T0} is the zero-bias threshold voltage, γ is the body effect parameter, $2|\Phi_F|$ is the Fermi potential, and V_{SB1} is the source-to-bulk voltage of MP01. As can be realized from this equation, to increase V_{T1}, V_{SB1} needs to be increased. Thus in summary, increasing W1 and/or decreasing I_{DS1} makes MP01 propagate a constant shift down voltage from the input to the output. Figure 4-21 shows the simulated

parametric sweep analysis of the width of MP01 and the length of MN05, denoted by W1 and L5, respectively.

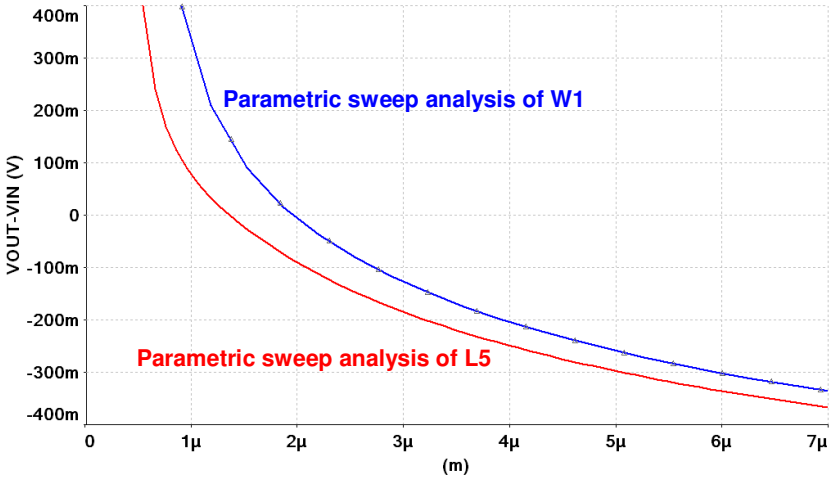


Figure 4-21 Parametric sweep simulation of Figure 4-13(a) and (b)

It is worth noting from Figure 4-21 that it is in theory feasible to level shift the input voltage upward as well as downward using the BDSSF of Figure 4-13(a) and (b), however from the view point of the effective input capacitance the authors recommend keeping the bulk-driven device MP01 in reverse biased operation. The description of the reverse biased junction capacitance, which is also known as the depletion capacitance C_j, is given by the following model:

$$C_j = C_{j0} / (1 + (V_{SB}/V_0))^{0.5} \tag{4-9}$$

where C_{j0} is the zero-bias (V_{SB}=0) junction capacitance, V_{SB} is the bulk-to-source voltage, and V_0 is the bulk junction potential. However, if the bulk of MP01 is in forward biased operation, then another capacitance model called the diffusion capacitance C_d would be introduced, which can be expressed by:

$$C_d = \tau_T (I_D/V_t) \tag{4-10}$$

where τ_T is the transit time of the junction diode, I_D is the amount of current through the diode, and V_t is the thermal voltage (≈26mV at room temperature). Thus in the results for the forward biased operation of the bulk-driven device, the total input capacitance C_T would then be expressed as:

$$C_T = C_j + C_d \quad (4\text{-}11)$$

Therefore, in order to avoid introducing the diffusion capacitance at the input, the author recommends using the proposed level shifter by configuring the bulk-driven device in reverse bias operation, i.e. using Figure 4-13(b) to shift down the voltage. For shifting up operation, the author recommends the use of an nMOS bulk-driven transistor for the input device.

4.3.3 Simulated Results

Table 4-3 shows the simulated results of Figure 4-13(b) using the BSIM3 MOSFET models of a 0.35μm CMOS process. To see how different level shift settings and design approaches affect the overall performances, several BDSSF blocks of Figure 4-13(b) have been designed for comparison. The overall performance of the BDSSF blocks with 0-volt DC shift, 0.3-volt DC shift down achieved by increasing W1, 0.3-volt DC shift down achieved by decreasing I_{DS1}, 0.6-volt DC shift down effected by modifying both W1 and I_{DS1} are summarised in Table 4-3.

Table 4-3 Simulated results of the overall performance of Figure 4-13(b) with different level shift configurations

Parameter	Vshift =0V	Vshift =0.3V*	Vshift =0.3V**	Vshift =0.6V
-3dB frequency	6.5MHz	8MHz	4.5MHz	5.5MHz
Total current consumption	5.2µA	5.2µA	5.2µA	5.2µA
Slew Rate+ Slew Rate-	2.0V/µs 6.2V/µs	2.1V/µs 5.3V/µs	2.1V/µs 5.0V/µs	2.2V/µs 5.5V/µs
PSRR	53dB	55dB	62dB	62dB
1/*f* noise at 1kHz	3.7µV/√Hz	3.7µV/√Hz	3.8µV/√Hz	4.0µV/√Hz
THD: 0.8Vpp 100kHz				
CL=10pF	-67.7dB	-66.6dB	-67.1dB	-63.6dB
CL=22pF	-62.0dB	-62.5dB	-64.1dB	-61.7dB
CL=47pF	-55.0dB	-56.7dB	-59.7dB	-58.6dB
0.8Vpp 500kHz				
CL=10pF	-51.6dB	-53.4dB	-48.1dB	-50.1dB
0.8Vpp 1MHz				
CL=10pF	-35.4dB	-38.8dB	-31.5dB	-34.4dB
* W1=3W2, L5=L6 ** W1=W2, L5=3.5L6 Unless stated, the setup condition is as follows: *VDD*=3.3V, *VSS*=0V, *VIN*=2.5V, CL=10pF				

The simulated results for the circuit of Figure 4-13(b) where the DC level shift is adjusted to 0.3V downward by modifying W1, and the input signal of 0.8Vpp at 100kHz is applied to the circuit with a load capacitance C_L of 10pF is as shown in Figure 4-22.

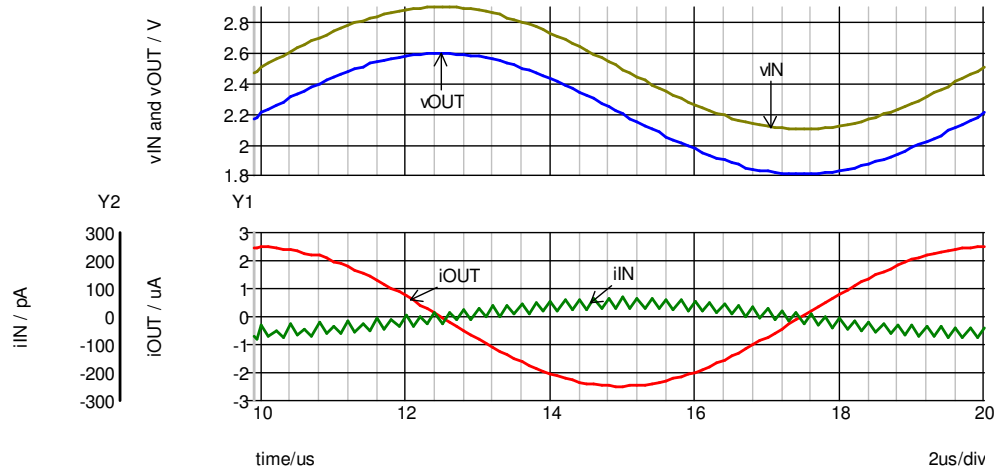


Figure 4-22 Simulated results of Fig. 2(b) with W1=3W2 and I_{DS1}= I_{DS2}, where v_{IN} = 0.8Vpp, 100kHz sinusoidal wave and CL with 10pF

As can be observed from Figure 4-22, the input current of only ±70pA is necessary to apply a 0.8Vpp 100kHz sinusoidal input voltage. It is worth remembering that this low input current would not have been possible to achieve if the bulk-driven input device MP01 was in the forward biased operation due to the significant increase in its input capacitance.

Application Example

As described in Section 4.3.1, a DC level shifter applied in a current mirror can be useful in reducing the voltage headroom consumption of the input device. Figure 4-23(a) illustrates the BDSSF of Figure 4-13(b) applied in a simple pMOS current mirror. RC and CC have been added between the input and the output of the BDSSF to minimize the output overshoot against the transient input signal. Given that V_{T0} of the pMOS transistor for the 0.35µm CMOS process is approximately 0.6V, the BDSSF of Figure 4-13(b) has been redesigned with a DC shift down of 0.2V, 0.5V and 0.6V and applied it to the current mirror as shown in Figure 4-23(a) to compare the overall performance. Figure 4-23(b) and Table 4-4 shows the simulated plots of the step response and the summary of the simulation results of Figure 4-23(a), respectively.

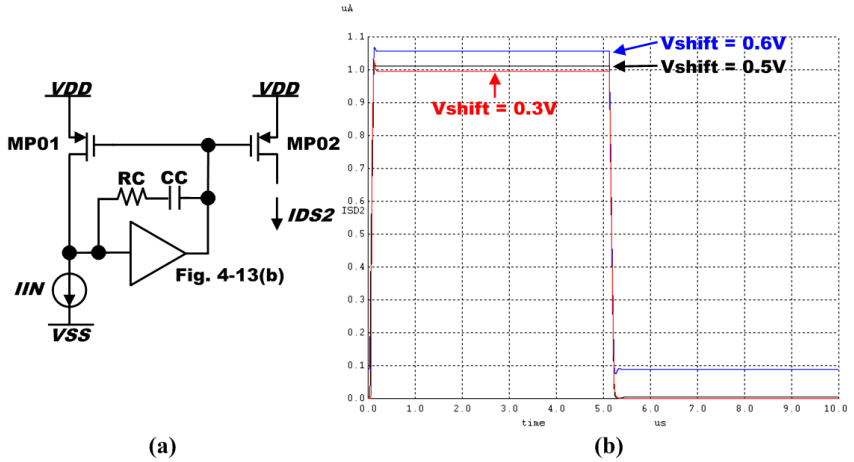


Figure 4-23 (a) A pMOS current mirror with level shifted BDSSF and (b) simulated plot of 1µA step response

Table 4-4 Summary of the simulation results of Figure 4-23(a)

Parameter	**Fig. 5(a) without Fig. 2(b)**	**Fig. 5(a) with Vshift = 0.2V**	**Fig. 5(a) with Vshift = 0.5V**	**Fig. 5(a) with Vshift = 0.6V**
Static current consumption of Fig. 2(b)	---	5.1μA	5.0μA	5.1μA
-3dB frequency	90MHz	70MHz	100MHz	100MHz
THD 1μApp				
1MHz	-53.3dB	-53.6dB	-53.2dB	-57.1dB
10MHz	-41.3dB	-37.0dB	-37.2dB	-38.1dB
Setup condition: *VDD*=1.8V, *VSS*=0V, *IIN*=1μA, *VD2*=*VDD*-0.5V				

As can be observed from Table 4-4, until 1MHz operation none of the BDSSF adds distortion noticeably. However, as can be realized from Figure 4-23(b) a caution is necessary to determine the amount of DC level shift. A DC level shift too close to V_{T0} would cause a noticeable offset in the DC current. In the case of the simulated plot of Figure 4-23(b), when the level shift is almost identical to V_{T0} (=0.6V) a DC offset current of approximately 60nA and 90nA is introduced when the input current is 1μA and 0μA, respectively. Even though the level shift was approximately 100mV below V_{T0} (i.e. when the level shift is set to approximately -0.5V), the offset current of 10nA and 4nA is drawn when the input current is 1μA and 0μA, respectively. Therefore it is advisable not to set the DC level shift too close to V_{T0}.

4.3.4 Section Conclusion

A novel design approach for a DC level shifter that can be programmed to a level less than the threshold voltage of a MOSFET has been presented. This technique is

based on utilising the power efficient BDSSF, with the bulk-driven input device forced to be reverse-biased to generate the constant DC voltage. SPICE simulations of the proposed block set up in a current mirror demonstrated that until 1MHz operation the proposed block does not introduce additional distortion, whilst the extra static current consumption spent is as little as 5μA. This proposed block has been shown to be an excellent solution for reducing the voltage headroom consumption of a current mirror but without introducing DC offset current.

4.4 Chapter Conclusion

In this chapter, new circuit design techniques that can convert the FVF [CAR05] and the SSF [GRA01] into the bulk-driven approach, which the author has given the names as BDFVF and BDSSF, respectively, have been presented. These two newly developed blocks still possess the load regulation capability so that the output becomes insensitive to resistive loads, but the bulk-driven approach allows implementing an additional feature such that the DC level shift can be eliminated and even programmable. The QFG technique [RAM04], that can convert the output slew rate from class-A to class-AB operation [LOP09], has also been investigated with the BDSSF and demonstrated that low-power high-speed performances can be achieved. Furthermore, it was verified that the degraded input impedance, which comes along with the bulk-driven approach, was not the case with BDFVF or BDSSF.

To further extend, two application examples of the BDSSF have been also demonstrated. One example was a design of a CMOS buffer using the complementary pair of BDSSF, which leads to achieving low-power (static current consumption of less than 8μA) high-drive (THD as low as -46dB with a 1.6Vpp

100kHz sine wave signal and a 68pF load) performances. The other application example was an implementation of the level-shifted BDSSF in a current mirror. Since the DC level shift of the BDSSF can be programmed at a level less than the threshold voltage of a MOSFET, the voltage headroom consumption of the input device of the current mirror can be reduced but without having the DC offset current at the output. The BDSSF in a current mirror does not introduce additional distortion until 1MHz operation, whilst the extra static current consumption spent is as little as 5μA.

In overall the newly developed BDFVF and BDSSF are powerful building blocks of source followers that can contribute achieving low-power high-speed performances of analogue circuit design.

Chapter 5 Bulk-Biased Cascodes

Cascode devices play essential roles in analogue systems, and many literatures discuss the properties in details [RAZ01], [SAN06], [SED11], [BAK08], [GRA01], [ALL02], [JOH97]. Adopting cascode devices in analogue amplifiers leads to increasing the output resistance and hence the small-signal gain as well. When a differential amplifier is used in a negative feedback configuration, its overall precision improves with the large open-loop small-signal gain of the amplifier, and thus implementing cascode devices helps a lot in this sense. In current mirror applications, cascode devices allow to supress the effect the channel-length modulation of the MOSFET and hence the output current becomes insensitive to the voltage at the output node. It is interesting to note the way Razavi describes the operation behaviour of cascode devices in his literature book in [RAZ01]. Quoting from his literature in the single-stage cascode amplifier section, *in a sense the cascode transistor "shields" the input device from voltage variation at the output*. Allen and Holberg book in [ALL02] provides the detail performance analysis for different operational amplifier (op-amp) topologies, and states that *the Power Supply Rejection Ratio (PSRR) of the folded-cascode op-amp has been greatly improved over the two-stage op-amp*. In Razavi's language, this statement can be alternatively described that the cascode device also "shields" the output node from the power supply noise.

This chapter presents a circuit design technique such that the output resistance of a cascode device can be further increased using its bulk-terminal. This technique was

developed by the author while tackling the problem of the low transconductance of a bulk-driven MOSFET g_{mb} which results to small open-loop gain of the op-amp when a bulk-driven differential pair (BDDP) is applied.

To demonstrate the effect of the developed circuit design approach of a cascode device, a complete set of a 0.8-volt rail-to-rail fully differential folded-cascode Operational Transconductance Amplifier (OTA) is designed using a 0.35μm twin-well CMOS technology having a threshold voltage of 0.6-volt. Taking this design as an opportunity, some other previous works of the bulk-driven approach are also adopted in the other part of the OTA for review. In this OTA, a complementary pair of BDDP [TER02] is implemented at the input stage to achieve a constant effective transconductance $g_{m(eff)}$. In the Common-Mode Feedback (CMFB) design, not only that the BDDP is applied at the input stage but also bulk-driven cascode current mirrors [TER02] have been adopted to reduce the voltage headroom consumption. The simulated results of the overall performance of the OTA are provided.

5.1 A 0.8-Volt Fully-Differential CMOS OTA Design

5.1.1 Introduction

As discussed in Chapter 2 a BDDP leads to achieving rail-to-rail Input Common-Mode Range (ICMR) operation under the low-supply voltage constraint, however many drawbacks are associated with this approach. One of the severe concerns is that the transconductance of a bulk-driven MOSFET is g_{mb} is less than the transconductance of a gate-driven MOSFET is g_m. This advantage and the

disadvantage can be visually realised by performing a simulation plot for g_{mb} and g_m, as shown in Figure 5-1.

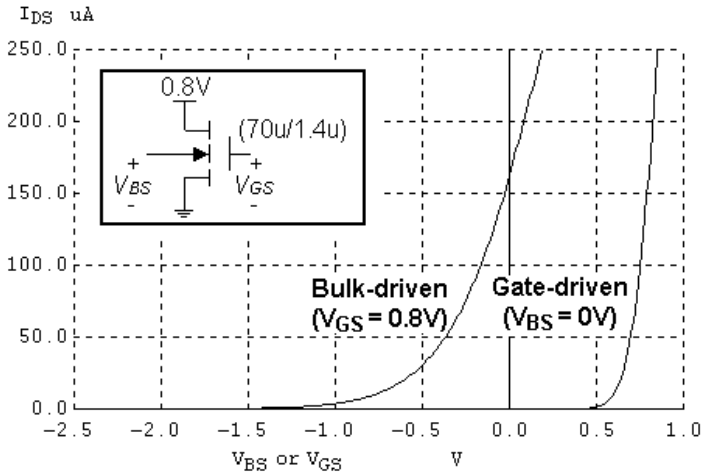


Figure 5-1 Simulating transconductance characteristics of gate-driven and bulk-driven nMOS transistors using a 0.35µm CMOS technology

As can be seen in Figure 5-1, the bulk-driven MOSFET is still in the active region at the zero-bias voltage which results to wider operation range than the gate-driven MOSFET. On the other hand g_{mb} is less than g_m. (g_m and g_{mb} are the slopes of its drain current versus its input voltage at the bias point). Thus implementing a BDDP in the op-amp design causes the open-loop small-signal gain of the op-amp to be reduced.

Another severe concern that needs to addressed is that g_{mb} is dependent to the DC operating point of the bulk-driven MOSFET, namely its bulk-to-source voltage V_{BS}. g_{mb} can be expressed by

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F| - V_{BS}}} \tag{5-1}$$

where $2|\Phi_F|$ is the Fermi potential and γ is the body-effect coefficient. Thus a BDDP causes a large variation in the effective transconductance of the op-amp $g_{m(eff)}$, which results to introducing signal distortion and creating difficulty in the frequency compensation of the multi-stage op-amps [HOG92], [WU94].

There are some previous works that address the above issues. The work presented by Terry *et al* in [TER02] addresses the issue the $g_{m}(eff)$ variation of a BDDP, and the work presented by Rosenfeld *et al* in [ROS04] addresses the issue of low g_{mb} of a BDDP adopted in folded-cascode OTA design by utilising the gain boosting technique. However, as studying further this gain boosting technique the author came up with an alternative design idea which leads to increasing the output resistance without introducing an additional hardware or extra power consumption in the core OTA block.

In this section the design of a 0.8 volt fully differential rail-to-rail folded-cascode OTA using a 0.35μm twin-well CMOS technology having a threshold voltage of 0.6 volt is presented. This OTA consists of not only a complementary pair BDDP for achieving rail-to-rail operation with constant $g_{m}(eff)$, but also the author's original design idea for the cascode devices of the OTA so that the output resistance is increased and hence the open-loop gain is enhanced to over 60dB.

5.1.2 Previous Essential Works

As the design task for achieving high-performance OTA that can be operated with a 0.8 volt supply voltage using a CMOS technology having a threshold voltage of 0.6 volt was not easy, many previous essential works have been referred and utilised in the OTA design. This subsection provides the brief review of those previous essential works.

According to the literature in [RAZ01], the topology of the gain-boosting technique was first invented in 1976 in [HOS79] and applied to boost the gain of the op-amps in 1989 in [BUL90] and [SAC90]. The concept of this topology is illustrated in Figure 5-2.

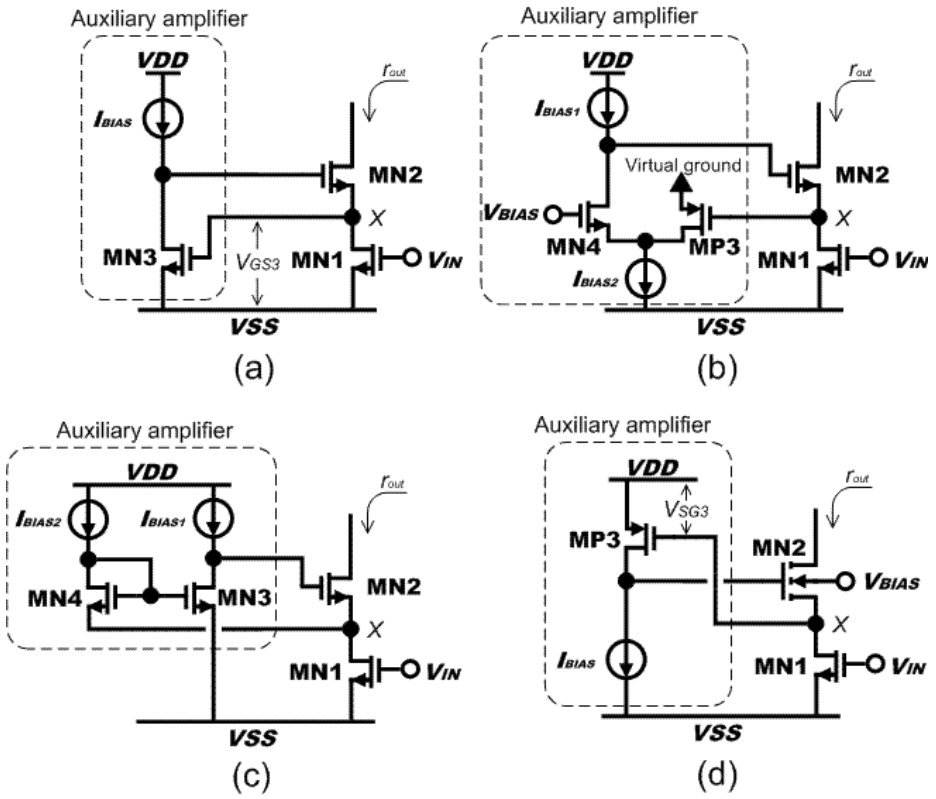


Figure 5-2 Gain-boosting topology with different auxiliary amplifiers, (a) common-source stage [HOS79] (b) folded-cascode [RAZ01], (c) common-source stage with a level shifter [COB94], and (d) complementary common-source stage [ROS04]

Figure 5-2(a) shows the circuit realisation of the gain-boosting topology using a common-source type of auxiliary amplifier placed in the feedback loop [HOS79], [BUL90], [SAC90]. This feedback amplifier regulates the voltage at node-X so that the output current remains more constant, which results to achieving a higher output resistance r_{out}. This approach, however, causes a limitation in the output voltage swing since the regulated voltage at node-X V_X becomes equal to the gate-to-source voltage of MN3 V_{GS3}, which is too much voltage consumption for low-voltage

applications. To overcome this concern, there are some known alternative design approaches today. Razavi's literature in [RAZ01] discusses utilising the folded-cascode type of auxiliary amplifier, as shown in Figure 5-2(b), as this concept allows pMOS and nMOS combination in the small-signal path. John and Martin's literature in [JOH97] on the other hand introduces Coban *et al*'s approach presented in [COB94], which is shown in Figure 5-2(c). This approach is identical to the one shown in Figure 5-2(a) except that a diode-connected MOSFET MN4 is additionally included for level-shifting purposes. In Rosenfeld *et al*'s work in [ROS04] presented an approach as shown in Figure 5-2(d), which its auxiliary amplifier is in the pMOS version of a common-source amplifier as shown in Figure 5-2(a). However, Zabihian *et al* in [ZAB07] provides the large-signal analysis of Figure 5-2(d) and states that it is not simple to operate the transistor MP3 in saturation under the low-supply voltage environment unless the threshold voltage of MN2 is reduced by V_{BIAS}. Also, V_X may be sensitive to *VDD* noise since the auxiliary amplifier in Figure 5-2(d) is not a differential amplifier (as V_X and *VDD* are directly related by V_{SG3}).

While studying further the approaches mentioned above, the author noticed an important property of a cascode device using its bulk-terminal. This chapter reports an OTA design without the use of auxiliary amplifiers but instead utilising only the bulk-terminal of the cascode devices for increasing the output resistance.

Bulk-Driven Current Mirror

The bulk-driven current mirror that was developed by Blalock *et al* in [BLA95], as shown in Figure 5-3(a), can eliminate the large voltage drop across the input device. This is because the voltage drop across the input device MN1 V_{DS1}, which is equal to the bulk-to-source voltage of MN1 V_{BS1}, does not need to be greater than the threshold voltage V_{T0} for proper operation. The cascode configuration [BLA96], as shown in

Figure 5-3(b), can be used to improve current matching and increase the finite output impedance of the current mirror. In this configuration, the voltage drop across the input devices MN1 and MN3, i.e. $V_{DS1}+V_{DS3}$ ($=V_{BS1}+V_{BS3}$), still remains below V_{T0}.

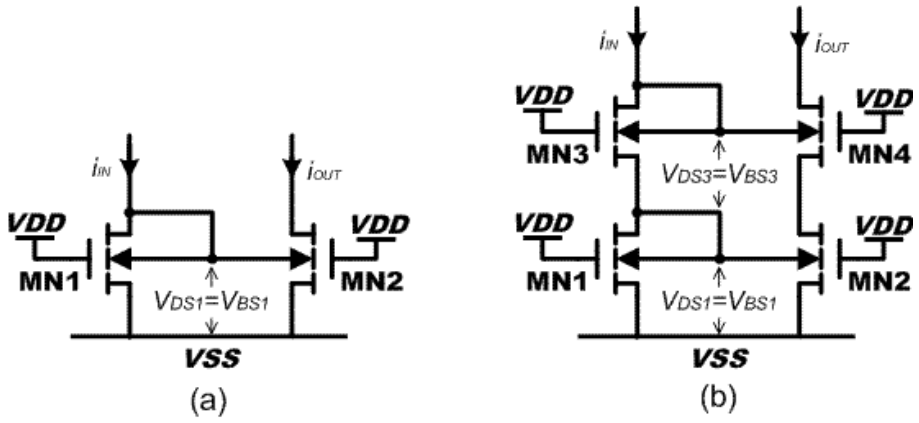


Figure 5-3 Bulk-driven current mirror (a) simple [BLA95] and (b) cascode [BLA96]

Taking the advantage of this low drop voltage property of the bulk-driven current mirror, the OTA design reported in this chapter utilises the Bulk-Driven Cascode Current Mirror (BDCCM) as shown in Figure 5-3(b) in the Common-Mode Feedback (CMFB) block.

Complementary BDDP

As discussed in the Introduction in Section 5.1.1, a BDDP applied in an op-amp design leads to achieving rail-to-rail IMCR operation but suffers from large $g_{m(eff)}$ variation. To overcome this concern a design technique called the complementary BDDP, which has been proposed by Terry *et al* in [TER02], has been applied in the OTA design reported in this chapter. Detail analysis results are given in the next section.

Supply-Independent Bias Circuit

To design an OTA that can be operated with a 0.8 volt supply voltage using a CMOS technology having a threshold voltage of 0.6 volt, a bias circuit block that can be also

operated with the 0.8 volt supply voltage was also needed. To accomplish this need, a supply-independent bias circuit block that can operated at a minimum supply voltage of V_{T0}+2V_{DSsat}, which was proposed by Dong *et al* in [DON02], has been applied in the OTA design reported in this chapter. Detail analysis results are given in the next section.

5.1.3 Proposal

Core OTA

Figure 5-4 illustrates the core part of the low-voltage fully-differential OTA, which utilises the folded-cascode topology and the bulk-driven approach at the input stage for achieving rail-to-rail ICMR operation.

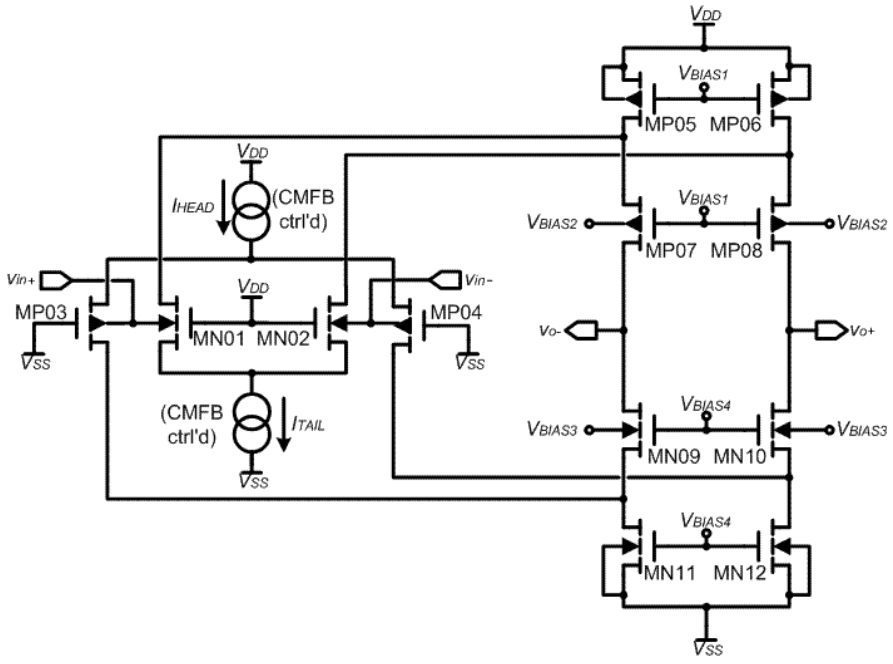


Figure 5-4 Proposed core OTA

Complementary BDDP

As mentioned in Section 5.1.1, the depletion characteristics of an nMOS transistor allow the ICMR to extend below the negative power supply. The transconductance of an nMOS transistor, however, increases by increasing the ICMR [BLA98].

This effect can be illustrated by simulating the transconductance of an nMOS transistor with the set-up shown in Figure 5-5(a). The results of the simulation are shown in Figure 5-6. The variance of the input transconductance causes the op-amp open-loop gain and also the phase margin to vary with ICMR. For a pMOS transistor with the setup illustrated in Figure 5-5(b), the complementary characteristics can be observed as illustrated in Figure 5-6.

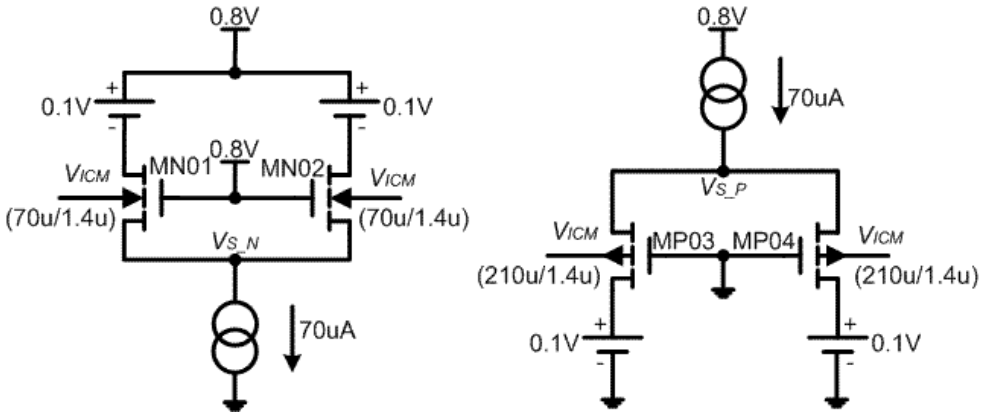


Figure 5-5 Setup for simulating (a) g_{mb1} and (b) g_{mb3}

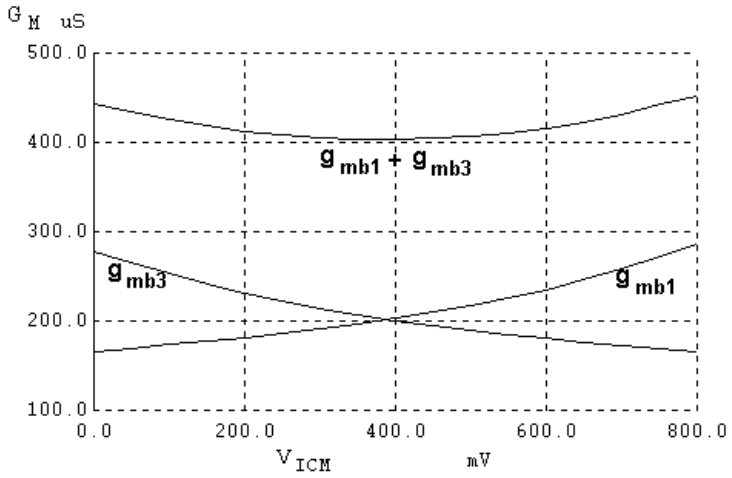


Figure 5-6 Simulation plots of g_{mb1} and g_{mb3}

In order to reduce the variance of the input transconductance, complementary BDDP can be utilised [TER02], as the results demonstrate in Figure 5-6. The overall transconductance variation, which is the sum of the transconductance of the nMOS and pMOS transistors, is improved by approximately 50%. To achieve a transconductance with minimum variations, a proper W/L ratio for the nMOS and pMOS transistors should be carefully selected.

Cascode Devices

As can be realized from Figure 5-1, the transconductance of a bulk-driven differential pair is less than that of a gate-driven differential pair, causing a challenge in achieving high open-loop gain for the amplifier. One possible method to increase the open-loop gain is to increase the output resistance. The output resistance of the core OTA in Figure 5-4 can be approximated to:

$$r_{out} \approx (g_{m7}+g_{mb7})r_{o7}(r_{o5}//r_{o1}) \;//\; (g_{m9}+g_{mb9})r_{o9}(r_{o11}//r_{o3}) \qquad (5\text{-}2)$$

From Equation (5-2) it can be realized that g_{mb7} and g_{mb9} can be increased as the bulks are slightly forward-biased. Therefore if a twin-well process is available, the bulks of cascode transistors could be slightly forward-biased. As an numerical example, for the term (g_m+g_{mb}), which equals to $(1+\eta)g_m$, the η can be increased by

approximately 0.04 when V_{BS} of the nMOS and pMOS cascode transistors are increased from -0.1V to 0.2V in a 0.35µm CMOS technology.

Common-Mode Feedback

To stabilise the CML of the two outputs to be midway between the power-supply voltages,a CMFB block is required. Figure 5-7 illustrates typical circuit diagrams of continuous-time CMFB circuits [ALL02], [RAZ01].

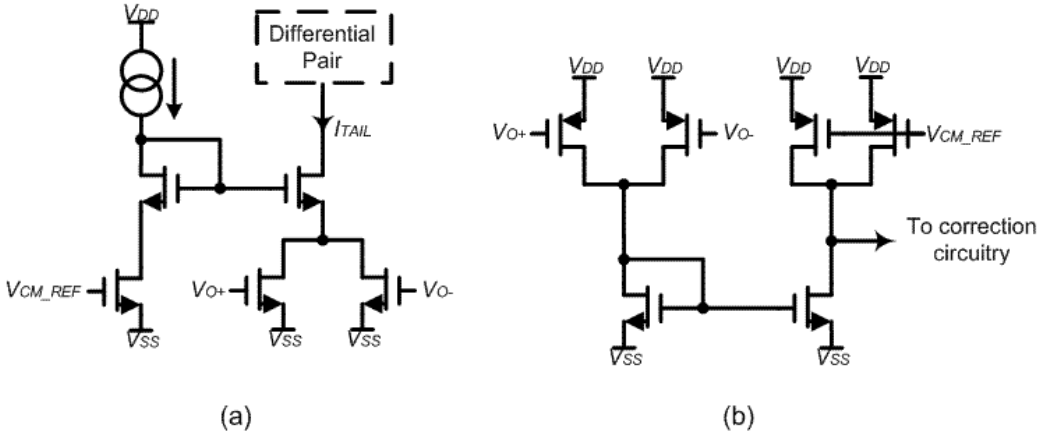


Figure 5-7 Typical CMFB circuit (a) current output and (b) voltage output

The problem of using the CMFB circuit shown in Figure 5-7 in a low-supply-voltage environment is that the reference input V_{CM_REF} and the output CML of the OTA have to be greater than the threshold voltage for the circuit to operate in the active region. To overcome this problem, the bulk-driven approach can be utilised. The proposed CMFB circuit is illustrated in Figure 5-8.

These proposed CMFB circuits are simply the same as Figure 5-7(b) with the bulk-driven differential pairs and current mirrors included. M_{C05P} and M_{C22N} are added extra to improve the input range of operation, which is the output range of the core OTA. Simulation results of this proposal are shown in Figure 5-9.

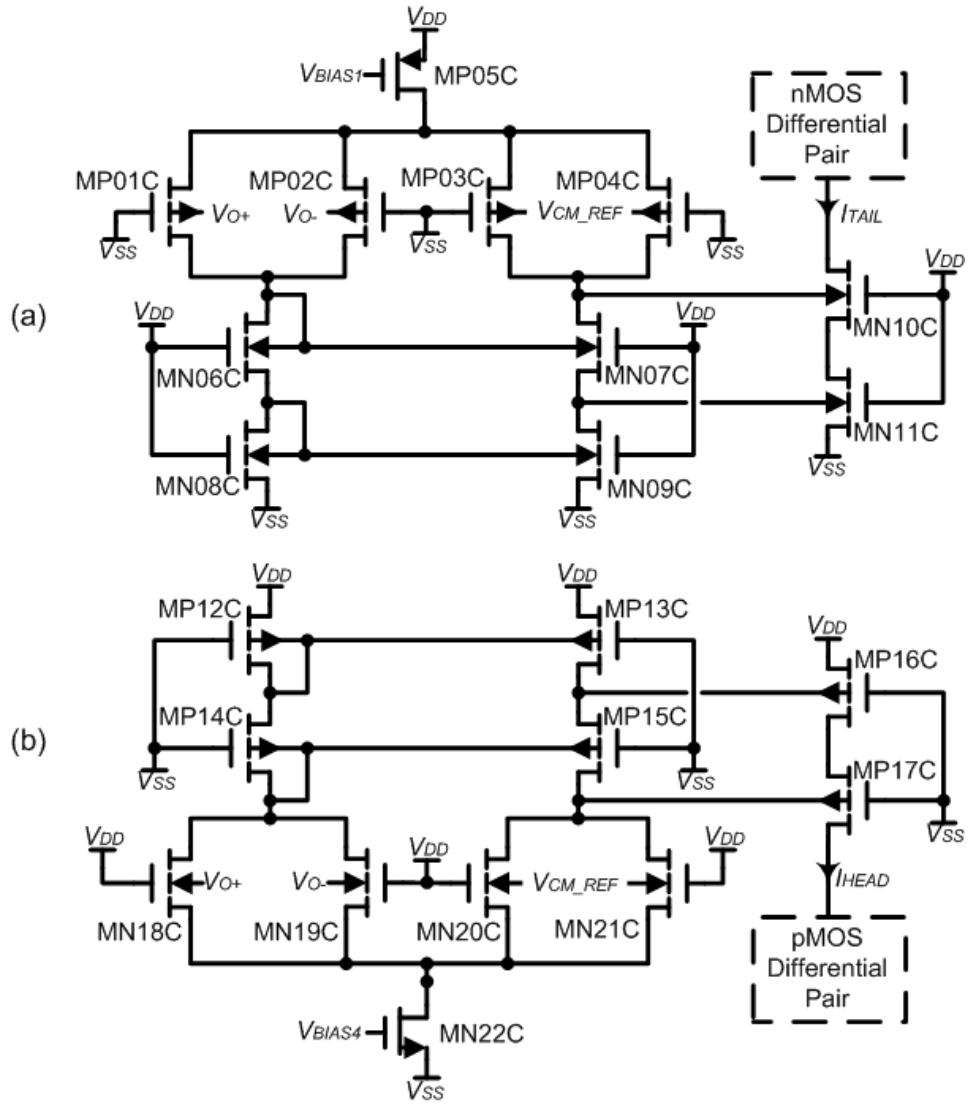


Figure 5-8 Proposed (a) nMOS driven CMFB and (b) pMOS driven CMFB

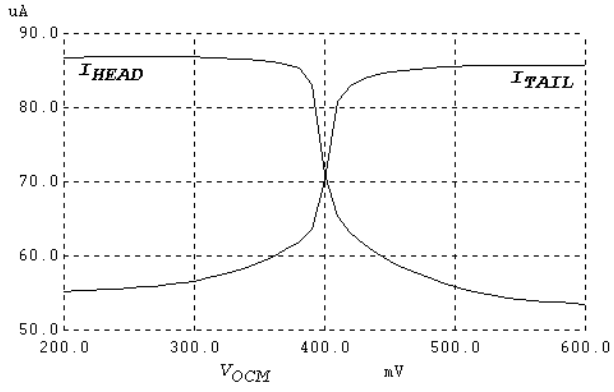


Figure 5-9 Verification of the proposed CMFB circuitry

The simulation results shown in Figure 5-9 imply that the bulk-driven technique can also be a candidate for low-voltage rail-to-rail CMFB design.

Supply-Independent Bias Circuit

The supply independent bias circuit presented in [DON02], as shown in Figure 5-10(a), can be operated at a minimum supply voltage of $V_{T0}+2V_{DSsat}$. This is very suitable for low-voltage systems and therefore applied for generating V_{BIAS1} and V_{BIAS4}. For generating V_{BIAS2} and V_{BIAS3}, which have to be less than V_{T0}, bulk-driven devices can be utilised as shown in Figure 5-10(b).

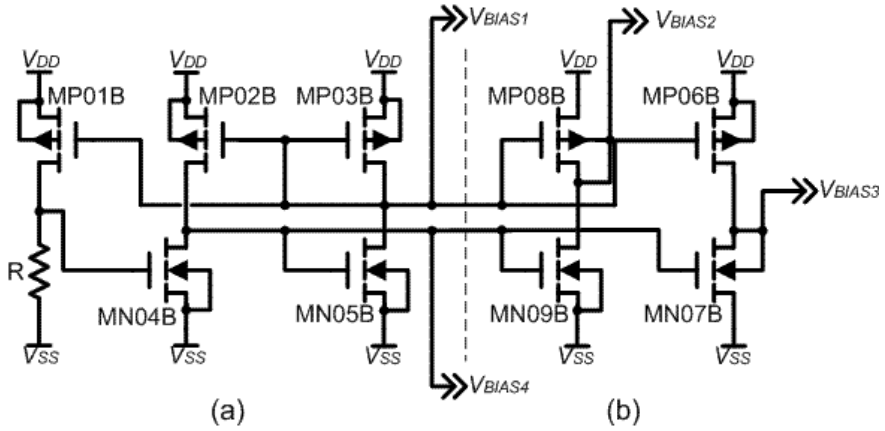


Figure 5-10 (a) Using the supply-independent bias circuit presented in [6] for generating V_{BIAS1} and V_{BIAS4} and (b) bias voltage generator for V_{BIAS2} and V_{BIAS3}

Simulation results of Figure 5-10 are illustrated in Figure 5-11.

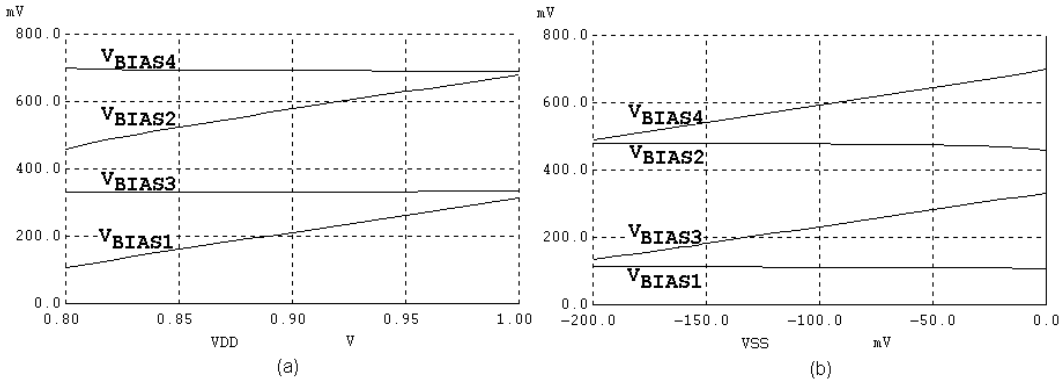


Figure 5-11 Effects of bias voltages with respect to (a) VDD and (b) VSS

As expected and seen in Figure 5-11, V_{BIAS1} and V_{BIAS2} are independent of *VSS* and therefore suitable for biasing pMOS devices. Similarly, V_{BIAS3} and V_{BIAS4} are independent of *VDD* and therefore suitable for biasing nMOS devices.

5.1.4 Simulation Results

A 0.35µm CMOS twin-well technology was used to verify the proposal. The Bode plot of the OTA with a load capacitance of 5pF is depicted in Figure 5-12. The overall OTA characteristics are shown in Table 5-1.

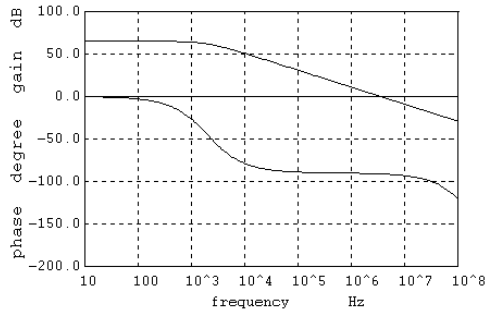


Figure 5-12 Simulated plots of open-loop gain and phase margin

Table 5-1 Summary of the proposed OTA Performance

Characteristics	**Simulated Value**
Open-loop DC gain	66dB
Unity gain-bandwidth	3.4MHz
Total current consumption	243µA
Phase margin	>80°
Differential output voltage swing	1V
Slew rate	SR+=4.7V/µs, SR-=5.1V/µs
ICMR	0.8V
VDD = 0.8V, *VSS*=0V, V_{ICM} = 0.4V, C_L = 5pF	

5.1.5 Section Conclusion

This paper explored the approach of low-voltage OTA design using the bulk-driven technique. The observed advantages are:

- As previously pointed out by [BLA98], BDDP can provide rail-to-rail ICMR operation, and bulk-driven current mirrors can be operated with less voltage headroom consumption.
- With the use of bulk- and gate-biased cascodes, the output resistance of a folded-cascode fully differential OTA can be increased with no additional circuit or extra power consumption.
- Bulk-driven CMFB can sense the input common-mode voltage smaller than the threshold voltage.

5.2 Input Impedance of the Complementary BDDP

Utilising the design work given in Section 5.1 as an opportunity, it is worth analysing the input impedance characteristics of the complementary BDDP stage utilised in the proposed OTA and compare with the differential pair design given in Chapter 3. Figure 5-13 shows the simulated ac characteristics of the input impedance.

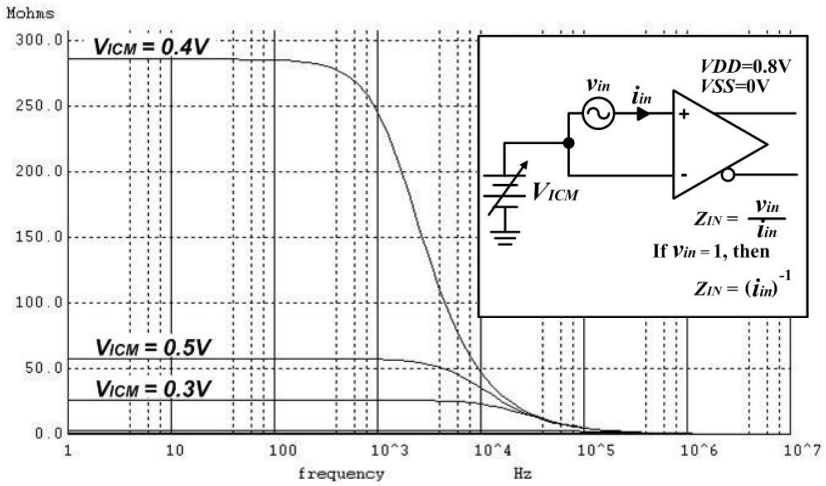


Figure 5-13 Simulation results of the circuit-level input impedance characteristics of the proposed OTA utilising the complementary BDDP stage

In comparison to Figure 3-8, it is apparent from Figure 5-13 that the input impedance of the BDDRB stage proposed in Section 3.1 is far better than the complementary BDDP. As can be observed from Figure 5-13, the input resistance maintains as high as 300MΩ for V_{ICM} around the mid-point of the supply voltage, but it considerably decreases to few-MΩ when V_{ICM} moves away by more than 200mV from the mid-point of the supply voltage. Therefore, in this aspect, it is evident that the BDDRB stage far advances.

5.3 Chapter Conclusion

Throughout the complete design of the proposed OTA, it was verified that the bulk-driven approach sees many advantages in low supply voltage analogue amplifier design. The BDDP and the BDCM can be applied not only at the core part of the amplifier but also at the CMFB block as well. Furthermore, it has been demonstrated that forward-biasing the bulk of cascode devices of the OTA helps enhancing the output resistance and hence the open-loop gain. Apparently, the bulk-driven

approach is a strong candidate that makes the low-voltage CMOS analogue amplifier design realisable.

Chapter 6 The BSIM3 Simulation and the Measurement of the Input Capacitance of a Bulk-Driven Buffer

So far this thesis has proposed several analogue CMOS design techniques using the bulk-driven approach, and for the verification the Berkeley Short-Channel Insulated-Gate Field Effect Transistor (IGFET) Model Version-3 (BSIM3), which is a widely used MOSFET model in the semiconductor industry [ALL02] [SED11], has been utilised in the SPICE simulations. However several works have been published recently that provide the comparison results of several popular MOSFET models with the measurement data of the fabricated bulk-driven devices, and report that Enz-Krummenacher-Vittoz (EKV) [ENZ95] is the most suitable MOSFET model for the nanometre bulk-driven applications [HE08] [WAN09] [WAN10].

The author finds the need for further extending this study for two reasons. Firstly, it may not always be the case that the fabrication services support EKV model for the available CMOS processes, and circuit designers may rather prefer to use the MOSFET model which the parameters have been already extracted by the fabrication services. Another reason is that circuit designers may need to size the length of the bulk-driven devices larger than the minimum, in particular in differential pair applications where good matching and reduced $1 / f$ noise are important [TER03]. The work reported in [HE08] [WAN09] [WAN10] all focuses on a bulk-driven device that is sized in a sub-micron channel length.

To further extent the author was particularly keen to focus on the study of the input capacitance of a bulk-driven CMOS buffer, because throughout the author's experiences in presenting the research works at conferences the author noticed the audiences' high interests in the input capacitance of the proposals.

Taking into an account of the viewpoint mentioned above, this chapter reports the research work on the use of the BSIM3 MOSFET model for determining the input capacitance of a CMOS bulk-driven buffer. To validate the accuracy of the BSIM3 simulation, a bulk-driven CMOS buffer has been designed and fabricated with On-Semiconductor's 0.35µm CMOS process in order to obtain the measurement results for comparison.

This chapter is structured as follows. In Section 6.1, a bulk-driven CMOS buffer that has been designed and fabricated using On-Semiconductor's 0.35µm CMOS process is described. Section 6.2 demonstrates the postlayout simulation results using the BSIM3 MOSFET model. Section 6.3 describes the taken procedure for the input capacitance measurement, and examines the obtained results by comparing with the simulated results. Lastly, in Section 6.4, the concluding remarks are stated.

The supplementary information to this chapter is also listed in Appendix B and C. Appendix B lists the other prepared materials, such as the SPICE code used for the simulation, the IC layout of the whole die and the bonding diagram, more snapshots of the microphotograph, and the used test board for the measurement. Appendix C provides all the logs of the measurement results presented in Section 6.3.

6.1 Designing a Bulk-Driven CMOS Buffer for Fabrication

Figure 6-1 shows the circuit diagram of a bulk-driven CMOS buffer that has been designed for fabrication using On-Semiconductor's 0.35µm CMOS process, and Table 6-1 shows the size information for each devices.

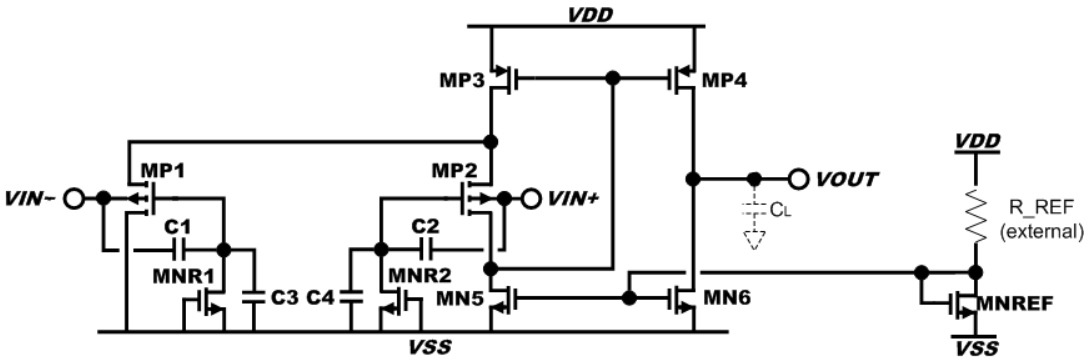


Figure 6-1 Circuit Diagram of the Bulk-Driven CMOS Buffer for Fabrication

Table 6-1 Device Dimensions for Figure 6-1

Device Name	Width	Length
MP1, MP2	60µm	1.4µm
MP3	20µm	1.4µm
MP4	10µm	1.4µm
MN5, MN6, MNREF	10µm	1.4µm
MNR1, MNR2	1.5µm	0.7µm
R_REF	220K	
C1, C2	0.2pF	
C3, C4	0.8pF	

The operation principle of Figure 6-1, which is simply the bulk-driven version of the differential voltage amplifier that was proposed in [SAN98], is as follows. Since MP2 is biased with a constant DC current, the AC current generated by the differential voltage input flows from MP3 to MP1, which is mirrored by the current mirror MP3/MP4 to the output. The key feature of Figure 6-1 is that the AC current is not limited by any DC current, and furthermore only three transistors MP1/MP3/MP4 carry the AC current which is clearly an advantage for high-frequency low-power design [SAN06]. In addition, the Quasi-Floating Gate (QFG)

technique [RAM04] has been applied at the gate of the input devices MP1 and MP2 instead of DC-biasing them with the negative supply rail *VSS*. With the QFG technique, capacitive voltage dividers have also been implemented in order to avoid MNR1 and MNR2 to be reversely biased during the rail-to-rail operation.

The layout of the buffer circuit of Figure 6-1 has been generated using a freeware tool called Electric which is available for download from [ELE11] (and free video tutorials are available for view from [BAK11]). Figure 6-2 shows the layout design, which the overall size turned out to be 199µm x 84µm.

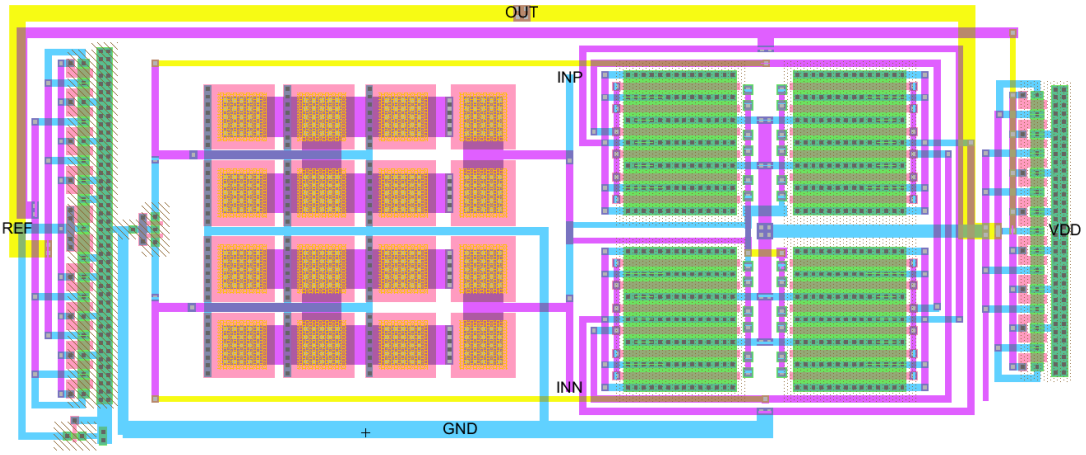


Figure 6-2 Layout Design of the Bulk-Driven CMOS Buffer of Figure 6-1

For the packaging, a DIL16 package, which consists of 16 pins and is the cheapest one available from the fabrication site, has been chosen. Also, since the mask cost of the chip remains the same for the chip area until 2mm^2, two of the same buffers have been integrated in the same chip. Figure 6-3 shows the pin assignment of the integrated two buffers.

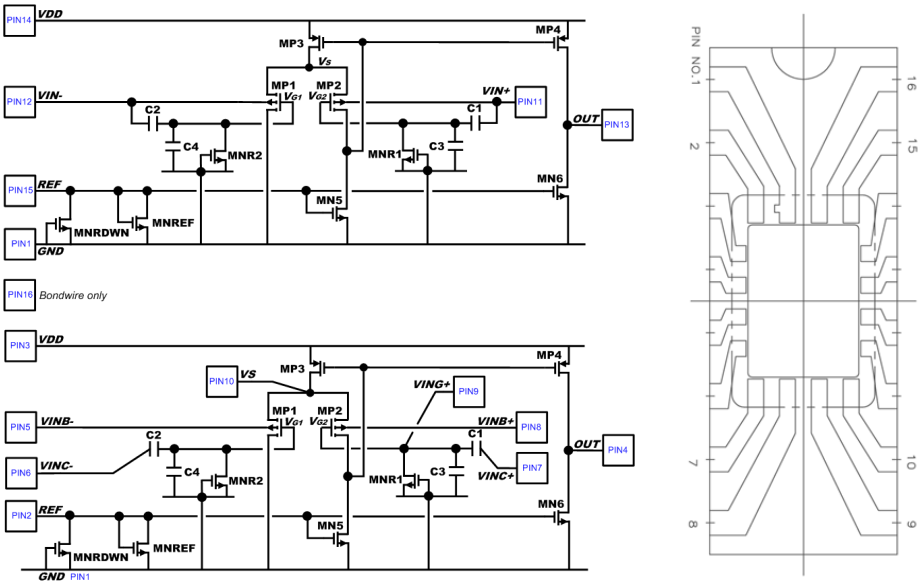


Figure 6-3 Pin Assignment

From Figure 6-3, please also remark that more pins have been assigned for the bottom buffer so that further measurements can be taken upon the need. Pin-5 is assigned at the coupled source of the differential pair so that $V_{SB1,2}$ can be measured. Pin-9 is connected to the gate of MP2 so that the output waveform of the QFG block with the capacitive divider can be measured. Pin-6 and pin-7 are the input pins for the QFG block with the capacitive divider, which are intended to be shorted to pin-5 and pin-8 respectively, but upon the need these pins can be left open instead to verify the effectiveness of the QFG block. Pin16 is connected to only the pad so that the characteristics of the pad itself, such as its parasitic capacitance, can be measured if necessary.

The other prepared materials, such as the IC layout of the whole die and the bonding diagram, and the prepared test board, are listed in Appendix B.

6.2 Postlayout Simulation

Using the extracted postlayout netlist of Figure 6-2, the bulk-driven buffer has been simulated with a supply voltage of 1-volt. With R_REF of 220K, the reference current that is flowing through MNREF becomes approximately 1µA and hence the overall DC current consumption of the buffer turns out to be approximately 4µA. Figure 6-4 and 6-5 show the BSIM3 simulation results of the open-loop frequency response with a load capacitance of 10pF, and the output waveform of the buffer in unity-gain configuration with a 1-volt peak-to-peak 10kHz sinusoidal input, respectively.

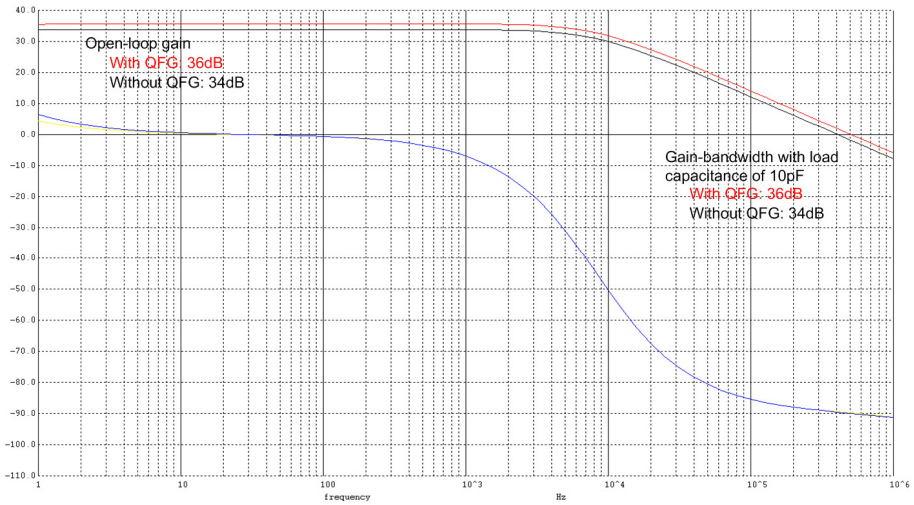


Figure 6-4 Postlayout Simulation Results of the Frequency Response (VDD=1V, VSS=0V, CL=10pF)

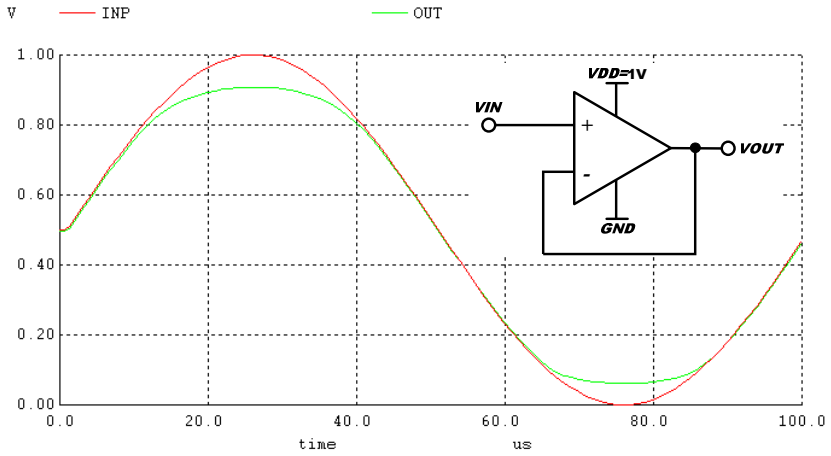


Figure 6-5 Postlayout Simulation Result of the Output Waveform with a 1Vp-p 10kHz Sinusoidal Input

Procedure for Simulating the Input Capacitance

The setup illustrated in Figure 6-6 shows the applied procedure for simulating the equivalent input capacitance $C_{IN,eq}$.

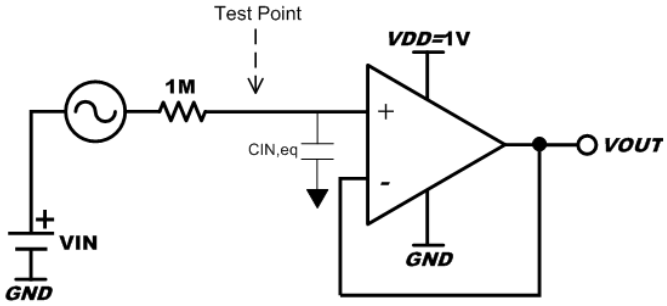


Figure 6-6 The Setup for Simulating $C_{IN,eq}$

The 1MΩ resistor shown in Figure 6-6 leads to constructing a low-pass filter at the test point, with a cut-off frequency f_{-3dB} as expressed in Equation (6-1):

$$f_{-3dB} = \frac{1}{2\pi C_{IN,eq}(1M\Omega)} \tag{6-1}$$

Thus once f_{-3dB} is determined then $C_{IN,eq}$ can be worked out by using Equation (6-2):

$$C_{IN,eq} = \frac{1}{2\pi f_{-3dB}(1M\Omega)} \tag{6-2}$$

From the theoretical observation expressed in Equation (6-2), the procedure for determining $C_{IN,eq}$ has been defined. A 100mV peak-to-peak sinusoidal input is applied at the input of the filter, and the frequency is adjusted to the cut-off frequency f_{-3dB}, i.e. the magnitude of the waveform at the test point becomes at 100mV x $(½)^{-0.5}$ (≈70.7mV) so that $C_{IN,eq}$ can be calculated using Equation (6-2). Figure 6-7 shows the postlayout simulation results of the determined f_{-3dB} point, where the DC operation point of the input is 0.5V.

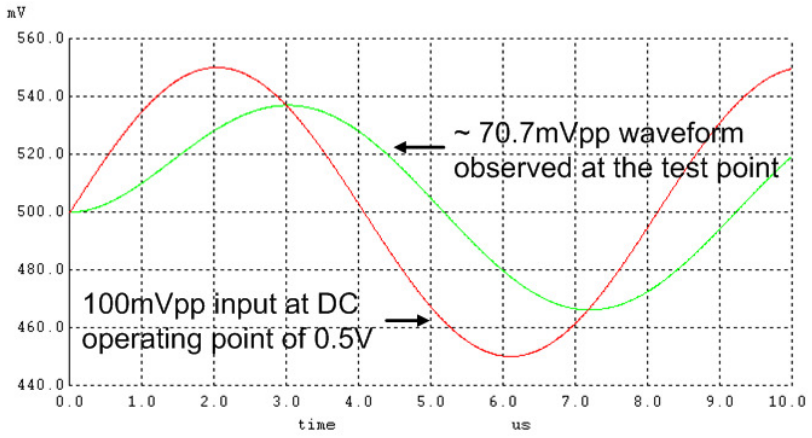


Figure 6-7 Postlayout Simulation of Figure 6-6 with the Input DC Operating Point at 0.5V

As discussed in Chapter 2, since the capacitance of the bulk of a MOSFET is bias-dependent of the DC operating point, the author decided to repeat Figure 6-7 with the DC operating point of the input V_{IN} from 0.1V to 0.9V in a 0.1V step. The SPICE code for performing this simulation is provided in Appendix B.

Figure 6-8 shows the determined $C_{IN,eq}$ per operation point V_{IN}.

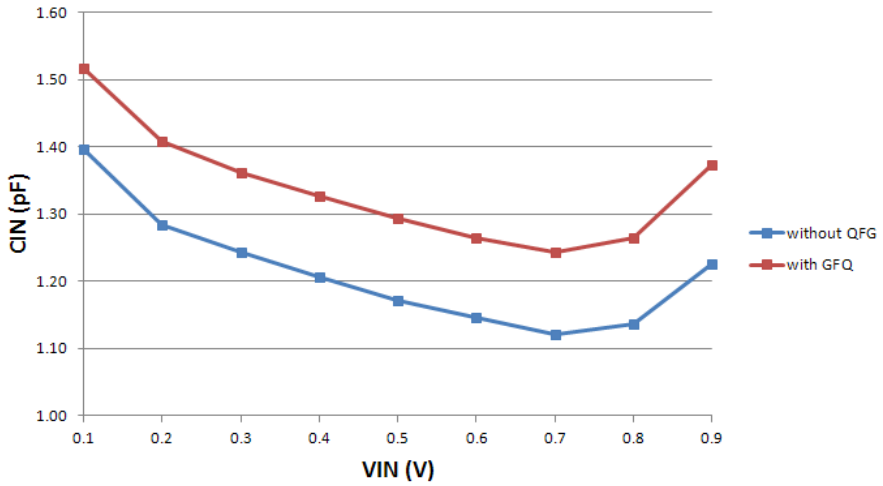


Figure 6-8 Postlayout Simulation Results of $C_{IN,eq}$

6.3 Measuring the Input Capacitance of the Fabricated Bulk-Driven Buffer

The buffer presented in Section 6.1 has been fabricated. Figure 6-9 shows the microphotograph of the fabricate buffer.

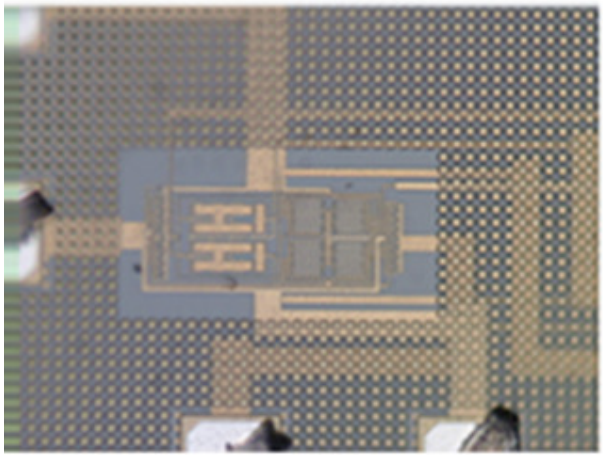


Figure 6-9 The microphotograph of the bulk-driven buffer presented in Section 6-1

In prior to assessing the input capacitance of the fabricated buffer shown in Figure 6-9, firstly the author verified that it is operational by configuring it in the same setup as described in Figure 6-5. Figure 6-10 shows the measurement result, which has become identical to the simulation result shown in Figure 6-5. Hence the fabricated buffer is ready to be tested for determining the input capacitance.

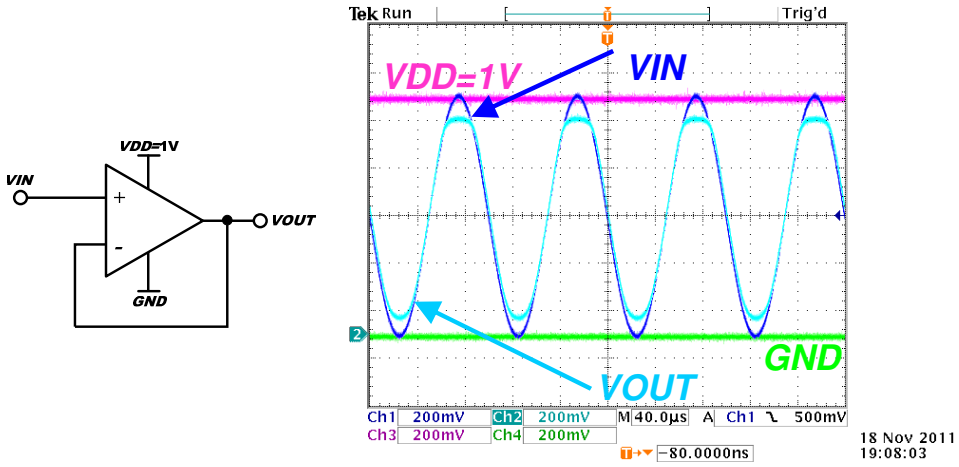


Figure 6-10 The Measurement Result of the Output Waveform with a 1Vp-p 10kHz Sinusoidal Input

Measurement Procedure

This sub-section describes the applied procedure for measuring the input capacitance of the fabricated buffer, where the DC operating point of the input voltage V_{IN} is from 0.1V to 0.9V in a 0.1V step, i.e. the same setup as shown in the simulation in Section 6.2.

It was in fact originally planned to use a LCR meter Wayne Kerr 4300, which is capable to measure the capacitance in femto-Farad range. However when this measuring equipment was set up with the fabricated buffer, the measured value shown in the LCD display did not turn out to be stable. The tendency was that the measured value became less instable when the test applied signal has larger amplitude like 1Vp-p and faster frequency (the highest frequency Wayne Kerr 4300 can produce is 200kHz), however the measured value shown in the LCD display was still unstable and thus unreliable to take the log. On the other hand with a discrete capacitor that was randomly selected, the Wayne Kerr 4300 indicated the expected capacitance value in the LCD display. Thus the measuring equipment itself was not faulty at all, but simply unsuitable for use with the fabricated buffer, and

consequently it was necessary to come up with an alternative procedure for determining the input capacitance of the fabricated buffer.

After searching through literatures the author came across with the work proposed in [NAT90], so called the phase measurement approach, which claims that only standard laboratory equipment is required for measuring small capacitances. To describe the proposed work of [NAT90] in brief, the phase lag between the output and the input sinusoidal signals of an RC low-pass filter can be expressed by:

$$\phi = \tan^{-1}(2\pi fRC) \tag{6-3}$$

where ϕ is the phase difference between the output and the input sinusoidal signals of the RC low-pass filter, f is the frequency of the applied input sinusoidal signal, and R and C are the resistance and the capacitance of the RC low-pass filter. If R and f are known and ϕ can be measured, then C can be worked out. In the work of [NAT90], the authors propose to adjust R and f such that ϕ near 45° is achieved for accurate measurement.

Using the concept described by the work in [NAT90], the fabricated buffer was set up as shown in Figure 6-11 and f is adjusted such that the phase shift between the output and the input of the sinusoidal signal ϕ became near 45°. Figure 6-12 shows the obtained measurement result.

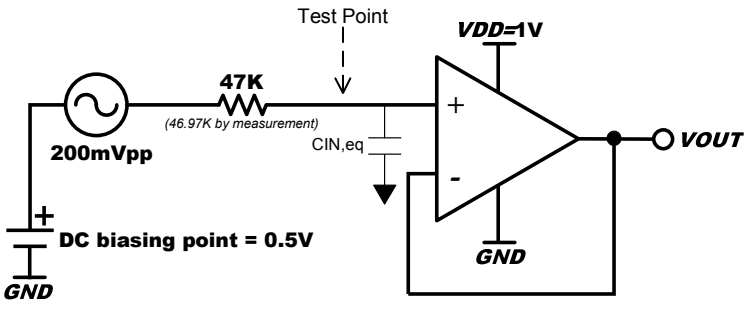


Figure 6-11 The Configured Setup for Determining the Input Capacitance of the Buffer

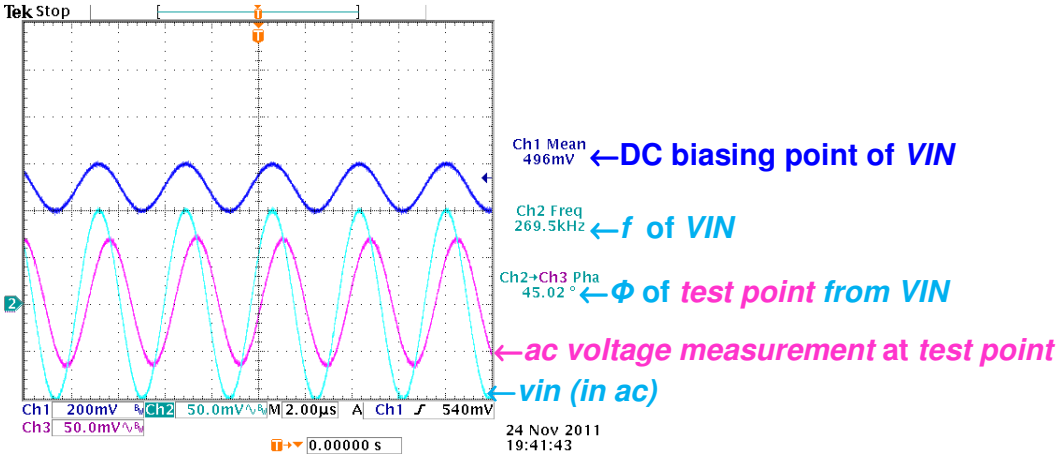


Figure 6-12 The Measurement Result of the Setup Shown in Figure 6-11

It is important to note, however, that the measurement result of Figure 6-12 also contains the parasitic elements (e.g. the parasitic of the used probe itself). To verify the overall parasitic element C_{stray}, the pin that is bond-wired to the PADONLY, as shown in Figure 6-12, has been probed and the same procedure has been taken for the measurement, so that in the end the capacitance of the interest, i.e. the input capacitance of the fabricated buffer $C_{IN,eq}$, can be extracted by calculation.

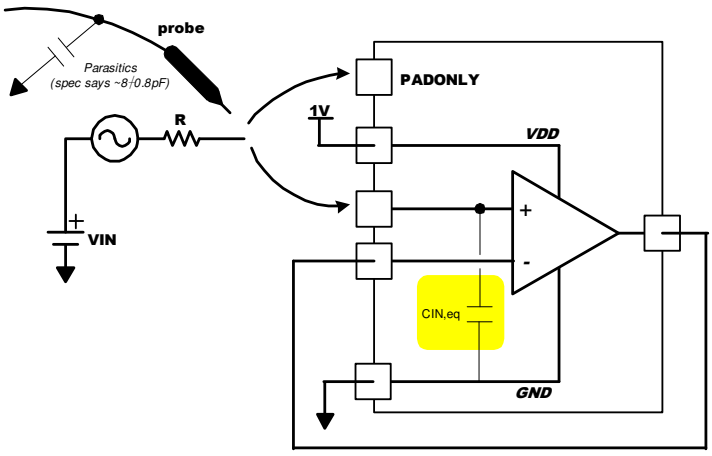


Figure 6-12 Measurement Procedure for Extracting $C_{IN,eq}$

For the R selection in Figure 6-12, various resistance values has been tried out to observe the effect in the overall result. Also, the amplitude of the input sinusoidal signal has been tried with 100mVpp and 200mVpp to see if it can additionally affect the measurement result. Table 6-2 shows the summary of the measurement results.

Table 6-2 Measurement Results of Figure 6-12 with Various Resistance Values and the Amplitudes of the Test Signal

Tested condition	Measurement Results	Extracted $C_{IN,eq}$ ($=C_{total} - C_{stray}$)
R=4k7 with 200mVpp	$C_{total} = 11.71 \pm 0.15$ pF $C_{stray} = 11.20 \pm 0.11$ pF	$C_{IN,eq} = 0.52 \pm 0.26$ pF
R=4k7 with 100mVpp	$C_{total} = 11.75 \pm 0.13$ pF $C_{stray} = 11.17 \pm 0.13$ pF	$C_{IN,eq} = 0.58 \pm 0.26$ pF
R=47k with 200mVpp	$C_{total} = 12.53 \pm 0.23$ pF $C_{stray} = 11.47 \pm 0.12$ pF	$C_{IN,eq} = 1.06 \pm 0.35$ pF
R=470k with 200mVpp	$C_{total} = 11.68 \pm 0.38$ pF $C_{stray} = 11.16 \pm 0.24$ pF	$C_{IN,eq} = 0.52 \pm 0.62$ pF
Other conditions: 1. The DC bias of the input voltage was set to 0.5V 2. The QFG block was unconnected in the buffer 3. The fabricated buffer has been measured for 20 times to compute the average and the standard deviation values.		

As can be seen from Table 6-2 the extracted result of $C_{IN,eq}$ is dependent to the measurement condition, which the author initially could not understand the reason behind. However, by taking a closer look at the setup, as shown in Figure 6-13, few reasons can be explained.

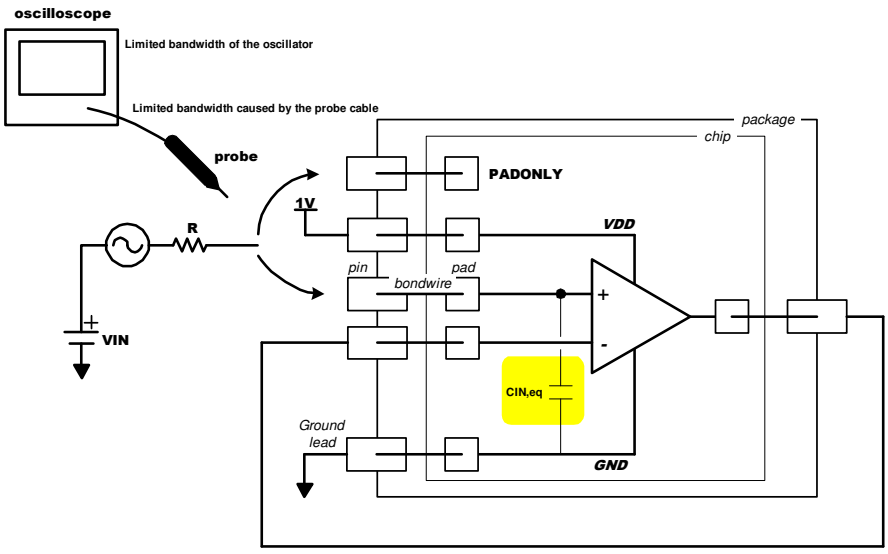


Figure 6-13 A Closer Look of the Set Up Shown in Figure 6-12

For R=4K7 *f* needed to be as fast as 3MHz in order to achieve ϕ near 45°, but faster frequency introduces some side effects that may ruin the measurement results. One side effect is that the inductive elements within the measurement setup (e.g. the bond wires within the package and the ground lead) would appear in the measurement result as *f* increases. One other side effect that would appear with faster frequency of the input signal is due to the performance limit of the measuring equipment. For instance, as *f* increases the input impedance of the probe dominates the loading effect, and the bandwidth limit of the probe and the oscilloscope may cause inaccuracy in the amplitude measurement of the signals [TEK_1], [TEK_2], [TEK_3]. Thus in order to reduce these possible side effects as minimal as possible, slower *f* (which consequently means the increased resistance of R) needs to be applied for accurate measurement.

However in contradict to the observation mentioned above, when R=470K and the adjusted *f* that achieves ϕ near 45° reduces to around 30kHz, the signal strength becomes weak and the noise disturbs the measurement. The results deviate more with

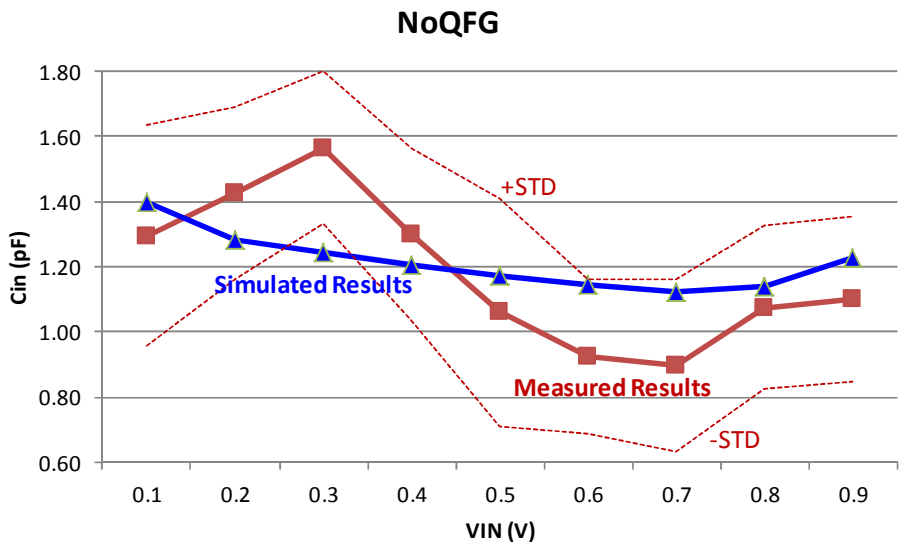
slower *f*. To obtain reliable measurement results, *f* needs to be faster than 30kHz to overcome the noise disturbance.

Concerning the amplitude of the input signal, 200mVpp was the maximum that can be set in this measurement as the objective was to measure the input capacitance of the fabricated buffer with the bias voltage of the input from 0.1V to 0.9V in a 100mV step. Under this measurement objective, a voltage amplitude of the input signal greater than 200mVpp would exceed the supply voltage rails of the buffer operating at 1V power supply. In order to justify that the amplitude of 200mVpp is large enough to extract $C_{IN,eq}$, another measurement has been carried out with the amplitude of 100mVpp to observe the effect. The result turned out the difference of only 0.06pF was obtained in the extracted $C_{IN,eq}$. Thus the amplitude of 200mVpp was judged as sufficiently large to carry on the experiment.

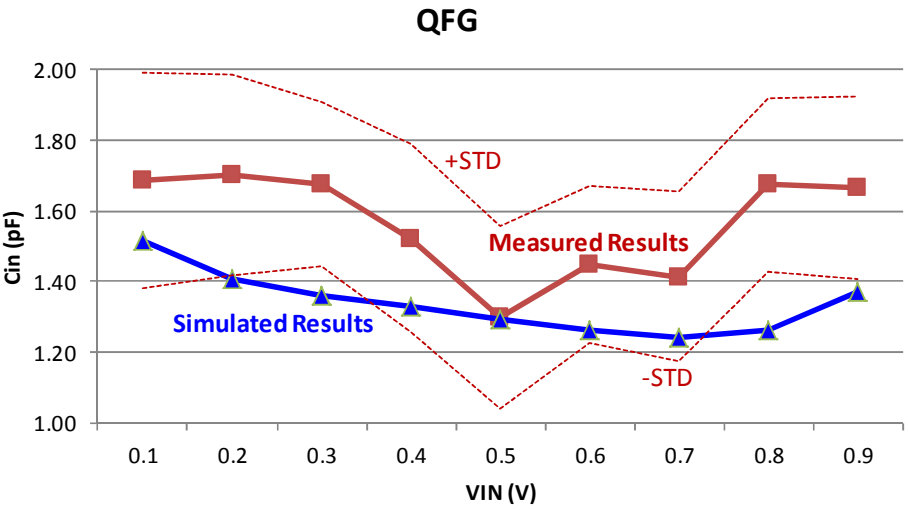
Considering all aspects mentioned above and carrying out further experiments with different setup of R, it appeared that R=47K with the amplitude of the input signal of 200mVpp gave a good compromise between the side effects of the fast signal input and the noise disturbance, and hence the author decided to continue the measurement under this setup.

Measurement Results and Observations

Base on the decision made for the measurement procedure as described above, the experiment was carried out to determine $C_{IN,eq}$ at different bias voltages V_{IN}. Figure 6-14 shows the measurement results of $C_{IN,eq}$ with V_{IN} varying from 0.1V to 0.9V in a 100mV step, and the comparison to the simulation results.



(a) the buffer without the QFG block



(b) the buffer with the QFG block

Figure 6-14 The Measurement Results of $C_{IN,eq}$ (20 measurements were taken to compute the average and the standard deviation) with V_{IN} varying from 0.1V to 0.9V in a 100mV step and the Comparison to the Simulation Results

The measurement has been taken for 20 times per each V_{IN} biasing point. In comparison to the simulation results, in average the measured $C_{IN,eq}$ differs by 16.9% (the maximum difference of 0.41pF at V_{IN} = 0.8V) and 12.9% (the maximum difference of 0.32pF at V_{IN} = 0.3V) for the buffer with and without the QFG block, respectively. The average deviation turned out to be 16.5 % (the maximum deviation

of ±0.30pF at V_{IN} = 0.1V) and 23.8% (the maximum deviation of ±0.35pF at V_{IN} = 0.5V) for the buffer with and without the QFG block, respectively. Taking into an account that the measurement of target is only in a few pico-Farad range, these deviation values are considerably small. The phase measurement approach proposed by [NAT90] works well in extracting $C_{IN,eq}$ of the fabricated bulk-driven buffer.

In overall, when V_{IN} is varied the measured $C_{IN,eq}$ changes more rapidly whereas the simulated $C_{IN,eq}$ looks more flat. The measured and the simulated results may appear to be different to each other, however considering that the measurement imperfections are also introduced by the noise disturbances, it is hard to predict how accurately the BSIM3 model performs in the simulation. Instead what can be stated from this experiment is that the BSIM3 model in the postlayout simulation gives a reasonable prediction of the $C_{IN,eq}$ of a bulk-driven buffer, within ±0.4pF of imprecision.

6.4 Chapter Conclusion

This chapter presented the study of the BSIM3 model used in the postlayout simulation of a bulk-driven buffer for determining $C_{IN,eq}$. For the verification the fabricated device was prepared and the phase measurement approach [NAT90] was investigated in details for extracting $C_{IN,eq}$. The obtained measurement and the simulation results of $C_{IN,eq}$ are relatively matched over various V_{IN} operating point. The BSIM3 model used in the postlayout simulation is a useful verification technique in predicting $C_{IN,eq}$ of a bulk-driven buffer.

Chapter 7 Conclusions

This Chapter summarises the achievements of this research work and provides the author's recommendations for further work relating to the bulk-driven approach.

7.1 Summary

The author's research objective as stated in Chapter 1 was to develop new circuit design techniques using the bulk-driven approach that can overcome many of the drawbacks which have been previously reported, and furthermore to invent new application areas of the bulk-driven approach where it can lead to performance enhancement in the field of CMOS analogue amplifier design. After reviewing the characteristics of a bulk-driven device in Chapter 2, where the key advantage is the depletion (JFET-like) characteristics whereas many of the associated drawbacks are related to small-signal behaviours and reliability, the following proposals have been made:

BDDP

In Chapter 3, two BDDP circuit blocks called the BDDRB and BDFVDP have been proposed. The BDDRB input stage uses the RBS to achieve constant small-signal behaviour hence to solve the non-linearity issue, and furthermore to diminish the latch-up issue by having the constant bias voltage. On the other hand, with the BDFVDP solves the issues of degraded input impedance characteristics and the latch-up by adding the reverse-bias connected diodes at the bulk-driven input. For both BDDRB and BDFVDP, the hardware implementation is simple.

Bulk-Driven Source Follower

Chapter 4 proposed the new application area of the bulk-driven approach, which is the design of source follower blocks. Like FVF and SSF, the proposed BDFVF and BDSSF blocks achieve low-power high-speed performances but with an additional feature such that the DC level shift can be eliminated and even programmable to the level that is less than the threshold voltage of a MOSFET. An application example of the level-shifted BDSSF in a simple current mirror was also given, which demonstrated the behaviour with the reduced voltage headroom consumption at the input device of the current mirror but without introducing an additional DC offset current.

Bulk-Driven Cascodes

Chapter 5 proposed another new application area of the bulk-driven approach, which is seen at the cascode output stage of op-amps, for instance folded-cascode OTAs. For any op-amps having a cascode at the output stage to increase the output resistance, then forward-biasing the bulk of the cascode device can further enhance the output resistance and hence the open-loop gain, which helps to cover the disadvantage of low g_{mb} of the BDDP but without introducing an additional hardware in the core part of the op-amps. Based on utilising BDDP and forward-biased cascode devices, a design methodology of a fully differential rail-to-rail OTA that can be operated with a power supply voltage of 0.8-volt using a 0.35μm twin-well CMOS technology having a threshold voltage of 0.6-volt is demonstrated, and the verification results indicated that the open-loop gain of over 60dB is achieved.

Verification of the BSIM3 model for Determining the Input Capacitance of a Bulk-Driven Buffer

Chapter 6 presented the study of the BSIM3 model used in the postlayout simulation of a bulk-driven buffer for determining the input capacitance. For the verification the phase measurement approach was applied for extracting the input capacitance of the fabricated buffer. The comparison between the measurement and the simulation results demonstrated that the BSIM3 model used in the postlayout simulation is a useful verification technique for predicting the input capacitance of a bulk-driven buffer.

In summary the bulk-driven approach may have an unfavourable impression due to too many associated problems, however the work reported in this thesis proves that that is false. Circuit design techniques like demonstrated in this thesis can overcome many of those drawbacks, and moreover new application areas can be identified and proposed by utilising the bulk-driven approach. The author's work has certainly made a progress in proving that this circuit design approach has a high potential in enhancing performances in the analogue amplifier design field, and it is encouraging to carry on the research to confront the difficulties of the low-voltage roadmap the ITRS is defining.

7.2 Recommendations for Further Work

After completing this work, the author would like to make the following recommendations:

Other New Application Areas

The author's work identified two new areas where the bulk-driven approach can be applied, in source followers and cascodes, however there have to be even more. In fact the author is currently aware of the following circuit blocks where the bulk-driven approach has been applied:

- Auxiliary amplifier for regulated cascode application [ZAB07], [MON09]
- Current conveyer [KHA06], [KHA11B]
- Mixer [HSI10], [SCH08] ,[VOR08]
- Phase Lock Loop [LUN09]
- Voltage Squarer [RAI10B]
- Variable Gain Amplifier [RAI10A]

Furthermore, the improved version of the bulk-driven current mirror, which was originally proposed in [BLA95], is recently proposed in [LAK11]. It is evident that the bulk-driven approach as a research topic is increasingly popular. The author recommends looking into other new application areas using the bulk-driven approach and/or developing the improved versions of the above circuit blocks.

Looking into other unsolved problems

The author's work reported in this thesis leads to solving many of the associated drawbacks of the bulk-driven approach but few others still remain, in particular the low g_{mb} issue. The cascode approach presented in Chapter 5 enhances the output resistance and so does the open-loop gain of the OTA, however the low g_{mb} issue has not been addressed and hence the low-speed high-noise issues remain. From literature search, the research effort is seen by means of partial positive feedback technique. The work in [CAR05] is applying the partial positive feedback at the active load, whereas the work in [RAI10C] is applying the partial positive feedback

at the input differential pair devices. The author fully agrees that the partial positive feedback technique is an excellent solution to avoid the speed reduction, but not the ultimate from the viewpoint that the issues of non-constant g_{mb} and the degraded input impedance characteristics remain unsolved. One last remark after completing this work and reviewing recent publications is that the author strongly believes the next research effort should be to develop a new circuit design technique that can combine the advantages of the gate and the bulk of a MOSFET.

Appendix A Published Works

The author's publications listed below are provided in this appendix.

[HAG05] Y. Haga, H. Zare-Hoseini, L. Berkovi, and I. Kale, "Design of a 0.8 Volt Fully Differential CMOS OTA Using the Bulk-Driven Technique", *IEEE Proc. International Symposium in Circuits and Systems*, 2005, pp. 220 – 223

[HAG06] Y. Haga, R. C. S. Morling, and I. Kale, "A New Bulk-Driven Input Stage Design for sub 1-volt CMOS Op-Amps", *IEEE Proc. International Symposium in Circuits and Systems*, 2006, pp.1547 – 1550

[HAG09A] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp.2717 – 2720

[HAG09B] Y. Haga and I. Kale, "CMOS Buffer Using Complementary Pair of Bulk-Driven Super Source Followers", *IEEE Electronic Letters*, Vol. 45, Issue 18, 2009, pp. 917 – 918

[HAG09C] Y. Haga and I. Kale, "Class-AB Rail-to-Rail CMOS Buffer with Bulk-Driven Super Source Followers", *IEEE European Conference on Circuit Theory and Design*, 2009, pp. 695 – 698

[HAG10] Y. Haga and I. Kale, "Bulk-Driven Flipped Differential Pair", *IEEE Proc. PhD Research in Microelectronics and Electronics*, 2010

[HAG11] Y. Haga and I. Kale, "Bulk-Driven DC Level Shifter", *IEEE Proc. International Symposium in Circuits and Systems*, 2011, pp.2039-2042

Design of a 0.8 Volt Fully Differential CMOS OTA Using the Bulk-Driven Technique

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***Abstract*— This paper explores and presents the possible approaches to the design of low-voltage Operational Transconductance Amplifier (OTA) using the bulk-driven technique. The design of a 0.8 volt fully differential folded-cascode OTA using a 0.35µm CMOS technology having a threshold voltage of 0.6 volt is presented. This OTA utilizes bulk-driven differential-pairs to achieve rail-to-rail input operation, and gate- and bulk-biased cascode transistors to increase the output resistance. A continuous-time Common-Mode FeedBack (CMFB) is used for this OTA, which implements the bulk-driven differential pairs to sense the common-mode voltage smaller than the transistor's threshold voltage, as well as bulk-driven current mirrors to reduce voltage headroom consumption. This OTA has been designed using Alcatel's 0.35µm twin-well CMOS technology, and the simulation results indicate an open-loop gain > 60dB, unity gain-bandwidth = 3.4MHz with a 5pF load, and an Input Common Mode Range (ICMR) of 0.8V.**

I. INTRODUCTION

The need of power supply voltage reduction in integrated circuits is driven by several factors: (1) the reduction in the minimum dimensions in CMOS technologies necessitating reduced power supply voltages, and (2) low supply voltages are in favor of reducing power consumption, weight and volume of the battery in portable electronics [1]. The main blocks of analog circuits such as the op-amps require a supply voltage of at least the sum of the magnitude of the nMOS and pMOS transistor's threshold voltages [3]. However, the threshold voltages do not decrease much below what is available today because of the digital logic [2], causing difficulty in designing analog circuits with low supply voltages on a standard CMOS technology. Consequently, novel circuit techniques are required to overcome this conflict.

The bulk-driven technique is a strong candidate for op-amp design under the constraints introduced by low-voltage operation. This paper firstly provides a brief review of the bulk-driven technique. It then follows by presenting a fully-differential Operational Transconductance Amplifier (OTA) design which operates at 0.8 volt power supply using a 0.35µm CMOS technology where the threshold voltage of the MOS transistor is 0.6 volt.

II. BRIEF REVIEW OF THE BULK-DRIVEN TECHNIQUE

When using a single MOS transistor as an amplifier, the input signal is usually fed into the gate (or sometimes the source) terminal and the bulk-terminal is tied to a fixed bias voltage (usually the supply-rail), as shown in Fig 1(a). In this configuration, named gate-driven MOS transistor throughout this paper, the gate-to-source voltage controls the drain current of the transistor. For a bulk-driven MOS transistor, on the other hand, its gate is tied to a fixed bias voltage (e.g. the supply-rail) and the input signal is fed into the bulk, as shown in Fig. 1(b). In this configuration, the threshold voltage of the transistor, which is a function of the bulk-to-source voltage, controls the drain current. The operational characteristics of the bulk-driven and gate-driven MOS transistors are illustrated in Fig. 2.

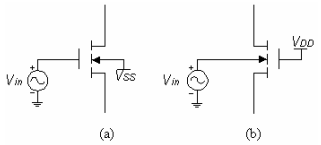

Figure 1. (a) Conventional gate-driven nMOS and (b) bulk-driven nMOS

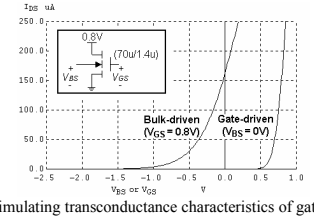

Figure 2. Simulating transconductance characteristics of gate-driven and bulk-driven nMOS transistors [3] using a 0.35µm CMOS Process

As shown in Fig. 2, to operate the gate-driven MOS transistor in the active region, the gate-to-source voltage

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needs to be greater than the threshold voltage (which is approximately 0.6 volts in this case). On the other hand, the bulk-driven MOS transistor behaves in a similar fashion to a depletion MOS transistor or a Junction Field Effect Transistor (JFET). Therefore, with the zero-bias voltage at the input node, the transistor is still in the active region. This is the key characteristic of a bulk-driven MOS transistor we use in designing low-supply voltage op-amps and other analog circuits. The two fundamental advantages of using the bulk-driven devices are:

- Bulk-driven differential pairs in op-amps significantly improve the Input Common-Mode Range (ICMR) since a bulk-driven device allows an extension in its input range on the negative side, as illustrated in Fig. 2. With proper design of the bulk-driven differential pair, the devices can remain saturated over the entire rail-to-rail ICMR.
- Bulk-driven current mirrors, as shown in Fig. 3(a), can eliminate the large voltage drop across the input device. This is because the voltage drop across the input device V_{DS}, which is equal to the bulk-to-source voltage V_{BS}, does not need to be greater than the threshold voltage V_{T0} for proper operation. The cascode configuration, as shown in Fig. 3(b), can be used to improve current matching and increase the finite output impedance of the current mirror. In this configuration, the voltage drop across the input devices still remains below the threshold voltage.

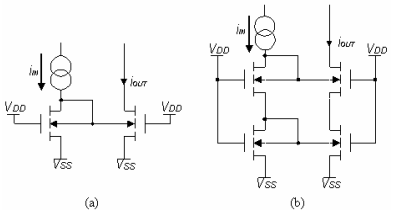

Figure 3. Bulk-driven current mirror (a) simple (b) cascode

However, there are several disadvantages of bulk-driven MOS transistors, which are all described in detail in [3]. The two fundamental ones are:

- As shown in Fig. 2, the transconductance of the bulk-driven MOS transistor g_{mb} is less than the transconductance of the conventional gate-driven MOS transistor g_m. (g_m and g_{mb} are the slopes of its drain current versus its input voltage at the bias point). Therefore utilizing a bulk-driven differential pair for op-amp design introduces a challenge in achieving high open-loop gain. Equation (1) is the level-1 model expression for g_{mb}/g_m ratio, η, which is typically 0.2 to 0.4, dependent on the Common-Mode Level (CML) of the input:

$$\eta = g_{mb}/g_m = (\gamma/2)(2|\Phi_F|-V_{BS})^{-0.5} \quad (1)$$

- The polarity of the bulk-driven MOS transistor is process related as *wells* are required to isolate the bulk-terminals. For a standard digital CMOS technology (i.e. n-well process), only pMOS can be bulk-driven. If both polarities need to be bulk-driven, then a twin-well technology is required.

III. State-of-the-Art and Design Objective

The op-amp design presented in [3] is a single-ended amplifier, which operates at 1-volt power supply using a standard digital CMOS technology with a threshold voltage of 0.8 volts. Their achieved open-loop gain is 48.8dB with a unity-gain bandwidth of 1.3MHz at 22pF load.

The op-amp design presented in [4] is a 0.8 volt fully differential OTA using a twin-well CMOS technology, and it utilizes a gain-boosting technique to increase the open-loop gain to 68dB with a unity-gain bandwidth of 93.3MHz with no load condition.

This paper reports on and demonstrates an alternative approach of increasing the open-loop gain of a fully differential folded-cascode OTA without the use of additional circuit or extra power consumption. In the next section, the design of 0.8 volt 60dB fully differential OTA is presented using a 0.35µm CMOS twin-well technology having a threshold voltage of 0.6 volts.

IV. Proposed Schematics

A. OTA

A one stage folded-cascode OTA using bulk-driven differential pairs at the input stage, which is illustrated in Fig. 4, was chosen for the low power-supply voltage amplifier.

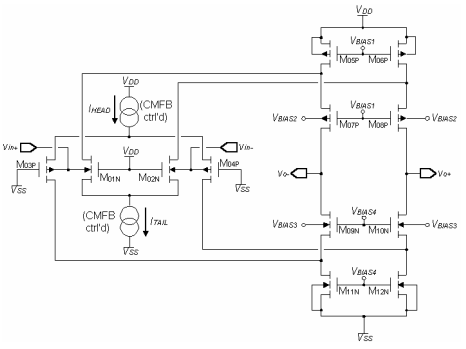

Figure 4. Proposed core OTA

- *Complementary Bulk-Driven Differential Pair*

As mentioned in section II, the depletion characteristics of an nMOS transistor allow the ICMR to extend below the negative power supply. The transconductance of an nMOS transistor, however, increases by increasing the ICMR [3].

This effect can be illustrated by simulating the transconductance of an nMOS transistor with the set-up shown in Fig. 5(a). The results of the simulation are shown in Fig 6. The variance of the input transconductance causes the op-amp open-loop gain and also the phase margin to vary with ICMR. For a pMOS transistor with the setup illustrated in Fig. 5(b), the complementary characteristics can be observed as illustrated in Fig. 6.

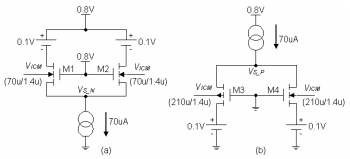

Figure 5. Set up for simulating (a) g_{mb1} and (b) g_{mb3}

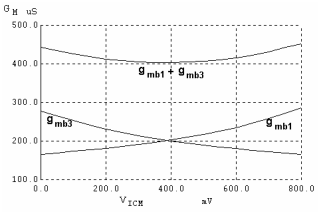

Figure 6. Simulation plots of g_{mb1} and g_{mb3}

In order to reduce the variance of the input transconductance, complementary differential pairs can be utilized [5], as the results demonstrate in Fig. 6. The overall transconductance variation, which is the sum of the transconductance of the nMOS and pMOS transistors, is improved by approximately 50%. To achieve a transconductance with minimum variations, a proper W/L ratio for the nMOS and pMOS transistors should be carefully selected.

- *Cascode Devices*

As can be realized from (1), the transconductance of a bulk-driven differential pair is less than that of a gate-driven differential pair, causing a challenge in achieving high open-loop gain for the amplifier. One possible method to increase the open-loop gain is to increase the output resistance. The output resistance of the core OTA in Fig. 4 can be approximated to:

$$R_{out} \approx (g_{m7}+g_{mb7})r_{o7}(r_{o5}//r_{o1})//(g_{m9}+g_{mb9})r_{o9}(r_{o11}//r_{o3}) \quad (2)$$

From (1) it can be realized that g_{mb7} and g_{mb9} can be increased as the bulks are slightly forward-biased. Therefore if a twin-well process is available, the bulks of cascode transistors could be slightly forward-biased. As an numerical example, for the term (g_m+g_{mb}), which equals to $(1+\eta)g_m$, the η can be increased by approximately 0.04 when V_{BS} of the nMOS and pMOS cascode transistors are increased from -0.1V to 0.2V in a 0.35µm CMOS technology.

B. Common-Mode Feedback

To stabilize the CML of the two outputs to be midway between the power-supply voltages the Common-Mode FeedBack (CMFB) is required. Fig. 7 illustrates typical circuit diagrams of continuous-time CMFB circuits [2], [7].

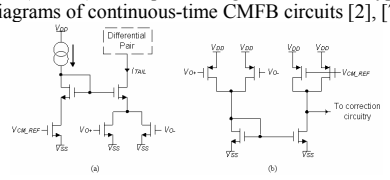

Figure 7. Typical CMFB circuit (a) current output and (b) voltage output

The problem of using the CMFB circuit shown in Fig. 7 in a low-supply-voltage environment is that the reference input V_{CM_REF} and the output CML of the OTA have to be greater than the threshold voltage for the circuit to operate in the active region. To overcome this problem, bulk-driven devices can be utilized. The proposed CMFB circuit is illustrated in Fig.8.

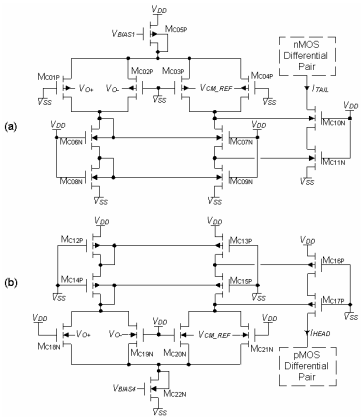

Figure 8. Proposed (a) nMOS driven CMFB and (b) pMOS driven CMFB

These proposed CMFB circuits are simply the same as Fig. 7(b) with the bulk-driven differential pairs and current mirrors included. M_{C05P} and M_{C22N} are added extra to improve the input range of operation, which is the output range of the core OTA. Simulation results of this proposal are shown in Fig. 9.

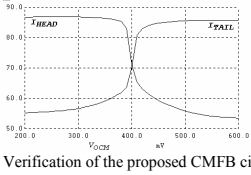

Figure 9. Verification of the proposed CMFB circuit

The simulation results shown in Fig. 9 imply that the bulk-driven technique can also be a strong candidate for low-voltage CMFB design.

C. Supply-Independent Bias Circuit

The supply independent bias circuit presented in [6], as shown in Fig. 10(a), can be operated at a minimum supply voltage of $V_{T0}+2V_{DSsat}$. This is very suitable for low-voltage systems and therefore applied for generating V_{BIAS1} and V_{BIAS4}. For generating V_{BIAS2} and V_{BIAS3}, which have to be less than V_{T0}, bulk-driven devices can be utilized as shown in Fig. 10(b).

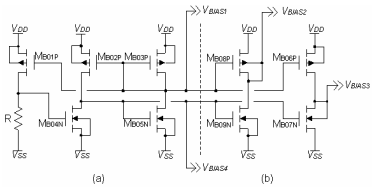

Figure 10. (a) Using the supply-independent bias circuit presented in [6] for generating V_{BIAS1} and V_{BIAS4} and (b) bias voltage generator for V_{BIAS2} and V_{BIAS3}

Simulation results of Fig. 10 are illustrated in Fig. 11.

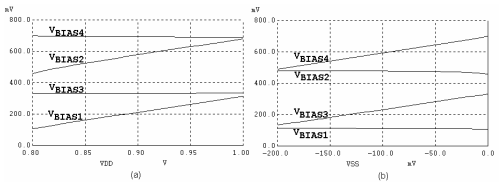

Figure 11. Effects of bias voltages with respect to (a) VDD and (b) VSS

As expected and seen in Fig.11, V_{BIAS1} and V_{BIAS2} are independent of *VSS* and therefore suitable for biasing pMOS devices. Similarly, V_{BIAS3} and V_{BIAS4} are independent of *VDD* and therefore suitable for biasing nMOS devices.

D. Simulation Results

Alcatel's 0.35µm CMOS twin-well technology was used to verify the proposal. The open-loop gain and the phase margin of the OTA with a load capacitance of 5pF is depicted in Fig. 12. The overall OTA characteristic is shown in Table I.

CONCLUSION

This paper explored the approach of low-voltage OTA design using the bulk-driven technique. The observed advantages are:

- As previously pointed out by [3], bulk-driven differential-pairs can provide rail-to-rail ICMR operation, and bulk-driven current mirrors can be operated with less voltage headroom consumption.
- With the use of bulk- and gate-biased cascodes, the output resistance of a folded-cascode fully differential OTA can be increased with no additional circuit or extra power consumption.
- Bulk-driven CMFB can sense the input common-mode voltage smaller than the threshold voltage.

In summary, the bulk-driven technique has been shown to be a serious contender for low-supply voltage amplifier design.

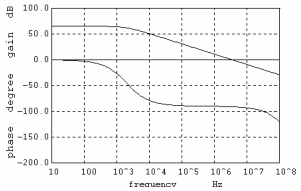

Figure 12. Plots of open-loop gain and phase margin

TABLE I. SUMMARY OF OTA PERFORMANCE

Characteristics	Simulated Value
Open-loop DC gain	66dB
Unity gain-bandwidth	3.4MHz
Total current consumption	243µA
Phase margin	>80°
Differential output voltage swing	1V
Slew rate	SR+=4.7V/µs, SR-=5.1V/µs
ICMR	0.8V
VDD = 0.8V, VSS=0V, V_{ICM} = 0.4V, C_L = 5pF	

REFERENCES

[1] S. S. Rajput and S. S. Jamuar, "Low Voltage Analog Circuit Design Techniques" *Circuits and Systems Magazine, IEEE*, Volume: 2, Issue: 1, pp. 24-42, 2002.

[2] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, Second Edition, 2002, ISBN 0-19-511644-5

[3] B. J. Blalock, P.E. Allen and G. A. Rincon-Mora, "Designing 1-V Op Amps Using Standard Digital CMOS technology," *IEEE Trans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, Vol. 45, No. 7, July 1998.

[4] J. Rosenfeld, M. Kozak, and E.G. Friedman, " A 0.8 Volt High Performance OTA Using Bulk-Driven MOSFETs for Low Power Mixed-Signal SOCs", *SOC Conference, 2003 Proceedings, IEEE International [Systems-on-Chip]*, pp. 245-246, 17-20 September 2003

[5] S. Terry, B. J. Blalock, L. Yong, B. Dufrene and M. Mojarradi, "Complementary Body Driving – A Low Voltage Analog Circuit Technique for SOI," *SOI Conference*, *IEEE International 2002*, pp.80-82, 7-10 Oct. 2002

[6] Z. Dong and P. E. Allen, "Low-Voltage, Supply Independent CMOS Bias Circuit," *The 2002 45th Midwest Symp. on Circuits and Systems (MWSCAS 2002)*, Vol. 3, pp.568-570, 4-7 Aug. 2002

[7] B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw Hill, International Edition, 2001, ISBN 0-07-118839-8

A New Bulk-Driven Input Stage Design for Sub 1-Volt CMOS Op-Amps

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***Abstract*— This paper presents a new design approach for a rail-to-rail bulk-driven input stage using a standard single-well (n-well in this paper) CMOS technology. This input stage can provide nearly constant transconductance and constant slew rate over the entire input common-mode voltage, operating with a wide supply voltage ranging from sub 1-volt (V_{T0}+3V_{DSsat}) to the maximum allowed for the CMOS process, as well as preventing latch-up.**

I. INTRODUCTION

Lowering of the supply voltage in portable electronics has always been a priority for many years, as it allows reduction in the number of battery cells rendering the products more compact and light, and leading to decreased power consumption of the digital circuits. However, in analog circuits, particularly op-amps in unity-gain configuration, lowering the supply voltage degrades the signal-to-noise ratio. As a consequence, those op-amps require rail-to-rail input and output stages.

For the input stage, it is essential that its effective transconductance (g_m) is nearly constant over the rail-to-rail Input Common-Mode Range (ICMR), as the large variation introduces signal distortion and creates difficulty in the frequency compensation of the multi-stage op-amps [1], [7]. Traditionally, complementary differential pairs are used to achieve the rail-to-rail operation, and the tail current is controlled with current switches to keep the g_m constant [1]. However, the mobility ratio of the complementary pairs (μ_n/μ_p) is process- and temperature-dependent, causing the g_m variation to deviate by approximately 12% [2]. This motivates designers to come up with new circuit topologies using only a single type of the differential pair. Currently three candidates have been proposed – level-shifting [2], floating-gate [3], and the bulk-driven [4] techniques.

At the present time, the bulk-driven technique is probably the least popular, since the transconductance of a bulk-driven MOSFET (g_{mbs}) is dependent on the bulk-to-source voltage (V_{BS}). The level-1 model of the g_{mbs} is given by:

$$g_{mbs} = \gamma\,(2\beta I_{DS})^{0.5} / 2\,(2|\Phi_F| - V_{BS})^{0.5} \qquad (1)$$

where γ is the bulk-threshold parameter, β is the small-signal transconductance parameter, I_{DS} is the drain current, and $2|\Phi_F|$ is the surface potential. The g_{mbs} is typically only 20-40% of the gate-driven transconductance [4]. However, the beauty of a bulk-driven MOSFET is that it removes the threshold voltage constraint. This property makes the bulk-driven approach worthy of development to improve its performance.

So far three proposals are available for improving the g_m variation of the Bulk-Driven Differential Pair (BDDP) – the complementary BDDP [5], the Replica-Biased Scheme (RBS) [5], and the feedback techniques [6]. The complementary BDDP technique utilizes the complementary behavior of the pairs to reduce the g_m variation. However, a special CMOS technology (e.g. a twin-well process) is required for the implementation. The RBS, as illustrated in Fig. 1, biases the gates of the pair to keep V_{BS} = 0 so that the g_{mbs} becomes constant. The problem is, however, V_{BS} = 0 means $V_B = V_S$, and it is impossible for the source-coupled voltage to swing rail-to-rail. Thus the g_m is constant over only a portion of the rail-to-rail ICMR. The feedback technique senses the input common-mode voltage (V_{ICM}) and adjusts the tail current to reduce the g_m variation; however, this causes the Slew Rate (SR) to become V_{ICM} dependent.

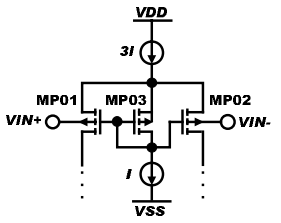

Figure 1. The bulk-driven RBS proposed in [5]

This paper presents a new bulk-driven rail-to-rail input stage using a standard single-well (n-well in this paper) CMOS process. This input stage achieves almost constant-g_m and constant-SR, working with a wide supply voltage

ranging from sub 1-volt (V_{T0}+3V_{DSsat}) to the maximum allowed by the CMOS process, and also diminishes the latch-up likelihood.

II. The New Bulk-Driven Input Stage

A. Topology

The idea of our bulk-driven input stage comes from utilizing two pairs of the RBS to cover all portions of the rail-to-rail ICMR. Fig. 2 illustrates the topology of our approach, which we call the Bulk-Driven Double Replica-Biased (BDDRB) input stage.

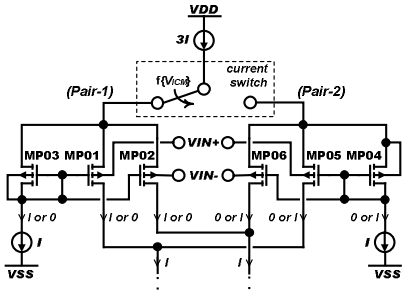

Figure 2. Topology of the BDDRB input stage

The BDDRB input stage consists of pair-1 (MP01~MP03) and pair-2 (MP04~MP06), which are assigned for the low and high portions of the ICMR, respectively, and a current switch.

The device sizes of pair-1 are all the same, and the same dc current runs through each device when the pair is selected. This leads MP03 to be the replica of the input pair, and $V_{BS1,2}$ to be equal to V_{GS3} (= constant). The same argument goes to pair-2 except that $V_{BS5,6}$ would be zero instead. The pair-1 would be operational for the ICMR between VDD-V_{SDsat}-V_{SG3} and VSS+V_{DSsat}, and for pair-2 the operational range would be between VDD-V_{SDsat} and VSS+V_{DSsat}+V_{SG4}. To maximize the ICMR a current switch is implemented so that the effective ICMR would be between VDD-V_{SDsat} and VSS+V_{DSsat}.

B. Principle of Operation

Fig. 4(a) illustrates how the BDDRB input stage can be realized as a transistor circuit. Again, MP01~MP03 (pair-1) and MP04~MP06 (pair-2) are the replica-biased input pairs for the low and high portions of the ICMR, respectively. MP09~MN12 form a current switch and work as a function of V_{ICM}. This input stage is configured such that it normally operates with pair-1. When V_{ICM} becomes high and causes V_{SG9} to be greater than the threshold voltage ($|V_{T0}|$), the switch deactivates pair-1 and activates pair-2 instead. Conversely, when V_{ICM} becomes low and causes $V_{SG9} < |V_{T0}|$, pair-1 turn on and pair-2 turns off. The bias-voltage, V_{SWITCH}, controls the crossover voltage between the two points.

To verify the operation of the BDDRB input stage, it was necessary to implement it in an op-amp. For this we chose a folded-cascode two-stage op-amp, as illustrated in Fig. 4(b), to present as an application example.

III. Simulation Results

Using the BSIM3 MOSFET models of a 0.18µm CMOS process, we simulated the op-amp of Fig. 4 with a supply voltage of 0.8-volt and a load resistance and capacitance of 1MΩ and 5pF, respectively. Table I shows the summary of the simulation results.

TABLE I. Simulation Results of the Overall Performance of the Op-amps in Figure. 4

Characteristics	Simulated Results
Open-loop DC gain	60dB
Unity-gain frequency	0.6MHz
Phase margin	58°
ICMR	0.6V
Total current consumption	61~74µA (V_{ICM} dependent)
SR	SR+ = 1.0V/µs, SR- = -0.5V/µs
Output voltage swing	0.6V
Common-mode rejection ratio	63dB (when V_{ICM} = 0.5(VDD+VSS))
Power Supply Rejection Ratio (PSRR)	PSRR+ = 58dB, PSRR- = 79dB
Input referred noise voltage	146~169nV/√Hz (white noise only, V_{ICM} dependent)
Total harmonic distortion, A_{VCL}=+1V/V	0.014% (-77.1dB) for 0.6Vp-p, 1kHz sine wave 0.093% (-60.6dB) for 0.6Vp-p, 10kHz sine wave
Measurement condition: VDD = 0.8V, VSS = 0V, C_L = 5pF, R_L=1MΩ	

The simulation confirmed the rail-to-rail ICMR operation (VDD-$V_{SDsat14}$ to VSS+$V_{Dssat07}$ precisely). Fig.3 and Fig. 5 show the simulation results of the open-loop gain frequency response and the effective tail current of the op-amp in Fig. 4, which indicate that both characteristics are nearly V_{ICM} independent. Fig. 6 gives the simulation results of the effective transconductance [g_m(eff)] of the op-amp versus V_{ICM}.

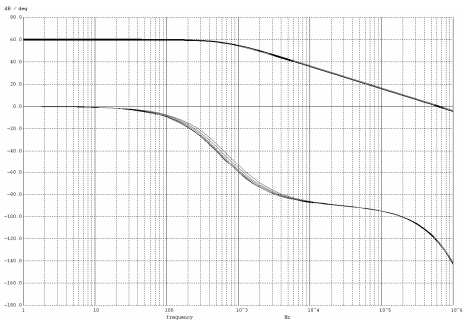

Figure 3. Simulated frequency response of the op-amps for V_{ICM} varying from 0.1 to 0.7V with a 0.1V step

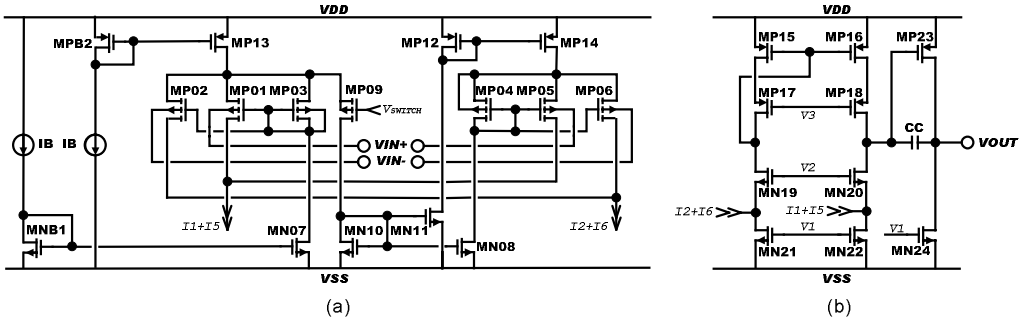

Figure 4. An application example of the BDDRB input stage in a folded-cascode two-stage op-amps (a) the BDDRB input stage, and (b) a folded-cascode two-stage op-amps

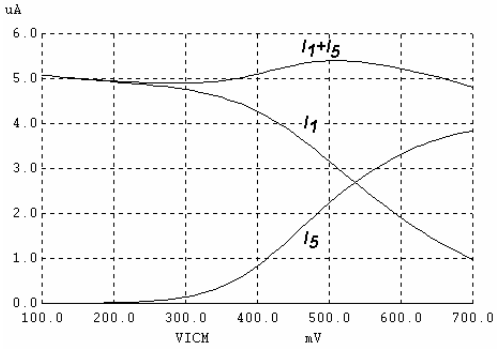

Figure 5. Simulated tail current vs V_{ICM}

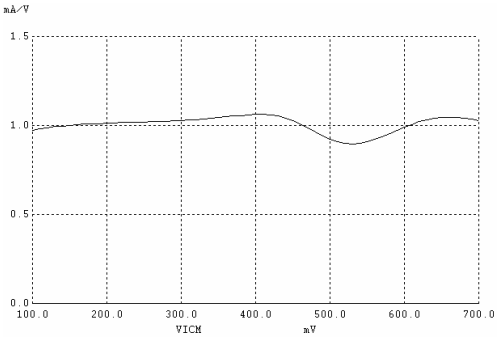

Figure 6. Simulated g_m(eff) vs V_{ICM}

Fig. 6 indicates that the g_m variation is approximately 10% over the rail-to-rail ICMR operation. This variation peaks at the transition point between the two pairs, i.e. when the pairs are partially on and off. It is worth noting that the source-to-bulk voltage of the input pairs (V_{SB1} and V_{SB5}) change at the transition stage, which should also have created a major impact in the g_m variation according to (1). Fig. 7 shows the simulation results of V_{SB1} and V_{SB5} versus V_{ICM}.

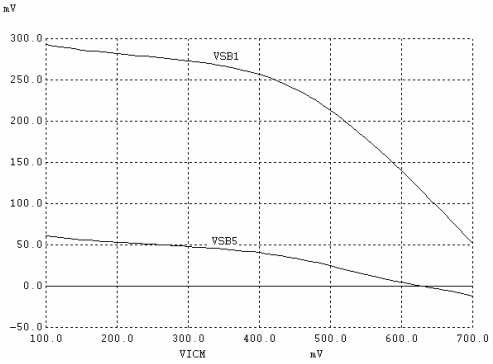

Figure 7. Simulated V_{SB1} and V_{SB5} vs V_{ICM}

IV. ADVANTAGES AND DISADVANTAGES

An important practical advantage of the BDDRP input stage is that it requires no special CMOS process. Other advantages are g_m(eff) and SR of the op-amp remain relatively constant with respect to V_{ICM}, and the circuit prevent latch-up. Conventional BDDP techniques require very low supply voltages, otherwise the rail-to-rail ICMR operation would cause the bulk terminals to be strongly forward-biased. With the BDDRB input stage, the bulk-to-source voltages remain as the same condition as the replica device regardless of the supply voltage condition. For confirmation, we simulated the circuit of Fig. 4 with a 3-volt power supply and observed that the rail-to-rail ICMR operations did not result in any significant input current or substantial forward-biased pn junctions.

However, in comparison to previously mentioned bulk-driven techniques, our proposal increases input referred

noise. Previously mentioned bulk-driven techniques utilize the depletion-mode characteristics of a MOSFET so that the input pair can be always on for rail-to-rail. In contrast, our input stage has two pairs connected in parallel, and except in the transition stage one of the pair is off. The off-pair contributes additional thermal noise, as it is inversely proportional to g_{mbs} [11].

Another drawback to previously mentioned bulk-driven techniques is the increase in input capacitance, since two input pairs are utilized in our proposal. The input capacitance of a bulk-driven MOSFET consists of C_{bsub} and C_{bs}, where C_{bsub} is the well-to-substrate capacitance and C_{bs} is the bulk-to-source capacitance. C_{bsub} depends on layout design, and a detail description is given in [4]. C_{bs}, on the other hand, can be controlled by circuit designers to some extent as it is directly related to its source-to-bulk voltage. Reducing the forward-bias of the bulk-terminal results in decreased C_{bs} as well as increased input resistance. With the BDDRB input stage, this can be easily achieved by decreasing the source-to-bulk voltage of the replica device (V_{SB3} of Fig 4(a), which is equivalent to V_{SG3}). Fig. 8 illustrates the simulation results of the input impedance measurements for the op-amp shown in Fig. 4.

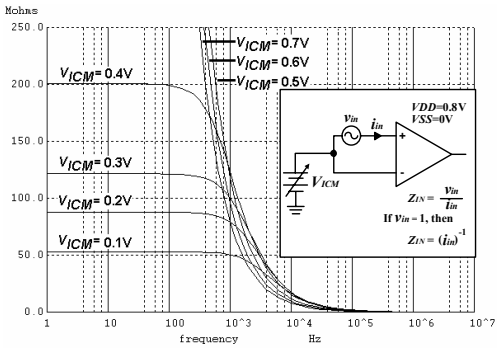

Figure 8. Simulation results of the circuit-level input impedance characteristic

V. CONCLUSION

A new approach for the bulk-driven input stage called BDDRP to achieve rail-to-rail ICMR operation has been presented. This approach leads the operational supply voltage to be from under 1-volt to the maximum allowed by the CMOS process used, as well as diminishing the latch-up problem. SPICE simulations indicate that the g_m is nearly constant (within 10%) over the entire ICMR whilst the effective tail current remains almost unchanged. The additional hardware implemented to achieve this performance is only a replica circuit for each pairs and a current switch.

REFERENCES

[1] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-*gm* rail-to-rail input stage," *IEEE Proc. ISCAS '92*, vol. 6, pp. 2876-2879, May 1992

[2] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. of Solid-State Circuits*, vol. 38, no. 8, August 2003

[3] J. Ramirez-Angulo, S.C. Choi, and G. Gonzalez-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 971-974, Nov. 1995

[4] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[5] B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-driving as a low-voltage analog design technique for CMOS technology," *IEEE Southwest Symp. on Mixed-Signal Design (SSMSD) 2000*, pp. 113-118, February 2000

[6] F. Bahmani, S. M. Fakhraie, and A. Khakifirooz, "A rail-to-rail, constant-gm, 1-volt CMOS opamp," *IEEE Proc. ISCAS'00*, vol. 2, pp. 669–672, May 2000

[7] W.-C. Wu, W. J. Helms, J. A. Kuhn, and B. E. Byrkett, "A digital process compatible high-drive CMOS op amp with tail-to-rail input and output ranges," *IEEE J. on Solid-State Circuits*, vol. 29, no. 1, pp. 63-66, January 1994

[8] B. Razavi, "Design of analog CMOS integrated circuit," McGraw Hill, International ed., 2001

[9] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford Univeristy Press, 2nd ed., 2002

[10] S. Yan and E. Sanchez-Sinencio, "Low voltage analog circuit design techniques: a tutorial," *IEICE Trans. Analog Integrated Circuits and Systems*, vol. E00-A, no. 2, February 2000

[11] J. F. Duque-Carrillo, J. M. Valverde, and R. Perez-Aloe, "Constant-gm rail-to-rail common-mode range input stage with minimum CMRR degradation," *IEEE J. Solid-State Circuits*, vol.28, no. 6, pp. 661-666, June 1993

Bulk-Driven Flipped Voltage Follower

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***Abstract*— A voltage buffer so-called the bulk-driven flipped voltage follower is presented. This proposal is based on the Flipped Voltage Follower (FVF) technique, but a bulk-driven MOSFET with the replica-biased scheme is utilized for the input device to eliminate the DC level shift. The proposed buffer has been designed and simulated with a 0.35μm CMOS technology. The input current and capacitance of our proposal are 1.5pA and 9.3fF respectively, and with 0.8V peak-to-peak 500kHz input, the total harmonic distortion is 0.5% for a 10pF load. This circuit can operate from a single 1.2V power supply and consumes only 2.5μA.**

I. INTRODUCTION

Voltage buffers play an essential role in analog and mixed-signal circuits and processing systems, where they are widely used for driving large capacitive loads at high speeds. The ideal performance of a voltage buffer is not only to drive the large load as fast as possible but also with minimal power consumption, which means that the buffer needs to have high slew rate and low static power consumption. Today, it is evident that the Flipped Voltage Follower (FVF) proposed by R. G. Carvajal *et al* in [1] is one of the closest to the ideal voltage buffer, as many recent proposals are utilizations and/or modifications of the FVF [2]-[5].

Recently, the new version of the class-AB FVF that is free from the DC level-shift has been proposed by Ramirez-Angulo *et al* [5]. In this paper, we present a much simpler technique which can eliminate the DC level shift and convert into class AB operation, whilst preserving the advantages of the FVF approach– low-power consumption with high-power drive.

II. PREVIOUS ESSENTIAL WORKS

This section covers a brief review of voltage followers and the bulk-driven MOSFETs used in a differential pair, which we have utilized and forms the essential part of our proposal.

A. Voltage followers

Figure 1 illustrates two types of voltage followers. Figure 1(a) is the conventional type of a voltage follower, which is also known as a source follower [6]-[7]. The input device MP01 is biased with the drain current of *IREF*, therefore the gate-to-source voltage $V_{GS\,MP01}$ becomes constant if the body-effect is neglected, and therefore the output voltage V_{OUT} is equal to $V_{IN} + V_{GS\,MP01}$. Figure 1(b) illustrates the FVF, in which V_{OUT} is also shifted up by $V_{GS\,MP01}$ from V_{IN}, however, in contrast to Figure 1(a), the beauty of the FVF is that it has current sourcing and sinking capabilities at the output, which can lead to delivering both high-power driving as well as low-power consumption simultaneously.

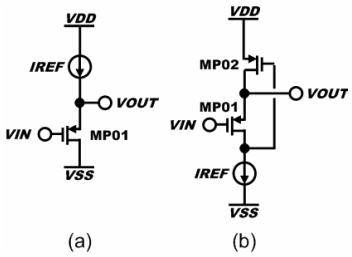

Figure 1. Voltage followers (a) common-drain amplifier (volotage follower) and (b) FVF proposed in [1]

B. Bulk-driven MOSFETs used in differential pairs

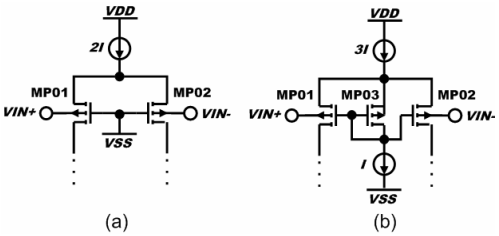

Figure 2. Bulk-driven differential pair (a) pMOS input pair and (b) the replical-biased scheme proposed in [10]

In low-voltage rail-to-rail operational amplifier designs, there exists a design technique called the bulk-driven approach. The traditional design technique for rail-to-rail operational amplifiers is the deployment of complementary differential pairs with the tail current being controlled with current switches to keep the g_m constant [8]. However, due to the fact that the mobility ratio of the complementary pairs (μ_n/μ_p) is process- and temperature dependent, causing the g_m

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variation to deviate by approximately 12% [9], there exist circuit topologies which use only a single type of the differential pair, where one of them is the bulk-driven one. Figure 2(a) illustrates a bulk-driven differential pair that uses p-type devices only.

The primary problem of Figure 2(a), however, is that the transconductance of a bulk-driven MOSFET (g_{mbs}) is dependent on the bulk-to-source voltage (V_{BS}). The level-1 model of the g_{mbs} is given by:

$$g_{mbs} = \gamma (2\beta I_{DS})^{0.5} / 2 (2|\Phi_F| - V_{BS})^{0.5} \quad (1)$$

where γ is the bulk-threshold parameter, β is the small-signal transconductance parameter, I_{DS} is the drain current, and $2|\Phi_F|$ is the surface potential.

To overcome the concern of g_{mbs} dependency over the V_{BS}, Blalock *et al* [10] proposed the Replica-Biased Scheme (RBS) as illustrated in Figure 2(b). The pMOS identified as MP03 is the replica device biasing the gates of the pair. Since the bulk of MP03 is shorted with its source, the V_{BS} of the pair is kept at zero.

We have noted the advantage from Blalock's approach namely that the condition of $V_{BS} = 0$ is kept constant, meaning $V_B = V_S$, and we chose to apply this to the FVF illustrated in Figure 1(b) to remove the DC level shift.

III. Proposed Bulk-Driven Flipped Voltage Follower

Figure 3 illustrates our proposal of the modified FVF, which we have named as "Bulk-Driven Flipped Voltage Follower (BDFVF)". As mentioned in the previous section, this is the FVF for which the input device has been modified to a bulk-driven MOSFET biased by the replica circuit to eliminate DC level shift.

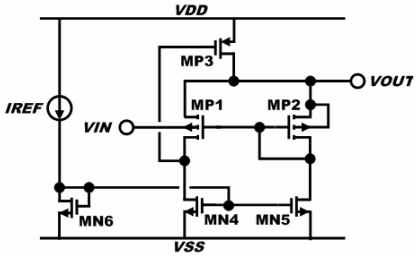

Figure 3. Bulk-driven flipped voltage follower (class-A)

The operation principle of the BDFVF of Figure 3 is very simple to follow. MP1, MP3, and MN4 form the FVF. MP1 is the input device, which its bulk is utilized to feed the input. MP2 and MN5 are the replica devices for MP1 and MN4 respectively. Note that the bulk of MP2 is physically shorted to its source, which is the output node. Since the gate of MP1 is biased with the diode-connected MP2, as well as the drain current of MP1 and MP2 are equally set to *IREF*, V_B and V_S of MP1 becomes virtually shorted (i.e. $V_{BSMP1} = 0$), and in effect the output voltage V_{OUT} becomes equal to V_{IN}.

Our proposal of Figure 3 works well, however since it is class-A type there is a limitation in its sink capability to 2*IREF*, which leads to poor pull capability in driving large loads at high speed. To overcome this problem, we have modified the circuit of Figure 3 to class-AB type as shown in Figure 4.

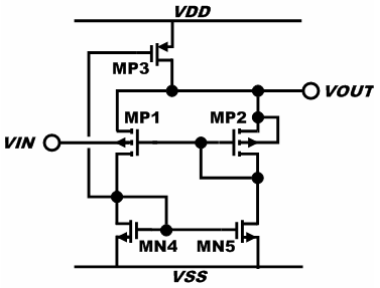

Figure 4. Proposed class-AB bulk-driven flipped voltage follower

The difference of Figure 4 from Figure 3 is that only MN4 has been modified to diode-connected instead of the constant bias to *IREF*. In this way, MP1 and MP2 can also have the same drain current and hence the replica-biased scheme remains valid. This simple change has lead to significant improvement in the sink capability of the output without the need of widening MN4 or MN5 or increasing *IREF*. In the next section, simulation results are provided.

IV. Simulated Results

A. Overall Performance

Using the BSIM3 MOSFET models of a 0.35µm CMOS process, we designed and simulated the BDFVF of Figure 4. Table I shows the simulation results summarizing the overall performance.

TABLE I. Simulation Results of the Overall Performance of the Class AB DBFVF Circuit of Figure. 4

Parameter	Simulated results
3dB frequency	2.8MHz
Total current consumption (when IL=0)	2.5µA
Slew rate (VDD=2V, VSS=0V, CL=10pF, VIN=1V↔2V)	1.9V/µs
PSRR+ / PSRR-	41.7dB / 42.0dB (dc to 100kHz)
1/*f* noise at 1kHz	880nV/√Hz
THD (Vpp=0.8V VDD=1.5V, VSS=0V, CL=10pF)	0.0747% when f=1kHz 0.0794% when f=100kHz 0.501% when f=500kHz
Input voltage range (VDD=2V, VSS=0V)	1V to 2V For offset ≤ 10mV
Load regulation	±15µA for offset ≤ 10mV
Input current	1.5pA
Input capacitance	9.3fF
Unless stated, the set up condition is: VDD=1.2V, VSS=0V, VIN=1V, CL=10pF, IL=0µA	

Figure 5 illustrates the simulated plot of V_{OUT} versus V_{IN} with the setup of *VDD* = 2V and *VSS* = 0V. The simulation

results indicate that the offset between V_{OUT} and V_{IN} was 10mV for the input range from 1V to 2V.

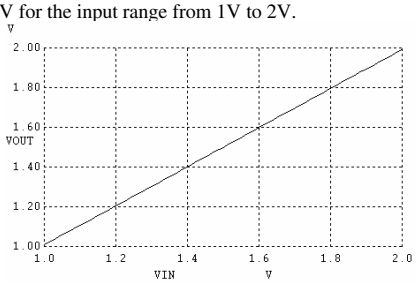

Figure 5. V_{OUT} vs V_{IN} (*VDD*=2V, *VSS*=0V)

Figure 6 illustrates the simulated plot of V_{OUT} with a sinusoidal V_{IN} input with 0.8V peak-to-peak magnitude and 500kHz frequency, and with the set up of *VDD* = 2V, *VSS* = 0V, and CL = 10pF. The simulation results indicate that the Total Harmonic Distortion (THD) was 0.5%.

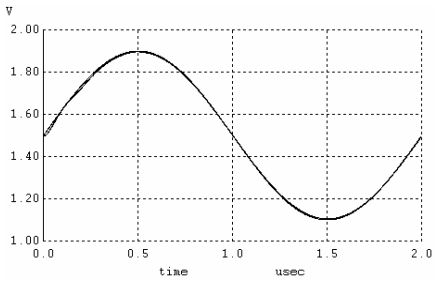

Figure 6. V_{OUT} and V_{IN} with 0.8Vpp 500kHz sinusoidal input (*VDD*=2V, *VSS*=0V, CL=10pF)

Figure 7 illustrates the simulated plot of V_{OUT} regulation capability against the load current I_L. With the setup of *VDD* = 1.5V, *VSS* = 0V, and V_{IN} =1V, the simulation results indicate that V_{OUT} kept on regulated within 10mV until the load current reaches to ±15μA.

B. Input impedance

Using bulk-driven MOSFETs in a differential pair of the operational amplifier is known to be a disadvantage in input current and capacitance [11]. In this sub-section, we present the theoretical overview as well as the simulated results to state that this disadvantage is not the case with the BDFVF.

1) Input current

With a bulk-driven MOSFET as an input device, the input signal is fed into the pn-junction of the MOSFET. The current through the pn-junction I_{Dpn} is modeled by Equation 2 [12]-[13]:

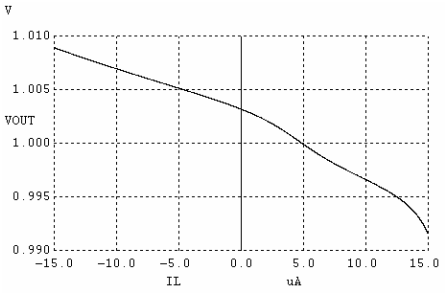

Figure 7. Load regulation (*VDD*=2V, *VSS*=0V, V_{IN}=1V)

$$I_{Dpn} = I_S \exp(V_D/V_T) \quad (2)$$

where I_s is the pn-junction current, which is also known as the scale current, when the voltage across the pn-junction V_D is zero. V_T is the thermal voltage, which is modeled as

$$V_T = kT/q \quad (3)$$

where k is the Boltzmann constant (=1.38 x 10^{-23}JK^{-1}), T is the temperature in Kelvin, and q is the charge of an electron (=1.602 x 10^{-19}C). At room temperature, V_T is approximately 26mV.

I_s can be described as in Equation 4:

$$I_s \propto A_D [(1/N_A) + (1/N_D)] \quad (4)$$

where A_D is the area of the diode junction, and N_A and N_D are the doping concentrations of the acceptors and donors respectively.

In the case of a bulk-driven differential pair, the input current is expected to be large because of the bulk being forward-biased. On the other hand for BDFVF, a large input current is not expected since the aim is to achieve a virtual short between the input and output. To affirm this theoretical consideration further, we have simulated deploying the setup used for arriving at Figure 5 to observe the offset behavior and the input current, as shown in Figure 8 and 9 respectively.

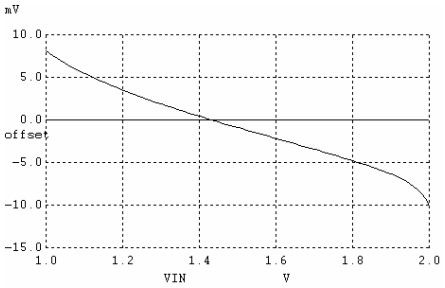

Figure 8. Offset voltage of Figure 5

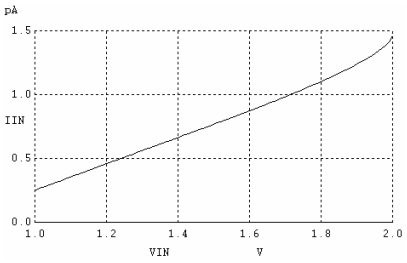

Figure 9. Input current (*VDD*=2V, *VSS*=0V)

The simulated result of Figure 9 shows that the input current remains at less than 1.5pA.

2) Input capacitance

The capacitance of the pn-junction C_j can be modeled by Equation 5 [11]-[13]:

$$C_j = C_{j0} / (1+(V_{SB}/\phi_0))^{0.5} \quad (5)$$

In the case of a bulk-driven differential pair, the input capacitance is expected to be large because of the bulk being forward-biased. On the other side for BDFVF, a large input capacitance is not expected since the aim is to achieve a virtual short between the input and output. To affirm this theoretical consideration further, we have set up the simulation condition as shown in Figure 10.

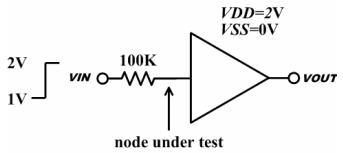

Figure 10. Simulation setup for the input capacitance

The simulated plot of the setup in Figure 10 is given in Figure 11.

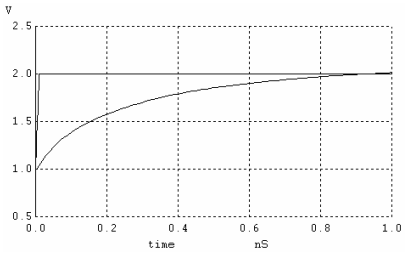

Figure 11. Simulation results for the Figure 10 setup

From Figure 11, the time constant τ was found to be 0.93ns. Hence, the input capacitance was determined as 9.3fF (τ=RC).

V. CONCLUSION

A new type of FVF called BDFVF has been presented. This proposal utilizes a bulk-driven MOSFET with the replica-biased scheme as the input device to eliminate the DC level shift. The theoretical overview of the input current and capacitance has been provided, and the simulation results showed that the input current and capacitance are in the pico-amp and femto-Farad ranges. The attractive and advantageous performances of the FVF, such as high-power driving and low-power consumption were retained. The BDFVF is a powerful block of the FVF family which is free of level shift.

REFERENCES

[1] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE trans on Circuits and Design I*, vol 52, no. 7, pp. 1276 – 1291, July 2005

[2] I. Padilla, J. Ramirez-Angulo, R. G. Carvajal, A. J. Lopez-Martin, A. Carlosena, "Compact implementation of linear weighted CMOS transconductance adder based on the flipped voltage follower*," IEEE proc. ISCAS 2006*, pp. 4281 – 4284, May 2006

[3] I. Padilla-Cantoya, J. E. Molinar-Solis, G. O. Ducoudary, "Class AB Low-Voltage CMOS Voltage Follower," *IEEE Proc. MWSCAS 2007*, pp. 887 – 890, August 2007

[4] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE trans on Circuits and Design I*, pp. 1392 – 1401, Vol 55, No. 5, June 2008

[5] J. Ramirez-Angulo, S. Gupta, R. G. Carvajal, A. J. Lopez-Martin, "New Improved CMOS Class AB Buffers Based on Differential Flipped Voltage Followers," *IEEE proc. ISCAS 2006*, pp. 3914 – 3917, May 2006

[6] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford Univeristy Press, 2nd ed., 2002

[7] B. Razavi, "Design of Analog CMOS Integrated Circuits", International Edition, McGraw-Hill, 2001

[8] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-*gm* rail-to-rail input stage," *IEEE Proc. ISCAS '92*, vol. 6, pp. 2876-2879, May 1992

[9] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. of Solid-State Circuits*, vol. 38, no. 8, August 2003

[10] B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-driving as a low-voltage analog design technique for CMOS technology," *IEEE Southwest Symp. on Mixed-Signal Design (SSMSD) 2000*, pp. 113-118, February 2000

[11] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[12] D. A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons Inc., 1997

[13] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", Fifth Edition, Oxford University Press, 2004

CMOS buffer using complementary pair of bulk-driven super source followers

Y. Haga and I. Kale

A power-efficient rail-to-rail CMOS analogue voltage buffer is presented. It consists of a complementary pair of super source followers, but a bulk-driven input device with the replica-biased scheme is utilised to eliminate the DC level shift, quasi-floating gate transistors to achieve class-AB performance, and a current switch which shifts between the complementary pair to allow rail-to-rail operation. The proposed buffer has been designed for a 0.35 μm CMOS technology to operate at a 1.8 V supply voltage. Simulated results are provided to demonstrate the total harmonic distortion for a 1.6 Vpp 100 kHz sine wave with a 68pF load is as low as −46 dB, while the static current consumption remains under 8 μA.

Introduction: Voltage buffers play a fundamental role in analogue and mixed-signal circuits and processing systems, especially for applications where the weak signal needs to be delivered to a large capacitive load without being distorted [1, 2]. To accomplish this demand, the input capacitance of the buffer needs to be as small as possible so that the weak signal is not affected under any circumstances, and the output stage needs to have a high slew-rate performance so that the signal can remain driven with large capacitive loads. Furthermore, for applications in portable electronics, where the battery lifetime needs to be extended to the maximum possible, the static power consumption of the buffer must be small while the slew-rate remains high. This suggests the use of a class-AB output stage in the buffer.

We recently proposed a CMOS buffer using a new circuit-design technique, the so-called 'bulk-driven flipped voltage follower' [3], and we demonstrated that this proposed buffer meets most of the needs mentioned above. In this Letter, we present a novel CMOS buffer based on our previous work reported in [3] which implements additional features of rail-to-rail power-efficient operation.

Class-AB bulk-driven super source follower: This Section briefly describes the previous works [1–4] using Fig. 1, which we have utilised to form the core part of our proposed CMOS buffer – a class-AB bulk-driven super source follower.

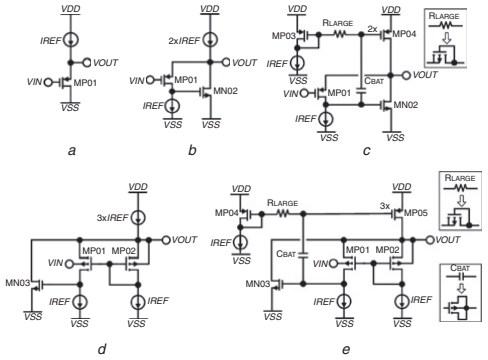

Fig. 1 *Class-A source follower (Fig. 1a), class-A super source follower (Fig. 1b), class-AB super source follower proposed by Lopez-Martín et al. [2] (Fig. 1c), class-A bulk-driven super source follower (Fig. 1d), class-AB bulk-driven super source follower using proposed QFG technique [4] (Fig. 1e)*

Fig. 1*a* illustrates a conventional pMOS source follower, widely used as a level-shifted voltage buffer [1, 2]. If the body-effect is neglected, then the output voltage *VOUT* follows the input voltage *VIN* with an upward DC shift, i.e. $VOUT = VIN + VSG_{MP01}$, where VSG_{MP01} is the source-to-gate voltage of the transistor MP01. In the case of an nMOS source follower, *VOUT* is instead shifted down from *VIN*. This conventional source follower is widely used, however the drawback is that it is sensitive to resistive loads. Since the drain current of MP01 is affected by the output current, the DC-level VSG_{MP01} cannot be kept constant. To overcome this concern, there exists a buffer which is often referred to as a super source follower [1], as shown in Fig. 1*b*. The topology of Fig. 1*b* is the same as Fig. 1*a*, but since the drain current through MP01 is biased with a constant current *IREF* and is independent of the output current, VSG_{MP01} is also held constant against the output current. Today, we can observe many published proposals using this super source follower.

Recently, López-Martín *et al.* emphasised in [2] that despite the output becoming much more insensitive to resistive loads with the super source follower, the slew-rate (SR) remains in class-A operation. In the case of a pMOS super source follower as shown in Fig. 1*b*, the positive SR is limited to *IREF*/CL, where CL is the load capacitance. Hence increasing *IREF* leads to one possible approach for SR improvement, but at a cost of greater static power consumption. To avoid this trade-off, López-Martín *et al.* proposed a class-AB super source follower [2] by using a quasi-floating gate (QFG) technique presented in [4]. Their proposed circuit diagram is depicted in Fig. 1*c*.

In Fig. 1*c*, the gate of MP04 is weakly connected to the gate of MP03 with a large resistor R_{LARGE}, and also to the gate of MN02 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow across R_{LARGE} and therefore the gate voltage of MP03 and MP04 are the same. Thus the static power dissipation between Figs. 1*b* and *c* remains the same. In terms of AC characteristics, a high-pass filter is formed with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, when observed from the gate of MN02 to the gate of MP04. Thus the AC element of the signal at the gate of MN02 can propagate to the gate of MP04, which in turn achieves class-AB operation without introducing any extra static current consumption. Furthermore, it is remarkable to realise in [2, 4] that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, which leads to achieving a low cutoff frequency $1/(2\pi R_{LARGE}C_{BAT})$ with a moderately small capacitance of C_{BAT}. In [2], López-Martín *et al.* discuss the C_{BAT} value in terms of attenuation factor α ($\simeq 1/(1 + CGS4/C_{BAT})$). A C_{BAT} greater than five times CGS4 leads to $\alpha > 0.83$, which is enough to propagate almost all frequencies except the DC component of the signal.

Fig. 1*d* illustrates the bulk-driven version of the super source follower, which is the same type of circuit-design technique we previously presented in [3]. As can be observed, the input is connected to the bulk terminal of MP01 instead of its gate. MP02 is the replica of the input device MP01, i.e. MP02 and MP01 have equal transistor sizing and are biased with the identical drain current and the gate voltage. Since the bulk-terminal of MP02 is directly shorted to its source-terminal, MP01 tends to replicate the conditions of MP02 and hence the source-terminal follows the input voltage with no DC voltage in between, thus $VOUT = VIN$. Remarkably, the input capacitance *CIN* of this type of buffer can be small because of the small junction capacitance of MP01. The junction capacitance of a MOSFET *Cj* is given by:

$$Cj = Cj0/(1 + (VSB/\Phi_0)^{0.5})$$

where *Cj*0 is the zero-bias ($VSB = 0$) junction capacitance, *VSB* is the bulk-to-source voltage, and Φ_0 is the bulk junction potential. Since *VSB* of MP01 in Fig. 1*d* is designed to be zero, the junction capacitance of MP01 is constant at *Cj*0. We discuss the simulated value of *CIN* later on in this Letter.

Fig. 1*e* shows a class-AB bulk-driven super source follower, where the class-AB operation has been implemented to Fig. 1*d* with the same technique proposed by Lopez-Martín *et al.* in [2]. However, we have chosen a modified approach for implementing the C_{BAT}. Ramírez-Angulo *et al.* [4] stated that, regarding the significance of the QFG technique, the actual value of C_{BAT} does not need to be highly accurate, as long as even a low frequency signal can be coupled. Owing to and appreciating this fact, we attempted to eliminate the need for a poly-poly capacitor, and chose to form the C_{BAT} with a MOSFET as shown in Fig. 1*e*. We observe that the size of the MOSFET five times larger than MP05 is more than enough to achieve good attenuation.

Proposed rail-to-rail class-AB CMOS buffer: We applied the bulk-driven super source follower as shown in Fig. 1*e* in our design to propose a rail-to-rail power-efficient CMOS voltage buffer. Fig. 2 illustrates the circuit diagram of our proposal.

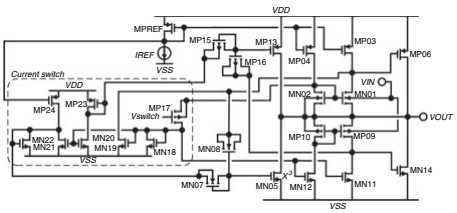

Fig. 2 *Proposed class-AB rail-to-rail CMOS analogue buffer using complementary pair of bulk-driven super source followers*

The operation principle of Fig. 2 is very simple to follow. From MN01 to MN08 and from MP09 to MP16 form an nMOS-type and pMOS-type of the bulk-driven super source follower, respectively, and from MP17 to MP24 forms a current switch. The *Vswitch* at the gate of MP17 determines the switching point between the two types of follower. When *VIN* (and thus *VOUT*) is close to *VSS* the pMOS follower is active while the nMOS follower is off, and when *VIN* moves towards *VDD*, *VOUT* and the drain voltage of MN02 also increase and eventually MP17 turns on to reduce the drain current of MN01, MN02 and MN05 (i.e. to shut off the nMOS follower) and instead to increase the drain current of MP09, MP10 and MP13 (i.e. to activate the pMOS follower) to continue the buffer operation.

Simulated results: Using a 0.35 μm CMOS process, we chose to operate the circuit of Fig. 2 at 1.8 V supply voltage and simulated with the BSIM3 MOSFET models. Table 1 shows the simulation results summarising the overall performance. From Table 1 we emphasise that the proposed buffer of Fig. 2 meets the demands we discussed in the Introduction. The input capacitance is as small as 17fF, the SR is very high such that the buffer can deliver a 1.6 Vpp 100 kHz signal with a total harmonic distortion as low as −46 dB when the capacitive load is as large as 68 pF, while the static current consumption remains under 8 μA. Also the offset voltage remains as small as 10 mV throughout the rail-to-rail operation.

Table 1: Simulated results of overall performance of Fig. 2

Parameter	Simulated results
−3 dB frequency	6 MHz
Static current dissipation	5 μA to 8 μA for *VIN* sweeping between *VDD* and *VSS*
Slew-rate	SR + = 9.3 V/μs, SR − = 13.7 V/μs
Input capacitance	17fF
Offset voltage	<10 mV for *VIN* sweeping between (*VDD* − 50 mV) and (*VSS* + 50 mV)
THD	−52 dB (1.6 Vpp at 100 kHz, CL = 10 pF) −50 dB (1.6 Vpp at 100 kHz, CL = 22 pF) −47 dB (1.6 Vpp at 100 kHz, CL = 47 pF) −46 dB (1.6 Vpp at 100 kHz, CL = 68 pF)
Simulated condition: *VDD* = 1.8 V, *VSS* = 0 V, *VSW* = 0.9 V, CL= 10 pF	

Conclusion: A new type of CMOS buffer using the complementary pair of bulk-driven super followers is presented. Utilising the bulk-driven MOSFETs with the replica-biased scheme and the QFG techniques into the buffer enabled us to have a few femto-Farad range of the input capacitance so that the weak input signals are minimally affected, while delivering the signal without much distortion even if the capacitive load is very large. The static current consumption can remain small too. Our proposed buffer can become a serious contender for portable electronics needing to deliver weak analogue signals into large capacitive loads with as little distortion as possible.

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References

1 Gray, P.R., Hurst, P.J., Lewis, H., and Mayer, R.G.: 'Analysis and design of analog integrated circuits' (John Wiley and Sons, New York, 2001, 4th edn.)
2 López-Martín, A.J., Ramírez-Angulo, J., Carvajal, R.G., and Acosta, L.: 'Power-efficient class AB CMOS buffer', *Electron. Lett.*, 2009, **45**, (2), pp. 89–90
3 Haga, Y., and Kale, I.: 'Bulk-driven flipped voltage follower'. Proc. IEEE Int. Symp. in Circuits and Systems, (ISCAS'09), 2009, Taiwan, (accepted)
4 Ramírez-Angulo, J., López-Martín, A.J., Carvajal, R.G., and Chavero, F.M.: 'Very low-voltage analog signal processing based on quasi-floating gate transistors', *IEEE J. Solid-State Circuits*, 2004, **39**, (3), pp. 434–442

Class-AB Rail-to-Rail CMOS Buffer with Bulk-Driven Super Source Followers

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***Abstract*—This paper describes a rail-to-rail CMOS analog voltage buffer designed to have extremely low static current consumption as well as high current drive capability. The buffer employs a complementary pair of super source followers, but a bulk-driven input device with the replica-biased scheme is utilized to eliminate the DC level shift, quasi-floating gate transistors to achieve class-AB performance, and a current switch which shifts between the complementary pair to allow rail-to-rail operation. The proposed buffer has been designed for a 0.35µm CMOS technology to operate at a 1.8V supply voltage. The simulated results are provided to demonstrate that the total harmonic distortion for a 1.6Vpp 100kHz sine wave with a 68pF load is as low as -46dB, whilst the static current consumption remains under 8µA.**

I. INTRODUCTION

Voltage buffers are essential building blocks in analog and mixed-signal circuits and processing systems, especially for applications where the weak signal needs to be delivered to a large capacitive load without being distorted [1-2]. To accomplish this demand, the input capacitance of the buffer needs to be as small as possible so that the weak signal is not affected under any circumstances, and the output stage needs to have a high slew-rate performance so that the signal can remain driven with large capacitive loads. Furthermore, for applications in portable electronics, where the battery lifetime needs to be extended to the maximum as possible, the static power consumption of the buffer must be small whilst the slew-rate remains high. This suggests the use of a class-AB output stage in the buffer.

The authors recently proposed a CMOS buffer using a new circuit-design technique so-called "bulk-driven flipped voltage follower" in [4], which they demonstrated that the proposed buffer meets most of the needs mentioned above. In this paper, we present a novel CMOS buffer based on our previous work in [4] but with additional features of rail-to-rail power-efficient operation to maximize the dynamic range as much as possible whilst attaining low-static high-drive current.

II. CLASS-AB BULK-DRIVEN SUPER SOURCE FOLLOWER

This section briefly describes the previous works [1-4] using Figure 1 and Figure 2, which we have utilized to form the core part of our proposed CMOS buffer – a class-AB bulk-driven super source follower.

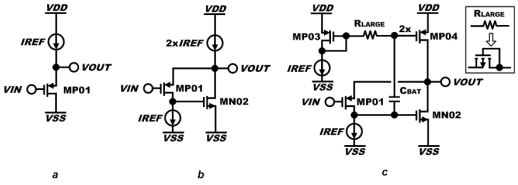

Figure 1. (a) class-A source follower, (b) class-A super source follower, and (c) class-AB super source follower proposed by Lopez-Martin *et al* [2]

Figure 1a illustrates a conventional pMOS source follower, widely used as a level-shifted voltage buffer [1-2]. If the body-effect is neglected, then the output voltage V_{OUT} follows the input voltage V_{IN} with an upward DC shift, i.e. $V_{OUT} = V_{IN} + V_{SG\text{MP01}}$, where $V_{SG\text{MP01}}$ is the source-to-gate voltage of the transistor MP01. In case of an nMOS source follower, V_{OUT} is instead shifted down from V_{IN}. This conventional source follower is widely used, however the drawback is that it is sensitive to resistive loads. Since the drain current of MP01 is affected by the output current, the DC-level $V_{SG\text{MP01}}$ cannot be kept constant. To overcome this concern, there exists a buffer which is often referred to as a super source follower [1], as shown in Figure 1b. The topology of Figure 1b is the same as Figure 1a, but since the drain current through MP01 is biased with a constant current I_{REF} and is independent of the output current, $V_{SG\text{MP01}}$ is also held constant against the output current. Today, we can observe many published proposals using this super source follower.

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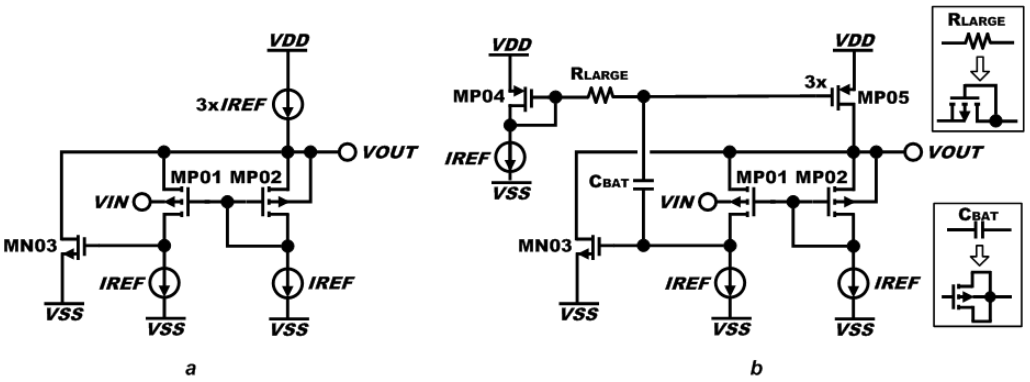

Figure 2. Bulk-driven super source followers (a) class-A operation, and (b) converting into class-AB operation using the QFG technique proposed by Ramìrez-Angulo *et al* [2-3]

Recently, A.J. Lopez-Martin *et al* emphasized in their work in [2] that despite the output becoming much insensitive to resistive loads with the super source follower, the Slew-Rate (SR) remains in class-A operation. In the case of a pMOS super source follower as shown in Figure 1b, the positive SR is limited to I_{REF}/C_L, where C_L is the load capacitance. Hence increasing I_{REF} leads to one possible approach for the SR improvement, but at a cost of larger static power consumption. To avoid this trade-off, A.J. Lopez-Martin *et al* proposed a class-AB super source follower in [2] by using a quasi-floating gate (QFG) technique presented in [3]. Their proposed circuit diagram is depicted in Figure 1c.

In Figure 1c, the gate of MP04 is weakly connected to the gate of MP03 with a large resistor R_{LARGE}, and also to the gate of MN02 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow across R_{LARGE} and therefore the gate voltage of MP03 and MP04 are the same. Thus the static power dissipation between Figure 1b and Figure 1c remains the same. In terms of AC characteristics, a high pass filter is formed with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, when observed from the gate of MN02 to the gate of MP04. Thus the ac element of the signal at the gate of MN02 can propagate to the gate of MP04, which in turn achieves class-AB operation without introducing any extra static current consumption. Furthermore, it is remarkable to realize in [2-3] that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, which leads to achieving a low cutoff frequency $1/(2\pi R_{LARGE}C_{BAT})$ with a moderately small capacitance of C_{BAT}. In [2], A.J. Lopez-Martin *et al* discuss the C_{BAT} value in terms of attenuation factor α ($\approx 1/(1+C_{GS4}/C_{BAT})$). A C_{BAT} greater than 5 times C_{GS4} leads $\alpha > 0.83$, which is enough to propagate almost all frequencies except the DC component of the signal.

Figure 2a illustrates the bulk-driven version of the super source follower, which is the same type of circuit-design technique the authors previously presented in [4]. As can be observed, the input is connected to the bulk terminal of MP01 instead of its gate. MP02 is the replica of the input device MP01, i.e. MP02 and MP01 having equal transistor sizing and are biased with the identical drain current and the gate voltage. Since the bulk-terminal of MP02 is directly shorted to its source-terminal, MP01 tends to replicate the conditions of MP02 and hence the source-terminal follows the input voltage with no DC voltage in between, thus $V_{OUT} = V_{IN}$. Remarkably, the input capacitance C_{IN} of this type of buffer can be small because of the small junction capacitance of MP01. The junction capacitance of a MOSFET C_j is given by:

$$C_j = C_{j0} / (1 + (V_{SB} / \Phi_0))^{0.5} \qquad (1)$$

where C_{j0} is the zero-bias (V_{SB}=0) junction capacitance, V_{SB} is the bulk-to-source voltage, and Φ_0 is the bulk junction potential. Since V_{SB} of MP01 in Figure 1d is designed to be zero, the junction capacitance of MP01 is constant at C_{j0}. We will discuss the simulated value of C_{IN} later on in this paper.

Figure 2b shows a class-AB bulk-driven super source follower, where the class-AB operation has been implemented to Figure 1d with the same technique proposed by A.J. Lopez-Martin *et al* in [2]. However, we have chosen a modified approach for implementing the C_{BAT}. Ramìrez-Angulo *et al* stated the significance of the QFG technique in [3] that the actual value of C_{BAT} does not need to be highly accurate, as long as even a low frequency signal can be coupled. Owing to and appreciating this fact, we attempted to eliminate the need for a poly-poly capacitor, and chose to form the C_{BAT} with a MOSFET as shown in Figure 1e. The authors observe that the size of the MOSFET five times larger than MP05 is more than enough to achieve good attenuation.

III. PROPOSED RAIL-TO-RAIL CLASS-AB CMOS BUFFER

We applied the bulk-driven super source follower as shown in Figure 2b in our design to propose a rail-to-rail power-efficient CMOS voltage buffer. Figure 3 illustrates the circuit diagram of our proposal.

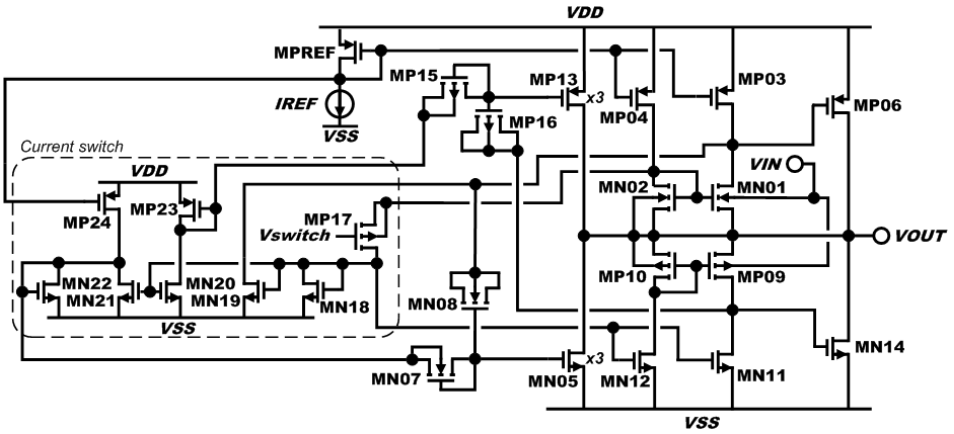

Figure 3. Proposed class-AB rail-to-rail CMOS analog buffer using a complementary pair of bulk-driven super source followers

The operation principle of Figure 3 is very simple to follow. From MN01 to MN08 and from MP09 to MP16 form a nMOS-type and pMOS-type of the bulk-driven super source follower, respectively, and from MP17 to MP24 forms a current switch. The *Vswitch* at the gate of MP17 determines the switching point between the two types of follower. When V_{IN} (and thus V_{OUT}) is close to *VSS* the pMOS follower is active while the nMOS follower is off, and when V_{IN} moves towards *VDD*, V_{OUT} and the drain voltage of MN02 also increase and eventually MP17 turns on to reduce the drain current of MN01, MN02 and MN05 (i.e. to shut off the nMOS follower) and instead to increase the drain current of MP09, MP10 and MP13 (i.e. to activate the pMOS follower) to continue the buffer operation.

IV. Simulated Results

Using a 0.35μm CMOS process, we designed to operate the circuit of Figure 3 at 1.8V supply voltage and simulated with the BSIM3 MOSFET models. Table 1 shows the simulation results summarizing the overall performance.

TABLE I. Simulated results of the overall performance of Figure 3

Parameter	Simulated Results
-3dB frequency	6MHz
Static current dissipation	5μA to 8μA for V_{IN} sweeping between *VDD* and *VSS*
Slew rate	SR+ = 9.3V/μs, SR- = 13.7Vμs
Input capacitance	17fF
THD	-52dB (1.6Vpp@100kHz, CL=10pF) -50dB (1.6Vpp@100kHz, CL=22pF) -47dB (1.6Vpp@100kHz, CL=47pF) -46dB (1.6Vpp@100kHz, CL=68pF)
Simulated condition: *VDD*=1.8V, *VSS*=0V, *VSW*=0.9V, CL= 10pF	

From Table 1 we emphasize that the proposed buffer of Figure 2 meets the demands we discussed in the Introduction. The input capacitance is as small as 17fF, the SR is very high such that the buffer can deliver a 1.6Vpp 100kHz signal with a total harmonic distortion as low as -46dB when the capacitive load is as large as 68pF, whilst the static current consumption remains under 8μA. Figure 4 is the simulated results of DC-sweeping the V_{IN}, which indicates that the offset remains small throughout the rail-to-rail operation.

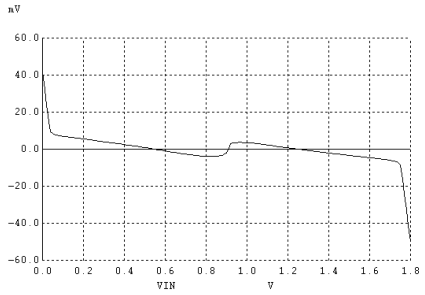

Figure 4. Simulated results of the DC offset voltage versus V_{IN} (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Fig 5 indicates the simulated results of the static current dissipation with DC sweeping the V_{IN} between *VDD* and *VSS*.

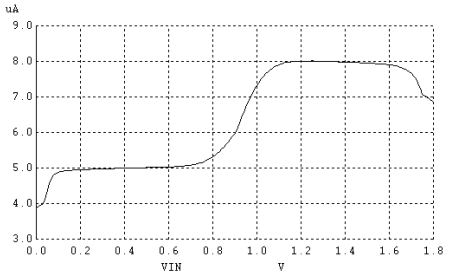

Figure 5. Simulated results of the static current dissipation (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 6 illustrates the simulated results of the V_{OUT} and the I_{OUT} with V_{IN} having 1.6V peak-to-peak 100kHz sine wave signal and a capacitive load CL of 68pF.

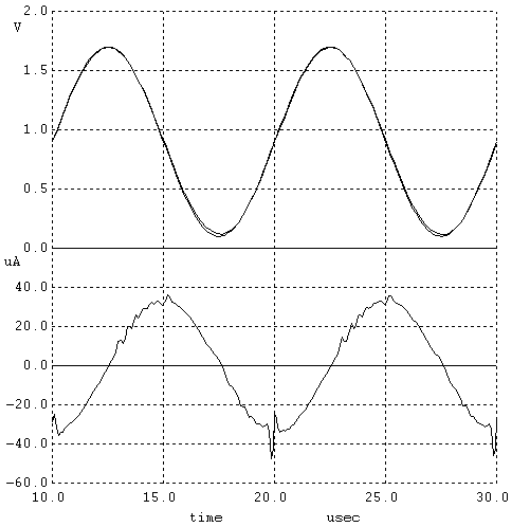

Figure 6. V_{OUT} vs V_{IN} and I_{OUT} with V_{IN} = 1.6Vpp 100kHz sinewave and CL =68pF (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 5 and Figure 6 show clearly that the goal of excellent power efficiency is achieved – during the static mode the current dissipation of the proposed buffer remains under 8μA, whereas I_{OUT} can be pushed and pulled to approximately ±40μA during the dynamic V_{IN} so that the Total Harmonic Distortion (THD) of V_{OUT} can be as small as -46dB even the CL is as large as 68pF.

To verify the input capacitance of the proposed buffer shown in Figure 3, we have set up the simulation condition as shown in Figure 7.

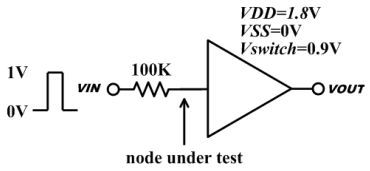

Figure 7. Simulation setup for the input capacitance

The simulated plot of the setup in Figure 7 is given in Figure 8.

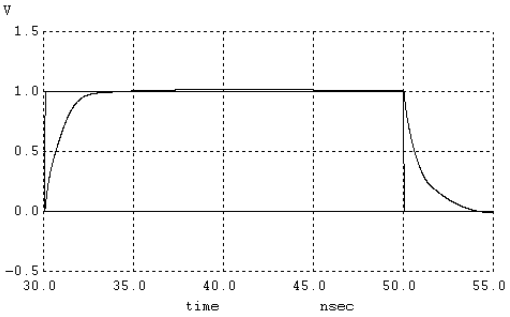

Figure 8. Simulation results for the Figure 7 setup

From Figure 8, the time constant τ was found to be 1.7ns. Hence, the input capacitance was determined as 17fF (τ=RC).

V. CONCLUSION

A new design technique for a CMOS buffer using the complementary pair of bulk-driven super followers has been presented. Applying the bulk-driven MOSFETs with the replica-biased scheme and the QFG techniques into the buffer enabled us to have a few femto-Farad range of the input capacitance so that the weak input signals are minimally affected, whilst delivering the signal without much distortion even if the capacitive load is very large. The static current consumption can remain small too. Our proposed buffer can become a serious contender for portable electronics needing to deliver weak analogue signals into large capacitive loads with as little distortion as possible.

REFERENCES

[1] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., Johnson Wiley and Sons, New York 2001

[2] A. J. López-Martin, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient Class AB CMOS Buffer", *IEE J. Electronic Letters*, 2009, 45, (2), pp. 89–90

[3] J. Ramírez-Angulo, A. J. López-Martin, R. G. Carvajal, and F. M. Chavero, "Very Low-Voltage Analog Signal Processing Based on Quasi-Floating Gate Transistors", *IEEE J. Solid-State Circuits*, 2004, 39, (3), pp. 434–442

[4] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp. 2717-2720

[5] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[6] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford Univeristy Press, 2nd ed., 2002

[7] D. A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons Inc., 1997

[8] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", Fifth Edition, Oxford University Press, 2004

Bulk-Driven Flipped Voltage Differential Pair

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***Abstract*— This paper explores a new design approach of a low-power high slew rate CMOS voltage buffer. The buffer is based on the Flipped Voltage Follower Pseudo Differential Pair, but the bulk-driven technique is utilized at the input stage to achieve rail-to-rail operation. This buffer has been designed for a 0.35µm CMOS technology to operate at a 1.8V supply voltage. The BSIM3 simulated results are provided which demonstrate the open-loop gain of 50dB, gain bandwidth of 3MHz with a 5pF load, whereas the total static current consumption remains below 9µA. This paper also addresses the issue of latch-up problem that occurs with a large step input.**

I. INTRODUCTION

Lowering of the supply voltage and the current consumption in portable electronics has been a top priority for many years, as it helps reducing the number of battery cells so that the product can be produced more compact and light. In digital circuits, lower supply voltage also leads to reduction of dynamic power consumption.

In analog circuits, particularly voltage buffers which play an essential role in analog and mixed-signal circuits, lowering the supply voltage brings a challenge in achieving acceptable dynamic range. To overcome this issue, rail-to-rail input stage would have to be adopted in the voltage buffer designs. Furthermore, lowering the static current consumption of voltage buffers causes less capability in driving large capacitive load at high speed.

There is a published proposal of a differential pair so-called Flipped Voltage Follower Pseudo Differential Pair (FVFDP) [1], which achieves high drive capability low static current consumption. Figure 1(a) and 1(b) illustrates the transistor realization of the FVFDP, and the simulated plot with I_B set to 1µA using a 0.35µm CMOS process.

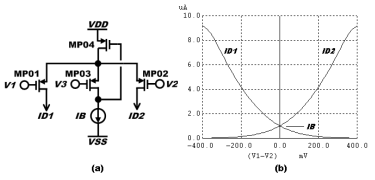

Figure 1. (a) (pMOS) FVFDP [1] and (b) simulating the DC transfer characteristics using a 0.35µm CMOS process

In Figure 1(a), V_1 and V_2 are the differential input, and V_3 is the common-mode voltage of V_1 and V_2, i.e. $(V_1+V_2)/2$. As can be observed from Figure 1(b), when no differential signal is applied (i.e. $V_1=V_2=V_3$, steady condition) the drain current of MP01 and MP02 (I_{D1} and I_{D2}) become equal to I_B, and when the differential signals are applied then I_{D1} and I_{D2} can become much larger than the twice of I_B. This low-static high-dynamic performance is not possible to achieve with the conventional differential pair.

In this paper, we present a design of a CMOS voltage buffer using the FVFDP but with the bulk-driven technique [2] applied at the input stage, so that rail-to-rail low-power high-driving performances can be all achieved.

II. BULK-DRIVEN MOSFET WITH DIODE

This section discusses utilization of a reverse-biased diode with the bulk-driven MOSFET, as the CMOS voltage buffer proposed in this paper is based on this technique. Figure 2(a) and 2(b) illustrate the circuit diagram of a bulk-driven pMOS connected with the reverse-biased diode, and a sketch of a diode realized in CMOS technology.

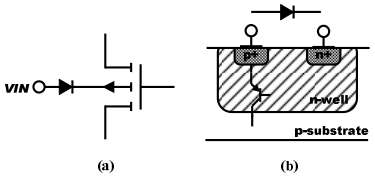

Figure 2. (a) bulk-driven pMOS with reversed-biased diode, and (b) diode in CMOS technology

Figure 4 shows the simulated plot of the DC sweep analysis of Figure 2(a) using a 0.35 µm CMOS process, where the transistor width and length are 2µm and 1.4µm, and source, drain, and gate voltages of the pMOS are fixed at 0V, -0.2V, and -0.8V respectively. For the diode the minimum size is used. As can be observed from the plot, only a few pico-ampere of the DC input current I_{IN} flows at any operation point of the input voltage V_{IN}, since the body-diode of the pMOS and the added diode are in reversely connected to each other and thus only the leakage current passes through. Consequently, the source-to-bulk voltage

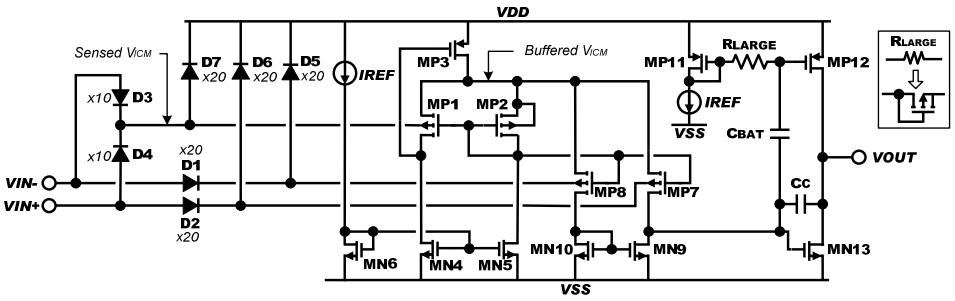

Figure 3. Proposed CMOS buffer using Bulk-Driven Flipped Voltage Differential Pair

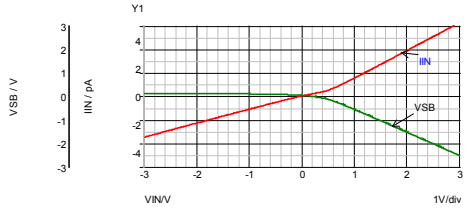

Figure 4. Simulated I_{IN} and V_{SB} of Figure 2(a)

V_{SB} of the PMOS does not become strongly forward-biased since the forward current of the diode is extremely small. It is worth noting that the added diode does not become strongly forward-biased either, so that the parasitic vertical bipolar illustrated in Figure 2(b) remains off.

Interestingly, with Figure 2(a) the input is fed into p+ implant, whereas it would have been n+ implant for a conventional bulk-driven MOSFET. This means that the input indirectly sees the pn-junction (from n-well to p-substrate), and thus the effective input capacitance can be significantly reduced.

III. Operation Principle of the Proposed Buffer

Based on the analysis shown in the previous section, we propose a CMOS voltage buffer using a new design technique which we named as Bulk-Driven Flipped Voltage Differential Pair (BDFVDP). Figure 3 illustrates the circuit diagram of the proposal.

The operation principle of the circuit in Figure 3 is simple to follow. From MP1 to MN5 form a circuit block called Bulk-Driven Flipped Voltage Follower (BDFVF) [3]. MP1 and MP2 are equally sized and biased with identical drain current with MN4 and MN5. Since the bulk-terminal of MP2 is physically shorted to the coupled source node (i.e. V_{SB2}=0), MP1 becomes the replica of MP2, and hence the source-to-bulk voltage of MP1 becomes virtually shorted (i.e. V_{SB1}≈0). In another words, the coupled source voltage follows the bulk input voltage of MP1. If MP3 is sized wide enough such that it is in linear region, then the coupled source node becomes low impedance and hence it becomes the buffered signal of the bulk input of MP1. In the design of the proposed buffer, BDFVF is utilized to buffer the common-mode signal of the differential input V_{ICM}.

From MP7 to MN10 forms the first stage of the operational amplifier. The input devices of this stage are bulk-driven, and when the differential signals V_{IN+} and V_{IN-} are in identical then the drain current of the input devices, I_{D7} and I_{D8}, settle to the bias current I_{REF}. When large differential signals are applied, then i_{D7} and i_{D8} can become much greater than twice the current of I_{REF}, since the coupled source node has very low impedance and MP3 can supply a source current that is bigger than 2 x I_{REF}.

From MP11 to MN13 forms the second stage of the operational amplifier, which has been converted to class-AB operation using the Quasi-Floating Gate (QFG) technique [4]. As can be observed, the gate of MP12 is connected to the gate of MP11 with a large resistor R_{LARGE}, and also to the gate of MN9 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow across R_{LARGE} and therefore the gate voltage of MP12 and MP11 are the same, and thus the static drain current I_{D12} is I_{REF}. In terms of AC characteristics, a high pass filter is formed at the gate of MP12 with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, and therefore MP12 achieves not only static but also dynamic operation, which in turn leads to class-AB operation. It is remarkable to realize that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, thus a low cutoff frequency can be achieved with a moderately small capacitance of C_{BAT}.

From D1 to D4 are the reverse-biased diodes to the bulk-driven devices. D3 and D4 are used to detect for V_{ICM}. In Figure 3, those diodes have been sized to 20 times of the minimum size of the diode for D1 and D2, and 10 times for D3 and D4, to prevent from further reduction of the transconductance as possible. The transconductance of a bulk-driven MOSFET with the reverse-biased diode g_{mb_VR} can be expressed as:

$$g_{mb\_VR} = \alpha\, g_{mb} \quad (1)$$

where α is the attenuation factor of the signal and g_{mb} is the transconductance of the bulk-driven MOSFET. α can be expressed as:

$$\alpha = C_{DIODE} / (C_{DIODE}+C_{SB}) \quad (2)$$

where C_{DIODE} is the junction capacitance of the reverse-biased diode, and C_{SB} is the source-to-bulk capacitance of the MOSFET. C_{DIODE} given by

$$C_{DIODE} = C_{J0\_DIODE} / (1+V_R/\phi_0)^{0.5} \quad (3)$$

where C_{J0_DIODE} is the zero-biased junction capacitance of the reverse-biased diode, V_R is the reversed-biased DC voltage, and ϕ_0 is the built-in bulk junction potential. Similarly,

$$C_{SB} = C_{J0\_MOSFET} / (1+V_{SB}/\phi_0)^{0.5} \quad (4)$$

where C_{J0_MOSFET} is the zero-biased junction capacitance of the MOSFET, and V_{SB} is the source-to-bulk DC voltage.

From D5 to D7 are the protection diodes to prevent latch up when a large step input is applied. The effectiveness of these diodes will be described in the next section.

IV. Simulated Results

To verify the proposed solution of Figure 3, we designed it using a 0.35um CMOS process to operate with a 1.8V supply voltage. This section provides simulated results using the BSIM3 MOSFET models.

A. DC-Sweep Analysis

This subsection provides the simulation results of the DC-sweep analysis. Figure 3 has been setup in a unity-gain configuration with a 1.8V supply voltage, and the input voltage V_{IN} is swept from rail to rail. Figure 5 shows the simulated behavior of the source-to-bulk voltage of the bulk-driven device MP7 V_{SB7} and the potential difference between the output V_{OUT} and V_{IN}.

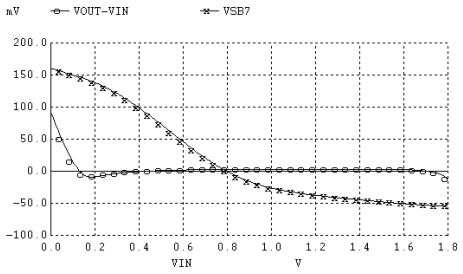

Figure 5. Simulated V_{OUT}-V_{IN} and V_{SB7} of Figure 3 in unity-gain configuration

As can be noticed from Figure 5, V_{SB7} does not become strongly forward biased which indicates that latch up does not occur, and $V_{OUT} - V_{IN}$ remains small which confirms that the proposed buffer is operational in rail-to-rail.

Figure 6 is the simulated plot of the input DC current I_{IN} of the same setup. It indicates that only ±30pA of DC current flows from rail to rail, suggesting that the input resistance would be as large as 30GΩ. This superior result is expected since the diodes are connected in reverse-bias to the body-diode of the MOSFET.

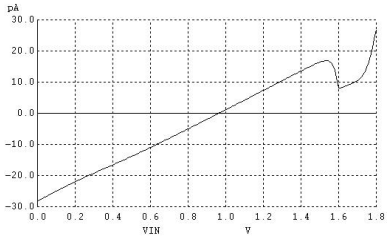

Figure 6. Simulated I_{IN} of Figure 3 in unity-gain configuration

B. Transient Analysis

This subsection provides the simulation results of the DC-sweep analysis. Figure 3 has been setup in a unity-gain configuration with a 1.8V supply voltage and a capacitive load of 5pF, and a step input from 0.2V to 1.6V and vise versa is applied. Figure 7 is the simulated plot of the input voltage v_{IN}, the output slew rate v_{OUT}, and the transient behavior of the source-to-bulk voltage of the bulk-driven device MP7, v_{SB7}. The key observation of Figure 7 is the v_{SB7} behavior when a large step-down input is applied. Appreciating to the protection capability of the diodes from D5 to D7, v_{SB7} does not even instantaneously become forward biased by more than 0.3V and therefore the latch up problem has been prevented.

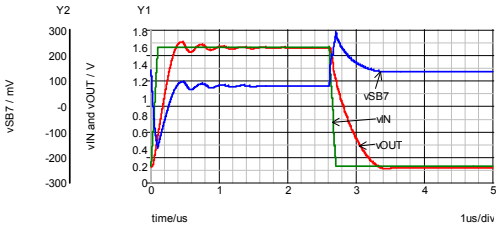

Figure 7. Simulated v_{SB7} and slew rate of v_{out} of Figure 3 in unity-gain configuration with CL=5pF (v_{IN} stepping between 0.2V and 1.6V)

Figure 8 is the simulated transient analysis plot of the input and output instantaneous current, i_{IN} and i_{OUT}, indicating that i_{IN} never achieves more than 1μA and i_{OUT} current reaches over 20μA. This suggests that the i_{IN} would always be in the nano-ampere range for an AC input slower than the Gain-Bandwidth (GBW), which proves the effectiveness of the proposed buffer. This low i_{IN} has been

achieved because the well-to-substrate capacitance is indirectly seen by the input and also the effective input capacitance has been lowered by the attenuation factor α.

Figure 8. Simulated i_{IN} and i_{OUT} of Figure 4 in unity-gain configuration with CL=5pF (v_{IN} stepping between 0.2V and 1.6V)

C. *Observation*

To further observe our proposal of Figure 3, we designed another CMOS buffer as shown in Figure 9 for comparison purposes. This circuit block is the gate-driven type of Figure 4, and all transistors are sized identical to Figure 3. Table I shows the summary of the overall performance of the two circuit blocks.

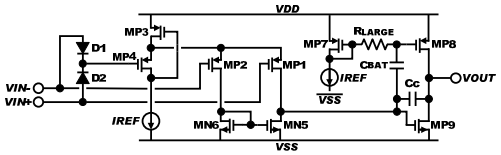

Figure 9. Gate-driven Flipped Voltage Differential Pair

As expected, the open-loop gain A_{OL} and the GBW of the bulk-driven one is smaller and slower in comparison to the gate-driven one due to reduced transconductance of the input device, however A_{OL}=50dB GBW (at CL=5pF) = 3MHz is relatively efficient for the total static current consumption of only 9µA. It is important to realize that the input referred noise of Figure 4 is moderately independent to the input condition since no transistors change the operation region. This property suggests that the single-pair approach is worthy of further improving than the double-pair approach which changes the operation region.

On the other hand, there are two significant drawbacks with our proposal. One is that the A_{OL} is not constant to V_{ICM}, where the dominant root cause is that α in Equation (1) varies significantly with the reverse voltage of the diode. The other drawback is that the Power Supply Rejection Ratio (PSRR) is substantially deteriorated, possibly due to the fact that the protection diodes D5 – D7 are directly propagating the supply noise towards the differential signal. Currently we are investigating these drawbacks to improve performances.

TABLE I. SIMULATED RESULTS OF THE OVERALL PERFORMANCE

Parameter	Simulated results	
	Figure 9	**Figure 4**
Open-loop gain A_{OL}	60dB	50dB
Gain bandwidth (GBW) at CL=5pF	9MHz	3MHz
Total static current consumption *ICC*	7µA	9µA
Power Supply Rejection Ratio (PSRR)	PSRR+=75dB PSRR-=56dB	PSRR+=26dB PSRR-=37dB
Slew Rate (SR) at CL=5pF	SR+=5.2V/µs SR-=7V/µs	SR+=5.2V/µs SR-=2.3V/µs
Input referred noise		
V_{IN}=*VDD* 1/f @1kHz	230mV/√Hz	11µV/√Hz
Wideband	70µV/√Hz	600nV/√Hz
V_{IN}=0.9V 1/f @1kHz	9µV/√Hz	15µV/√Hz
Wideband	600nV/√Hz	600nV/√Hz
V_{IN}=*VSS* 1/f @1kHz	1.5µV/√Hz	22µV/√Hz
Wideband	100nV/√Hz	600nV/√Hz
Total Harmonic Distortion (A_{CL}=1, 1.4Vpp sinewave)		
CL=5pF @100kHz	Not possible	-40dB
CL=10pF @100kHz		-33dB
CL=5pF @200kHz		-33dB
CL=5pF @300kHz		-27dB
Unless stated, the set up condition is: *VDD*=1.8V, *VSS*=0V, V_{IN}=0.9V, C_L=5pF		

V. CONCLUSION

A new low power consumption high-speed CMOS buffer has been proposed. The new circuit block consists of a FVFDP and a QFG type of class-AB second stage, which delivers high-speed at 3MHz GBW operation for a 5pF load whilst maintaining the static current consumption as small as 9µA. This paper also addresses the latch up problem by having reverse-bias connected diodes to the body diode of the bulk-driven MOSFET, so that only the diode's leakage current flows and forward biasing of the diodes can be prevented. Our proposed buffer has proven to be very power-efficient, and is motivating to work on for further improvement.

REFERENCES

[1] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE trans on Circuits and Design I*, vol 52, no. 7, pp. 1276 – 1291, July 2005

[2] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[3] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp. 2717 – 2720

[4] A. J. López-Martin, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient Class AB CMOS Buffer", *IEE J. Electronic Letters*, 2009, 45, (2), pp. 89–90

[5] B. Razavi, "Design of Analog CMOS Integrated Circuits", International Edition, McGraw-Hill, 2001

Bulk-Driven DC Level Shifter

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***Abstract*—A new CMOS DC level shifter that can be programmed at a level less than the threshold voltage of a MOSFET is proposed. This design technique utilizes a bulk-driven MOSFET, which is biased with a constant reverse voltage, to shift the input. Furthermore since the proposed block is in a class-AB super source follower form, it is power-efficient. This paper presents the design and the simulation of the proposed block and also its application in a simple current mirror using a 0.35µm CMOS process, which indicates leading to the reduction of the voltage headroom consumption of the input device but without introducing DC offset current, while the additional distortion remain negligible until 1MHz operation. The additional static current consumption is as small as 5µA.**

I. INTRODUCTION

Designing analog circuits that can operate from a low battery voltage is a challenge especially when one tries to avoid introducing performance drawbacks. Common building blocks such as current mirrors, which are widely used for biasing and as active loads in amplifiers, are no exception. To utilize current mirrors under the limited supply voltage available, designers must firstly confront the large voltage headroom consumed at the input device. One popular approach that can overcome this problem is by utilizing a DC level shifter in-between the drain and the gate of the input device [1-3]. Fig. 1 shows a couple of examples of CMOS circuit diagrams to describe this approach.

Fig. 1(a) and (b) depict a simple nMOS current mirror and utilization of a DC level shifter, respectively, and Fig. 1(c) shows the simulated results of the two blocks using the BSIM3 MOSFET models of a 0.35µm CMOS process. From Fig. 1(c), it is clear that a significant offset in the DC current is observed for Fig. 1(b). This is because the circuit block formed by MP3 and *IB* generates a DC level shift upward by more than the threshold voltage of MP3 and causes MN1 to leave the saturated region and enter into the linear region. To avoid this undesirable side effect, a DC level shifter that can be programmed to operate at a level less than the threshold voltage of a MOSFET is rather in favor of the novel technique, which to the best knowledge of the authors has not been reported in any open literature of today's circuit design techniques.

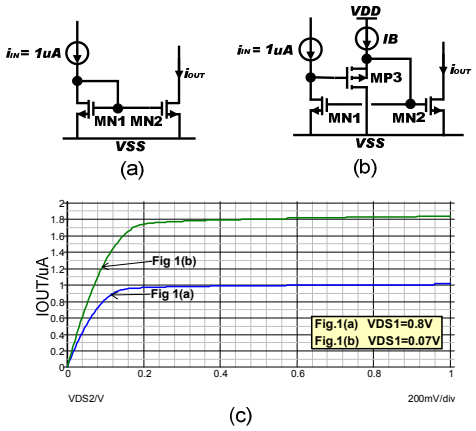

Figure 1. (a) Simple current mirror with I_{IN}=1µA, (b) with a DC level shifter, and (c) the V_{DS2} DC-sweep simulated results

In this paper we present a novel CMOS DC level shifter for which the constant DC voltage can be easily programmed to a level less than the threshold voltage of a MOSFET.

II. PREVIOUS ESSENTIAL WORKS

This section covers a brief review of the two essential design techniques, known as the Bulk-Driven Super Source Follower (BDSSF) [4] and the Quasi Floating Gate (QFG) technique [5-6], which we have utilized to come up with our novel proposal.

A. Bulk-Driven Super Source Follower (BDSSF)

Fig. 2(a) illustrates the circuit diagram of the BDSSF, which we have proposed this circuit design technique in [4] that can eliminate the DC level shift of a super source follower lectured in the literature of [7].

The operation principle of the BDSSF of Fig. 2(a) is simple to follow. MP01 is the input device, which its bulk is utilized to feed the input. MP02 and MN05 are the replica devices for MP01 and MN04 respectively. Note that the bulk

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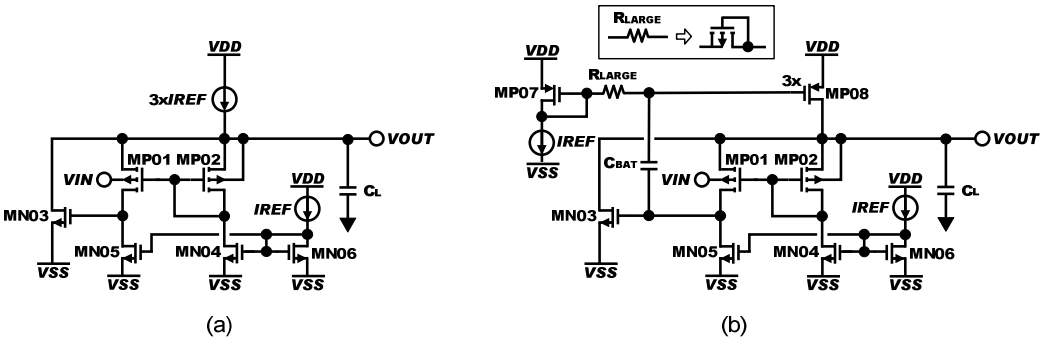


Figure 2. (a) class-A and (b) class-AB of BDSSF

of MP02 is physically shorted to its source, which is the output node. Since the gate of MP01 is biased with the diode-connected MP02, as well as the drain current of MP01 and MP02 are equally set to *IREF*, V_B and V_S of MP01 becomes virtually shorted (i.e. $V_{BS\text{MP01}} = 0$), and in effect the output voltage V_{OUT} becomes equal to V_{IN}.

B. Quasi Floating Gate (QFG) Technique

The BDSSF of Fig. 2(a) works well, however, since it is class-A type there is a limitation in its source capability to *IREF*, which leads to poor push capability in driving large loads at high speed. To overcome this problem, a circuit design technique proposed by [5] and [6], which is known as QFG, can be utilized to convert the BDSSF of Fig. 2(a) into class-AB operation. Fig. 2(b) illustrates the circuit diagram of a class-AB BDSSF.

The QFG technique utilizes RLARGE and CBAT to form a high pass filter, so that the AC element of the gate signal of the sink device MN03 can be propagated to drive the source device MP08 and therefore push capability can be expanded.

The significance of this technique is that a unity-size (i.e. the smallest size for the process) diode-connected MOSFET in the cut-off region can form a substantially large resistance RLARGE, and hence a moderately small capacitance CBAT will suffice to achieve a low cut-off frequency $1/(2\pi R_{LARGE}C_{BAT})$,\. In [6], the authors discuss the capacitance of C_{BAT} in terms of attenuation factor α ($\approx 1/(1+C_{SG8}/C_{BAT})$), where C_{SG8} is the source-to-gate capacitance of MP08. The capacitance of C_{BAT} greater than 5 times C_{SG8} leads $\alpha > 0.83$, which is enough to propagate almost all frequencies except the DC component of the signal. It is remarkable to realize that the DC performance of the circuits in Fig. 2(a) and (b) are exactly identical, i.e. to emphasize further, the QFG technique can convert from class-A to class-AB operation without introducing any extra static current consumption.

III. PROPOSAL

The design objective for this paper, which is to have a constant DC level shift less than the threshold voltage of a MOSFET, is simple to achieve by utilizing the BDSSF of Fig. 2(a) and (b). The source to bulk terminal of MP01, V_{SB1}, becomes reverse-biased by having a wider transistor width for MP01 and/or reducing its drain current I_{DS1}. The operation principle can be understood using the conventional square law model of a MOSFET. Whether the transistor size or the drain current of MP01 changes, this device maintains as the replica of MP02 and thus it operates in the saturated region. Let's suppose that MP01 is sized to have a relatively long length to minimize the effect of the channel length modulation, so that its drain current I_{DS1} can be approximated by:

$$I_{DS1} = (\mu_p C_{OX}/2)\,(W_1/L_1)\,(V_{SG1}-V_{T1})^2 \qquad (1)$$

where μ_p is the surface mobility of the pMOS transistor, C_{OX} is the capacitance of the gate oxide, W_1, L_1, V_{SG1}, V_{T1} are the width, the length, the source-to-gate voltage, and the threshold voltage of MP01, respectively. If for instance W_1 is increased and/or I_{DS1} is decreased, then the overdrive voltage $V_{SG1}-V_{T1}$ needs to be decreased to satisfy the above equation. However, since V_{SG1}, which is identical to the source-to-gate voltage of MP02, remains unchanged, V_{T1} needs to be increased. V_{T1} can be expressed by:

$$V_{T1} = V_{T0} + \gamma\,\{(2|\Phi F|+V_{SB1})^{0.5} - (2|\Phi F|)^{0.5}\} \qquad (2)$$

where V_{T0} is the zero-bias threshold voltage, γ is the body effect parameter, $|\Phi F|$ is the Fermi potential, and V_{SB1} is the source-to-bulk voltage of MP01. As can be realized from this equation, to increase V_{T1}, V_{SB1} needs to be increased. Thus in summary, increasing W_1 and/or decreasing I_{DS1} makes MP01 propagate a constant shift down voltage from the input to the output. Fig. 3 shows the simulated parametric sweep analysis of the width of MP01 and the length of MN05, denoted by W_1 and L_5, respectively (please note for clarification that the x-axis units are in μm and the y-axis ones in mV).

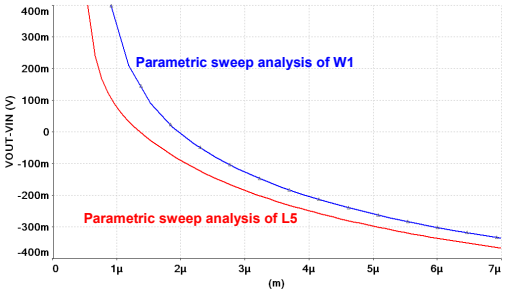


Figure 3. Parametric sweep simulation of Fig. 2(a) and (b)

It is worth noting from Fig. 3 that it is in theory feasible to level shift the input voltage upward as well as downward using the BDSSF of Fig. 2(a) and (b), however from the view point of the effective input capacitance the authors recommend keeping the bulk-driven device MP01 in reverse biased operation. The description of the reverse biased junction capacitance, which is also known as the depletion capacitance C_j, as given in [8] utilizes the following model:

$$C_j = C_{j0} / (1+(V_{SB}/\phi_0))^{0.5} \quad (3)$$

where C_{j0} is the zero-bias (V_{SB}=0) junction capacitance, V_{SB} is the bulk-to-source voltage, and ϕ_0 is the bulk junction potential. However, if the bulk of MP01 is in forward biased operation, then another capacitance model called the diffusion capacitance C_d would be introduced, which can be expressed by:

$$C_d = \tau_T (I_D/V_T) \quad (4)$$

where τ_T is the transit time of the junction diode, I_D is the amount of current through the diode, and V_T is the thermal voltage (≈26mV at room temperature). Thus in the results for the forward biased operation of the bulk-driven device, the total input capacitance C_T would then be expressed as:

$$C_T = C_j + C_d \quad (5)$$

Therefore, in order to avoid introducing the diffusion capacitance at the input, the authors recommend using the proposed level shifter by configuring the bulk-driven device in reverse bias operation, i.e. using Fig. 2(b) to shift down the voltage. For shifting up operation, the authors recommend the use of an nMOS bulk-driven transistor for the input device.

IV. Simulated Results

Table I shows the simulated results of Fig. 2(b) using the BSIM3 MOSFET models of a 0.35µm CMOS process. To see how different level shift settings and design approaches affect the overall performances, we designed several BDSSF blocks of Fig. 2(b) for comparison. The overall performance of the BDSSF blocks with 0-volt DC shift, 0.3-volt DC shift down achieved by increasing W1, 0.3-volt DC shift down achieved by decreasing I_{DS1}, 0.6-volt DC shift down effected by modifying both W1 and I_{DS1} are summarized in Table I.

Parameter	V_{shift} =0V	V_{shift} =0.3V*	V_{shift} =0.3V**	V_{shift} =0.6V
-3dB frequency	6.5MHz	8MHz	4.5MHz	5.5MHz
Total current consumption	5.2µA	5.2µA	5.2µA	5.2µA
Slew Rate+ Slew Rate-	2.0V/µs 6.2V/µs	2.1V/µs 5.3V/µs	2.1V/µs 5.0V/µs	2.2V/µs 5.5V/µs
Power Supply Rejection Ratio	53dB	55dB	62dB	62dB
1/*f* noise at 1kHz	3.7µV/√Hz	3.7µV/√Hz	3.8µV/√Hz	4.0µV/√Hz
Total Harmonic Distortion: 0.8Vpp 100kHz				
CL=10pF	-67.7dB	-66.6dB	-67.1dB	-63.6dB
CL=22pF	-62.0dB	-62.5dB	-64.1dB	-61.7dB
CL=47pF	-55.0dB	-56.7dB	-59.7dB	-58.6dB
0.8Vpp 500kHz CL=10pF	-51.6dB	-53.4dB	-48.1dB	-50.1dB
0.8Vpp 1MHz CL=10pF	-35.4dB	-38.8dB	-31.5dB	-34.4dB

* W1=3W2, L5=L6 ** W1=W2, L5=3.5L6
Unless stated, the setup condition is as follows:
VDD=3.3V, *VSS*=0V, *VIN*=2.5V, CL=10pF

TABLE I. Simulated Results of the Overall Performance of Fig. 2(b) with Different Level Shift Configurations

The simulated results for the circuit of Fig. 2(b) where the DC level shift is adjusted to 0.3V downward by modifying W1, and the input signal of 0.8Vpp at 100kHz is applied to the circuit with a load capacitance C_L of 10pF is as shown in Fig. 4.

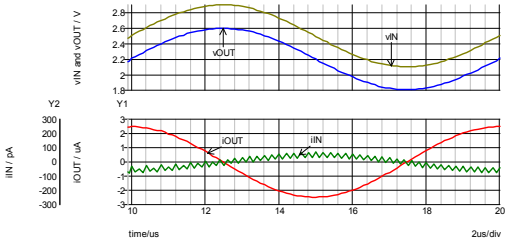


Figure 4. Simulated results of Fig. 2(b) with W1=3W2 and I_{DS1}= I_{DS2}, where v_{IN} = 0.8Vpp, 100kHz sinusoidal wave and C_L with 10pF

As can be observed from Fig. 4, the input current of only ±70pA is necessary to apply a 0.8Vpp 100kHz sinusoidal input voltage. It is worth remembering that this low input current would not have been possible to achieve if the bulk-driven input device MP01 was in the forward biased operation due to the significant increase in its input capacitance.

V. Application Example

As described in the Introduction of this paper, a DC level shifter applied in a current mirror can be useful in reducing the voltage headroom consumption of the input device. Fig. 5(a) illustrates the BDSSF of Fig. 2(b) applied in a simple pMOS current mirror. RC and CC have been added between the input and the output of the BDSSF to minimize the output overshoot against the transient input signal. Given that V_{T0} of the pMOS transistor for the 0.35µm CMOS process we have chosen is approximately 0.6V, we redesigned the BDSSF of Fig. 2(b) with a DC shift down of 0.2V, 0.5V and 0.6V and applied it to the current mirror as shown in Fig. 5(a) to compare the overall performance. Fig. 5(b) and Table II shows the simulated plots of the step response and the summary of the simulation results of Fig. 5(a), respectively.

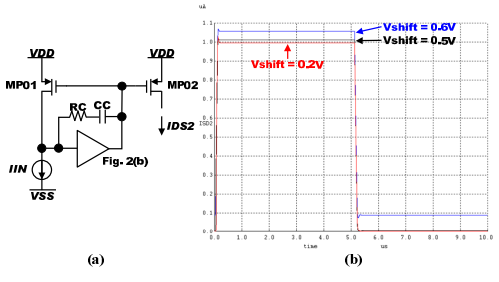


Figure 5. (a) A pMOS current mirror with level shifted BDSSF and (b) simulated plot of 1µA step response

Parameter	Fig. 5(a) without Fig. 2(b)	Fig. 5(a) with V_{shift} = 0.2V	Fig. 5(a) with V_{shift} = 0.5V	Fig. 5(a) with V_{shift} = 0.6V
Static current consumption of Fig. 2(b)	---	5.1µA	5.0µA	5.1µA
-3dB frequency	90MHz	70MHz	100MHz	100MHz
THD 1µApp 1MHz	-53.3dB	-53.6dB	-53.2dB	-57.1dB
10MHz	-41.3dB	-37.0dB	-37.2dB	-38.1dB
Setup condition: VDD=1.8V, VSS=0V, IIN=1µA, V_{D2}=VDD-0.5V				

TABLE II. Summary of the Simulation Results of Fig. 5(a)

As can be observed from Table II, until 1MHz operation none of the BDSSF adds distortion noticeably. However, as can be realized from Fig. 5(b) a caution is necessary to determine the amount of DC level shift. A DC level shift too close to V_{T0} would cause a noticeable offset in the DC current. In the case of the simulated plot of Fig. 5(b), when the level shift is almost identical to V_{T0} (=0.6V) a DC offset current of approximately 60nA and 90nA is introduced when the input current is 1µA and 0µA, respectively. Even though the level shift was approximately 100mV below V_{T0} (i.e. when the level shift is set to approximately -0.5V), the offset current of 10nA and 4nA is drawn when the input current is 1µA and 0µA, respectively. Therefore it is advisable not to set the DC level shift too close to V_{T0}.

VI. Conclusion

A novel design approach for a DC level shifter that can be programmed to a level less than the threshold voltage of a MOSFET has been presented. This technique is based on utilizing the power efficient BDSSF, with the bulk-driven input device forced to be reverse-biased to generate the constant DC voltage. SPICE simulations of the proposed block set up in a current mirror demonstrated that until 1MHz operation the proposed block does not introduce additional distortion, whilst the extra static current consumption spent is as little as 5µA. This proposed block has been shown to be an excellent solution for reducing the voltage headroom consumption of a current mirror but without introducing DC offset current.

References

[1] J. Ramírez-Angulo, "Low voltage current mirrors for built-in current sensors", *IEEE proc. ISCAS 1994*, pp. 529-532.

[2] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques", *IEEE Circuits and Systems Magazine*, 2002, issue 1, vol.2, pp. 24-42.

[3] J. Ramírez-Angulo, "Current mirrors with low input and low output voltage requirements", *IEEE proc. MWSCAS 1994*, pp. 107-110

[4] Y. Haga and I. Kale, "CMOS buffer using complementary pair of bulk-driven super source followers", *IEE J. Electronic Letters*, 2009, 45, (18), pp. 817-918.

[5] J. Ramírez-Angulo, A. J. López-Martín, R. G. Carvajal, and F. M. Chavero, "Very low-voltage analog signal processing based on quasi-floating gate transistors", *IEEE J. Solid-State Circuits*, 2004, 39, (3), pp. 434–442.

[6] A. J. López-Martín, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient class-AB CMOS buffer", *IEE J. Electronic Letters*, 2009, 45, (2), pp. 89-90.

[7] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., John Wiley and Sons, 2001.

[8] D. A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.

[9] S. Vlassis and G. Raikos, "Bulk-driven differential voltage follower", *IEE J. Electronic Letters*, 2009, 45, (25), pp. 1276-1277.

[10] Y. Haga and I. Kale, "Bulk-driven flipped voltage follower", *IEEE Proc. ISCAS 2009*, pp. 2717-2720

[11] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology", *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, 1998.

[12] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford Univeristy Press, 2nd ed., 2002.

[13] B. Razavi, "Design of Analog CMOS Integrated Circuits", International Edition, McGraw-Hill, 2001.

Appendix B Supplementary Information to Chapter 6

This appendix lists the supplementary information of the work presented in Chapter 6. The followings are included in this appendix:

- SPICE code for simulating the input capacitance
- IC layout of the whole die
- Bonding diagram
- More snapshots of the microphotograph of the fabricated device
- Test board

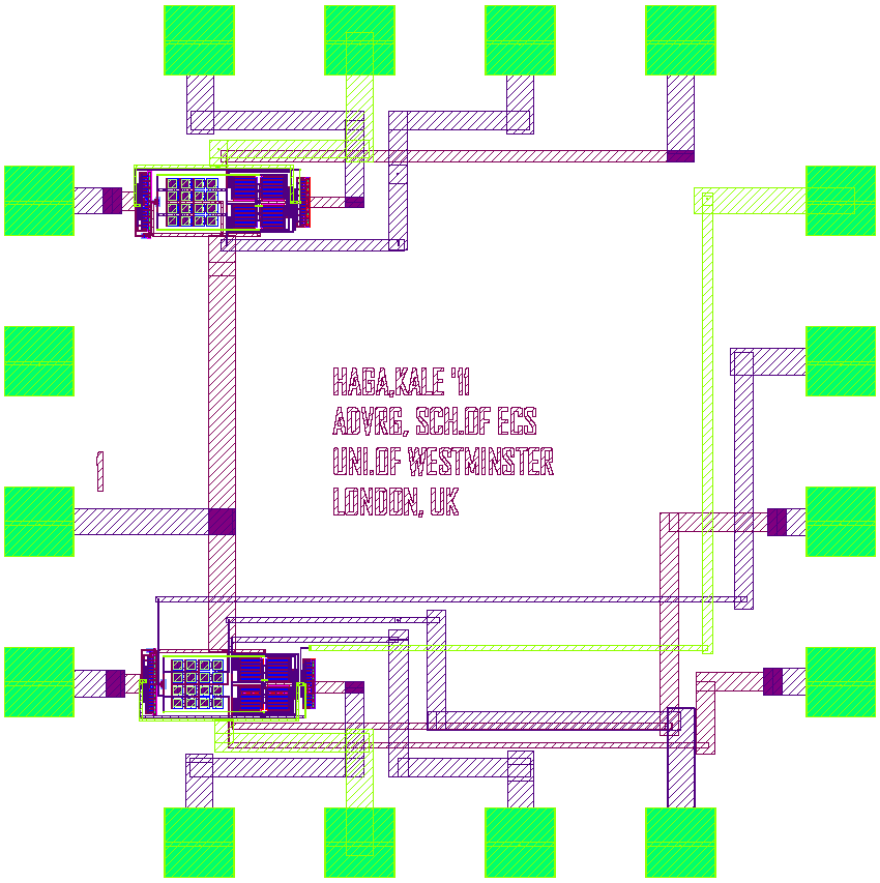
B.1 SPICE Code for Simulating the Input Capacitance

```
* Spice Script for simulating -3dB point with RIN=1meg to determine the input
capacitance
*
* ntyp.txt and ptyp.txt are the files containing BSIM3 parameters for p-type and
*n-type of MOSFET of On-Semiconductor's 0.35um CMOS process, respectively.
* buffer_monitor.spi is the file containing the extracted postlayout netlist of
*the bulk-driven buffer.
*
.lib ntyp.txt
.lib ptyp.txt
.lib buffer_monitor.spi
*
* Pin assignment
* Xbuffer_monitor INNB INNC INPB INPC INPG OUT REF VS gnd vdd buffer_monitor
********************
.control
run
let mag1s=vecmax(IN1S)-vecmin(IN1S)
let mag1o=vecmax(IN1O)-vecmin(IN1O)
let mag2s=vecmax(IN2S)-vecmin(IN2S)
let mag2o=vecmax(IN2O)-vecmin(IN2O)
let mag3s=vecmax(IN3S)-vecmin(IN3S)
let mag3o=vecmax(IN3O)-vecmin(IN3O)
let mag4s=vecmax(IN4S)-vecmin(IN4S)
let mag4o=vecmax(IN4O)-vecmin(IN4O)
let mag5s=vecmax(IN5S)-vecmin(IN5S)
let mag5o=vecmax(IN5O)-vecmin(IN5O)
let mag6s=vecmax(IN6S)-vecmin(IN6S)
let mag6o=vecmax(IN6O)-vecmin(IN6O)
let mag7s=vecmax(IN7S)-vecmin(IN7S)
let mag7o=vecmax(IN7O)-vecmin(IN7O)
let mag8s=vecmax(IN8S)-vecmin(IN8S)
let mag8o=vecmax(IN8O)-vecmin(IN8O)
let mag9s=vecmax(IN9S)-vecmin(IN9S)
let mag9o=vecmax(IN9O)-vecmin(IN9O)
print mag1s mag1o mag2s mag2o mag3s mag3o mag4s mag4o
+ mag5s mag5o mag6s mag6o mag7s mag7o mag8s mag8o
+ mag9s mag9o
plot IN1SS IN1S xunits s
plot IN1OO IN1O xunits s
plot IN2SS IN2S xunits s
plot IN2OO IN2O xunits s
plot IN3SS IN3S xunits s
plot IN3OO IN3O xunits s
```

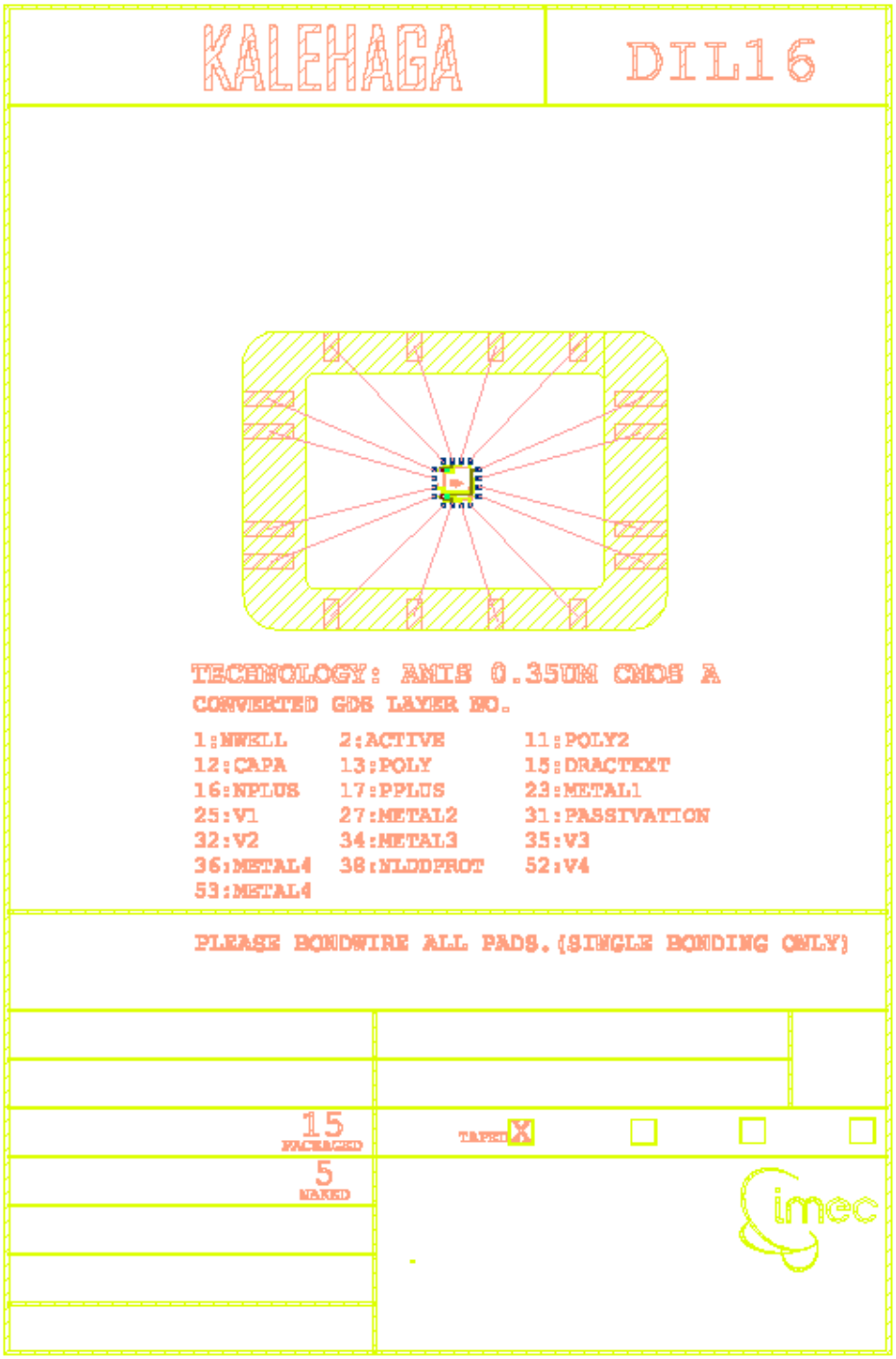
```
plot IN4SS IN4S xunits s
plot IN4OO IN4O xunits s
plot IN5SS IN5S xunits s
plot IN5OO IN5O xunits s
plot IN6SS IN6S xunits s
plot IN6OO IN6O xunits s
plot IN7SS IN7S xunits s
plot IN7OO IN7O xunits s
plot IN8SS IN8S xunits s
plot IN8OO IN8O xunits s
plot IN9SS IN9S xunits s
plot IN9OO IN9O xunits s
.endc
********************
.tran 10n 10u
********************
VDD vdd 0 DC 1
********************
********************
VIN1S IN1SS 0 DC sin(0.1 0.05 105k 10ns 0)
RIN1S IN1SS IN1S 1meg
RREF1S vdd REF1S 220k
X1S OUT1S OUT1S IN1S IN1S INPG1S OUT1S REF1S VS1S 0 vdd buffer_monitor
********************
VIN1O IN1OO 0 DC sin(0.1 0.05 114k 10ns 0)
RIN1O IN1OO IN1O 1meg
RREF1O vdd REF1O 220k
X1O OUT1O 0 IN1O 0 INPG1O OUT1O REF1O VS1O 0 vdd buffer_monitor
********************
VIN2S IN2SS 0 DC sin(0.2 0.05 113k 10ns 0)
RIN2S IN2SS IN2S 1meg
RREF2S vdd REF2S 220k
X2S OUT2S OUT2S IN2S IN2S INPG2S OUT2S REF2S VS2S 0 vdd buffer_monitor
********************
VIN2O IN2OO 0 DC sin(0.2 0.05 124k 10ns 0)
RIN2O IN2OO IN2O 1meg
RREF2O vdd REF2O 220k
X2O OUT2O 0 IN2O 0 INPG2O OUT2O REF2O VS2O 0 vdd buffer_monitor
********************
VIN3S IN3SS 0 DC sin(0.3 0.05 117k 10ns 0)
RIN3S IN3SS IN3S 1meg
RREF3S vdd REF3S 220k
X3S OUT3S OUT3S IN3S IN3S INPG3S OUT3S REF3S VS3S 0 vdd buffer_monitor
********************
VIN3O IN3OO 0 DC sin(0.3 0.05 128k 10ns 0)
RIN3O IN3OO IN3O 1meg
RREF3O vdd REF3O 220k
X3O OUT3O 0 IN3O 0 INPG3O OUT3O REF3O VS3O 0 vdd buffer_monitor
********************
VIN4S IN4SS 0 DC sin(0.4 0.05 120k 10ns 0)
RIN4S IN4SS IN4S 1meg
RREF4S vdd REF4S 220k
X4S OUT4S OUT4S IN4S IN4S INPG4S OUT4S REF4S VS4S 0 vdd buffer_monitor
********************
VIN4O IN4OO 0 DC sin(0.4 0.05 132k 10ns 0)
RIN4O IN4OO IN4O 1meg
RREF4O vdd REF4O 220k
X4O OUT4O 0 IN4O 0 INPG4O OUT4O REF4O VS4O 0 vdd buffer_monitor
********************
VIN5S IN5SS 0 DC sin(0.5 0.05 123k 10ns 0)
RIN5S IN5SS IN5S 1meg
RREF5S vdd REF5S 220k
X5S OUT5S OUT5S IN5S IN5S INPG5S OUT5S REF5S VS5S 0 vdd buffer_monitor
********************
VIN5O IN5OO 0 DC sin(0.5 0.05 136k 10ns 0)
RIN5O IN5OO IN5O 1meg
RREF5O vdd REF5O 220k
X5O OUT5O 0 IN5O 0 INPG5O OUT5O REF5O VS5O 0 vdd buffer_monitor
********************
VIN6S IN6SS 0 DC sin(0.6 0.05 126k 10ns 0)
RIN6S IN6SS IN6S 1meg
RREF6S vdd REF6S 220k
X6S OUT6S OUT6S IN6S IN6S INPG6S OUT6S REF6S VS6S 0 vdd buffer_monitor
********************
VIN6O IN6OO 0 DC sin(0.6 0.05 139k 10ns 0)
RIN6O IN6OO IN6O 1meg
RREF6O vdd REF6O 220k
X6O OUT6O 0 IN6O 0 INPG6O OUT6O REF6O VS6O 0 vdd buffer_monitor
********************
VIN7S IN7SS 0 DC sin(0.7 0.05 128k 10ns 0)
RIN7S IN7SS IN7S 1meg
```

```
RREF7S vdd REF7S 220k
X7S OUT7S OUT7S IN7S IN7S INPG7S OUT7S REF7S VS7S 0 vdd buffer_monitor
********************
VIN7O IN7OO 0 DC sin(0.7 0.05 142k 10ns 0)
RIN7O IN7OO IN7O 1meg
RREF7O vdd REF7O 220k
X7O OUT7O 0 IN7O 0 INPG7O OUT7O REF7O VS7O 0 vdd buffer_monitor
********************
VIN8S IN8SS 0 DC sin(0.8 0.05 126k 10ns 0)
RIN8S IN8SS IN8S 1meg
RREF8S vdd REF8S 220k
X8S OUT8S OUT8S IN8S IN8S INPG8S OUT8S REF8S VS8S 0 vdd buffer_monitor
********************
VIN8O IN8OO 0 DC sin(0.8 0.05 140k 10ns 0)
RIN8O IN8OO IN8O 1meg
RREF8O vdd REF8O 220k
X8O OUT8O 0 IN8O 0 INPG8O OUT8O REF8O VS8O 0 vdd buffer_monitor
********************
VIN9S IN9SS 0 DC sin(0.9 0.05 116k 10ns 0)
RIN9S IN9SS IN9S 1meg
RREF9S vdd REF9S 220k
X9S OUT9S OUT9S IN9S IN9S INPG9S OUT9S REF9S VS9S 0 vdd buffer_monitor
********************
VIN9O IN9OO 0 DC sin(0.9 0.05 130k 10ns 0)
RIN9O IN9OO IN9O 1meg
RREF9O vdd REF9O 220k
X9O OUT9O 0 IN9O 0 INPG9O OUT9O REF9O VS9O 0 vdd buffer_monitor
********************
.END
```

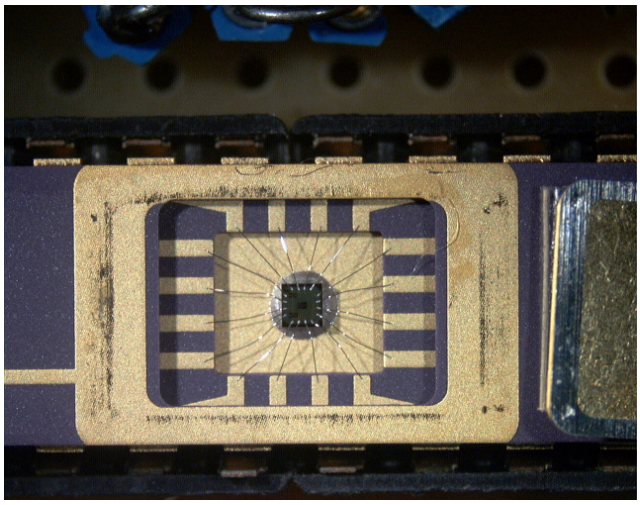
B.2 IC Layout of the Whole Die

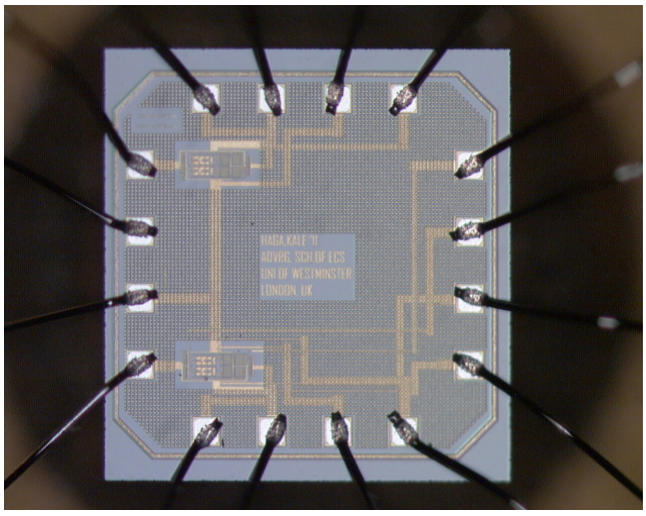


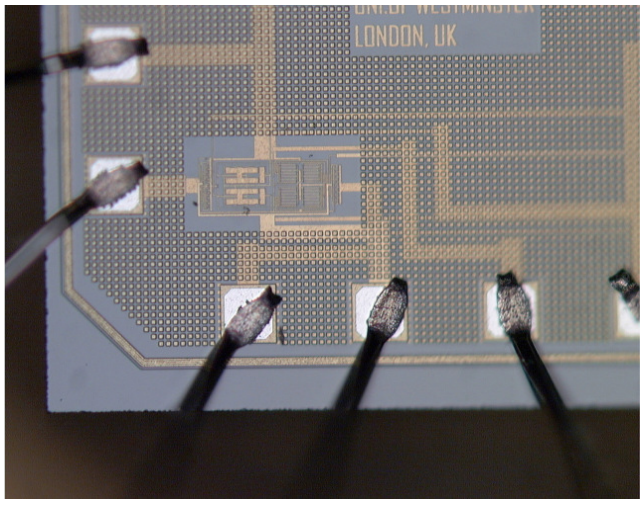
B.3 Bonding Diagram



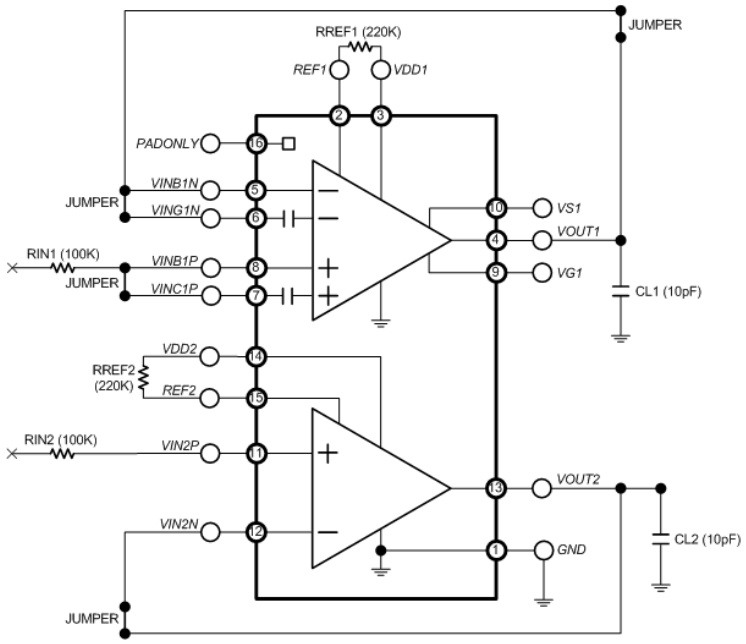
B.4 More Snapshots of the Microphotograph of the Fabricated Device

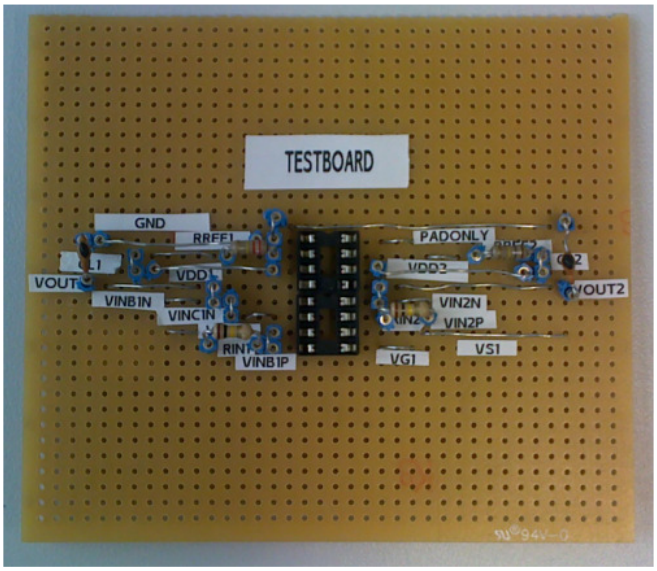






B.5 Test Board





Appendix C Logs of Measurement Data

This appendix lists all the logs of the measurement data which have been used to determine the overall input capacitance of the fabricated device described in Chapter 6. Table C-1 shown below gives the summary of the comparison between the measured and simulated results.

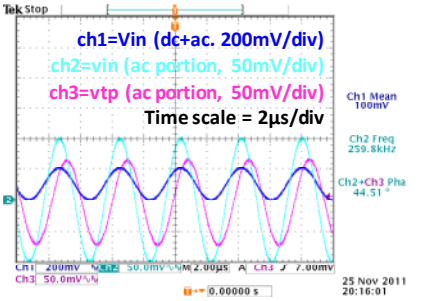
Table C-1 Comparison of the Summary of the Measurement Results to the Simulation Results

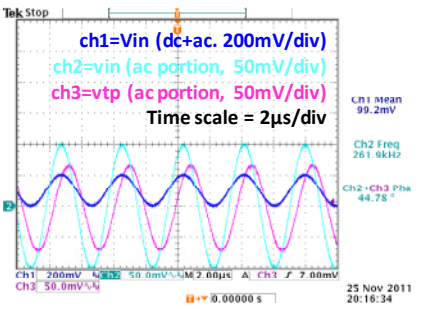
VBIAS	@ noQFG node		@ QFG node	
	Measured Results	Simulated Results	Measured Results	Simulated Results
0.1	C_Total= 1.258E-11 ± 1.7E-13 C_Stray= 1.128E-11 ± 1.7E-13 **Cin= 1.30E-12 ± 3.4E-13**	**Cin= 1.40E-12**	C_Total= 1.297E-11 ± 1.3E-13 C_Stray= use left **Cin= 1.69E-12 ± 3.0E-13**	**Cin= 1.52E-12**
0.2	C_Total= 1.267E-11 ± 1.3E-13 C_Stray= 1.124E-11 ± 1.3E-13 **Cin= 1.43E-12 ± 2.7E-13**	**Cin= 1.28E-12**	C_Total= 1.294E-11 ± 1.5E-13 C_Stray= use left **Cin= 1.70E-12 ± 2.8E-13**	**Cin= 1.41E-12**
0.3	C_Total= 1.282E-11 ± 1.1E-13 C_Stray= 1.126E-11 ± 1.3E-13 **Cin= 1.56E-12 ± 2.3E-13**	**Cin= 1.24E-12**	C_Total= 1.293E-11 ± 1.1E-13 C_Stray= use left **Cin= 1.67E-12 ± 2.3E-13**	**Cin= 1.36E-12**
0.4	C_Total= 1.255E-11 ± 1.3E-13 C_Stray= 1.125E-11 ± 1.3E-13 **Cin= 1.30E-12 ± 2.6E-13**	**Cin= 1.21E-12**	C_Total= 1.277E-11 ± 1.3E-13 C_Stray= use left **Cin= 1.52E-12 ± 2.6E-13**	**Cin= 1.33E-12**
0.5	C_Total= 1.253E-11 ± 2.3E-13 C_Stray= 1.147E-11 ± 1.2E-13 **Cin= 1.06E-12 ± 3.5E-13**	**Cin= 1.17E-12**	C_Total= 1.277E-11 ± 1.4E-13 C_Stray= use left **Cin= 1.30E-12 ± 2.6E-13**	**Cin= 1.29E-12**
0.6	C_Total= 1.213E-11 ± 1.1E-13 C_Stray= 1.121E-11 ± 1.3E-13 **Cin= 9.2E-13 ± 2.4E-13**	**Cin= 1.15E-12**	C_Total= 1.266E-11 ± 9.5E-14 C_Stray= use left **Cin= 1.45E-12 ± 2.2E-13**	**Cin= 1.26E-12**
0.7	C_Total= 1.222E-11 ± 1.3E-13 C_Stray= 1.132E-11 ± 1.3E-13 **Cin= 9.0E-13 ± 2.6E-13**	**Cin= 1.12E-12**	C_Total= 1.274E-11 ± 1.1E-13 C_Stray= use left **Cin= 1.41E-12 ± 2.4E-13**	**Cin= 1.24E-12**
0.8	C_Total= 1.232E-11 ± 1.2E-13 C_Stray= 1.125E-11 ± 1.3E-13 **Cin= 1.07E-12 ± 2.5E-13**	**Cin= 1.14E-12**	C_Total= 1.292E-11 ± 1.1E-13 C_Stray= use left **Cin= 1.67E-12 ± 2.4E-13**	**Cin= 1.26E-12**
0.9	C_Total= 1.238E-11 ± 1.2E-13 C_Stray= 1.128E-11 ± 1.4E-13 **Cin= 1.10E-12 ± 2.5E-13**	**Cin= 1.22E-12**	C_Total= 1.295E-11 ± 1.2E-13 C_Stray= use left **Cin= 1.67E-12 ± 2.6E-13**	**Cin= 1.37E-12**

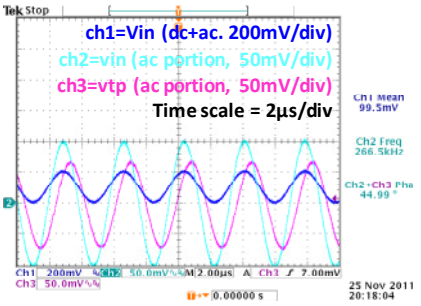
Measurements at NoQFG point with VBIAS=0.1V

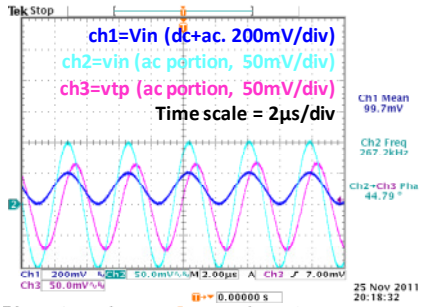
RIN= 4.697E+04

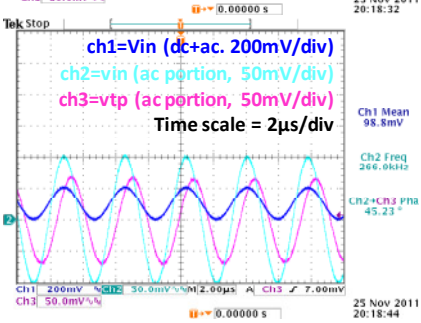
Sample No.	*phase*	*f*	*c*
1	44.51	2.598E+05	1.28E-11
2	44.78	2.619E+05	1.28E-11
3	44.99	2.665E+05	1.27E-11
4	45.05	2.662E+05	1.28E-11
5	44.79	2.672E+05	1.26E-11
6	44.64	2.678E+05	1.25E-11
7	45.23	2.669E+05	1.28E-11
8	44.97	2.683E+05	1.26E-11
9	44.75	2.671E+05	1.26E-11
10	45.15	2.688E+05	1.27E-11
11	44.75	2.689E+05	1.25E-11
12	45.43	2.689E+05	1.28E-11
13	44.88	2.721E+05	1.24E-11
14	45.39	2.714E+05	1.27E-11
15	44.76	2.726E+05	1.23E-11
16	44.68	2.720E+05	1.23E-11
17	44.92	2.713E+05	1.25E-11
18	44.91	2.714E+05	1.24E-11
19	44.98	2.716E+05	1.25E-11
20	44.86	2.725E+05	1.24E-11
Average	44.92	2.687E+05	**1.258E-11**
STD	0.24	3.460E+03	**1.698E-13**

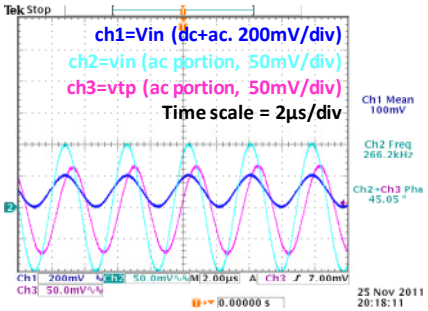


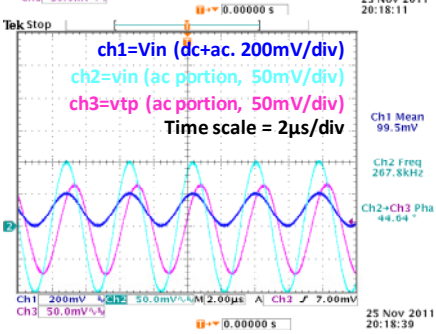


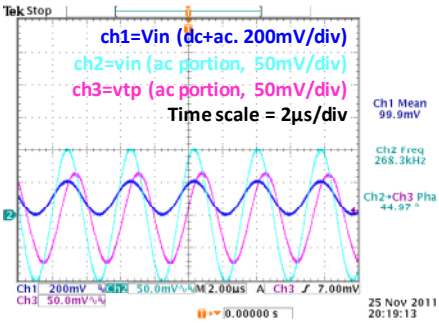


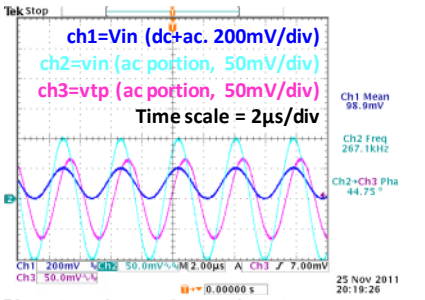


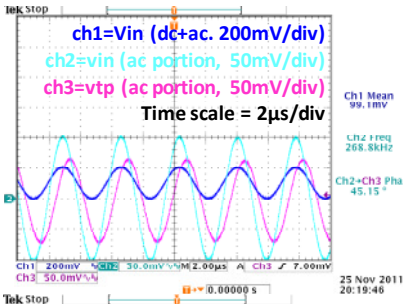


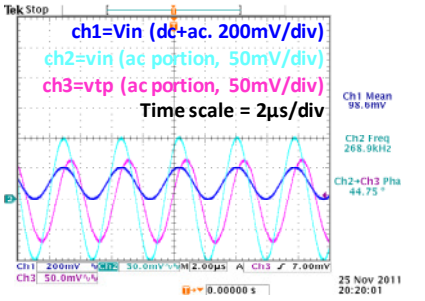


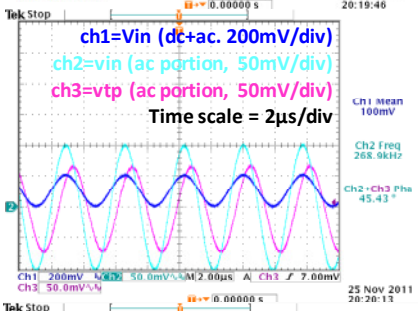


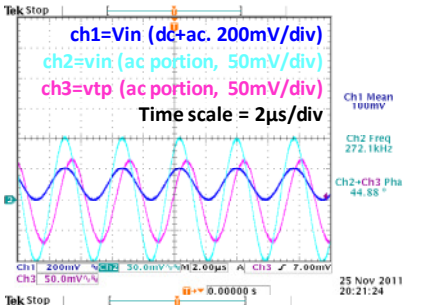


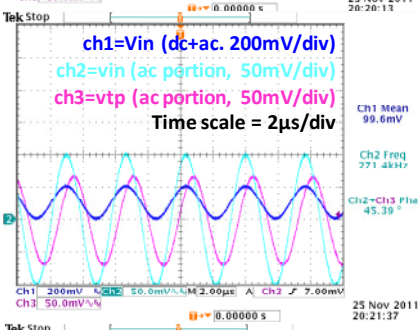

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
98.9mV
Ch2 Freq
267.1kHz
Ch2+Ch3 Pha
44.75 °
25 Nov 2011
20:19:26

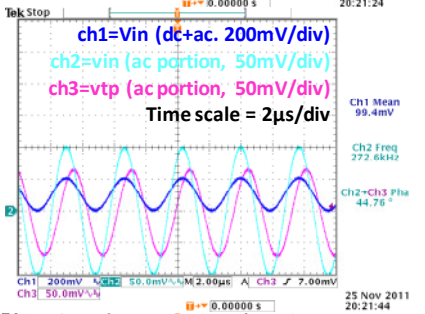

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
99.1mV
Ch2 Freq
268.8kHz
Ch2+Ch3 Pha
45.15 °
25 Nov 2011
20:19:46

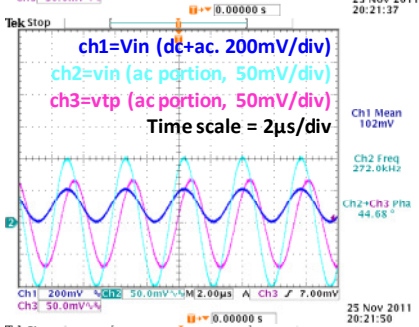

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
98.6mV
Ch2 Freq
268.9kHz
Ch2+Ch3 Pha
44.75 °
25 Nov 2011
20:20:01

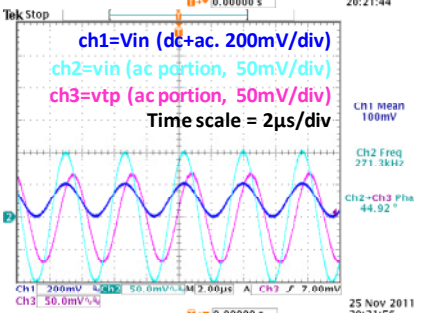

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
100mV
Ch2 Freq
268.9kHz
Ch2+Ch3 Pha
45.43 °
25 Nov 2011
20:20:13

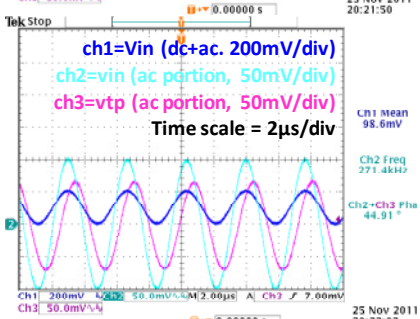

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
100mV
Ch2 Freq
272.1kHz
Ch2+Ch3 Pha
44.88 °
25 Nov 2011
20:21:24

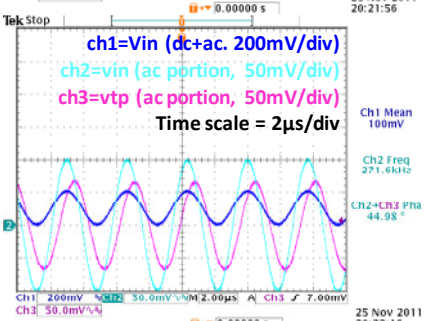

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
99.6mV
Ch2 Freq
271.4kHz
Ch2+Ch3 Pha
45.39 °
25 Nov 2011
20:21:37

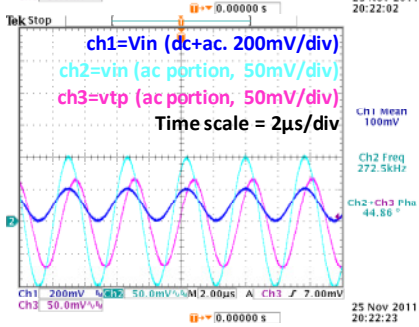

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
99.4mV
Ch2 Freq
272.6kHz
Ch2+Ch3 Pha
44.76 °
25 Nov 2011
20:21:44


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
102mV
Ch2 Freq
272.0kHz
Ch2+Ch3 Pha
44.68 °
25 Nov 2011
20:21:50


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
100mV
Ch2 Freq
271.3kHz
Ch2+Ch3 Pha
44.92 °
25 Nov 2011
20:21:56


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
98.6mV
Ch2 Freq
271.4kHz
Ch2+Ch3 Pha
44.91 °
25 Nov 2011
20:22:02

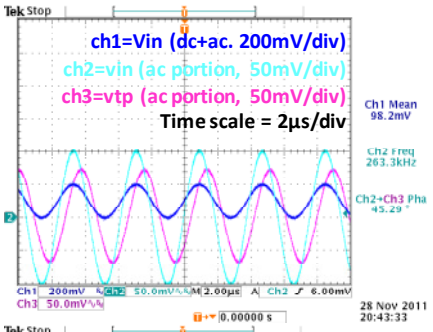

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
100mV
Ch2 Freq
271.6kHz
Ch2+Ch3 Pha
44.98 °
25 Nov 2011
20:22:16

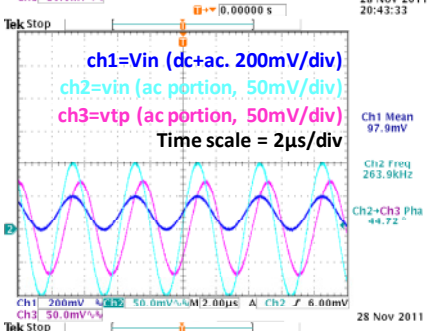

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
100mV
Ch2 Freq
272.5kHz
Ch2+Ch3 Pha
44.86 °
25 Nov 2011
20:22:23

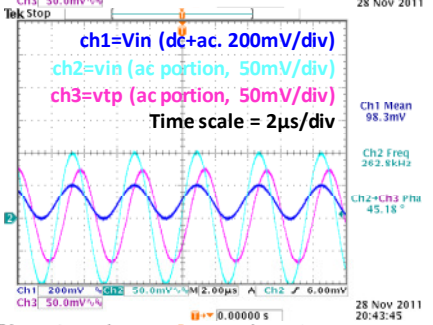
Measurements at QFG point with VBIAS=0.1V

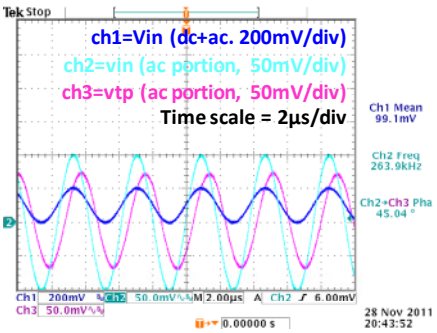
RIN= 4.697E+04

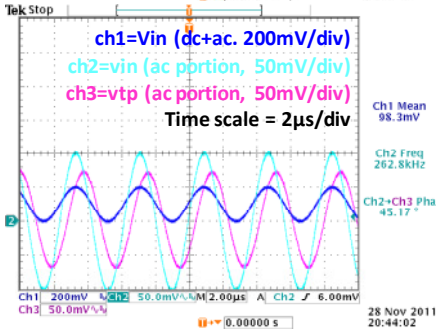
Sample No.	*phase*	*f*	*c*
1	45.29	2.633E+05	1.30E-11
2	44.72	2.639E+05	1.27E-11
3	45.18	2.628E+05	1.30E-11
4	45.04	2.639E+05	1.29E-11
5	45.17	2.628E+05	1.30E-11
6	45.33	2.629E+05	1.30E-11
7	45.11	2.628E+05	1.29E-11
8	45.00	2.626E+05	1.29E-11
9	45.50	2.625E+05	1.31E-11
10	45.45	2.631E+05	1.31E-11
11	45.21	2.639E+05	1.29E-11
12	45.34	2.629E+05	1.30E-11
13	45.03	2.626E+05	1.29E-11
14	44.90	2.629E+05	1.28E-11
15	45.53	2.626E+05	1.31E-11
16	45.29	2.632E+05	1.30E-11
17	45.06	2.635E+05	1.29E-11
18	45.75	2.625E+05	1.33E-11
19	44.58	2.627E+05	1.27E-11
20	45.31	2.627E+05	1.30E-11
Average	45.19	2.630E+05	**1.297E-11**
STD	0.28	4.662E+02	**1.344E-13**

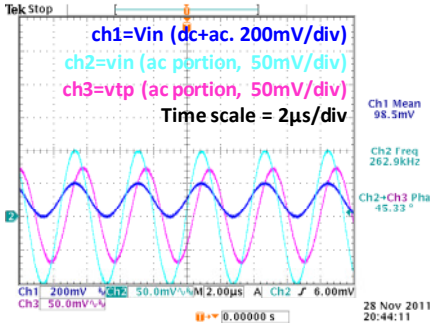


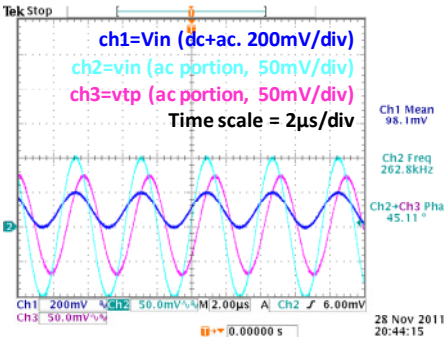


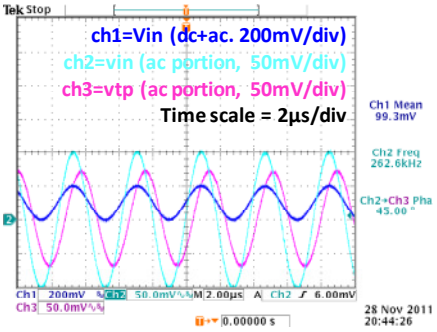


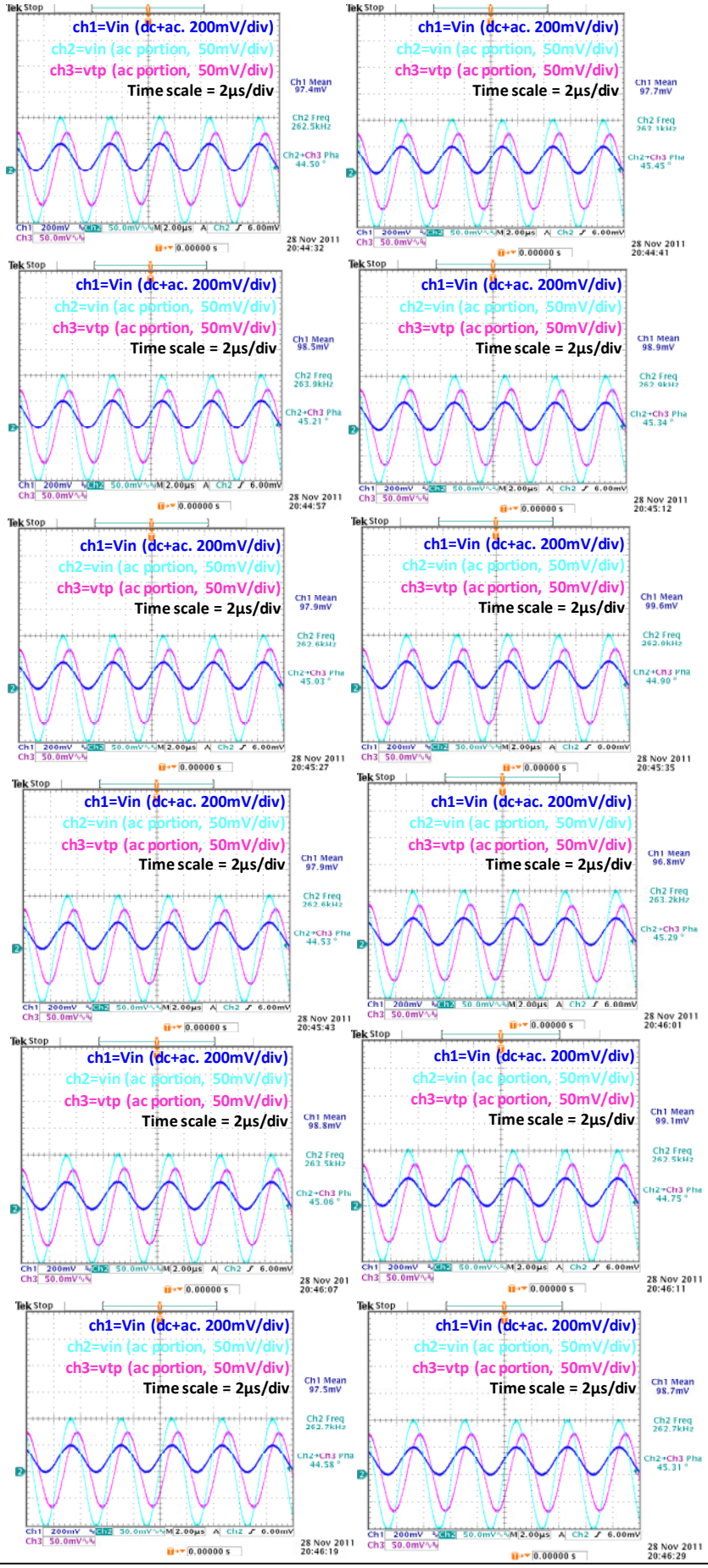








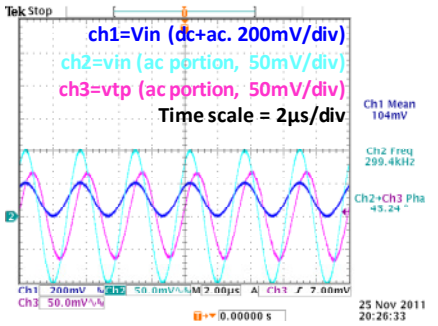


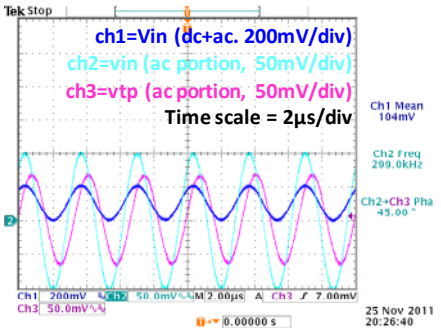

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 97.4mV
Ch2 Freq 262.5kHz
Ch2+Ch3 Pha 44.50°
28 Nov 2011 20:44:32
Ch1 Mean 97.7mV
Ch2 Freq 262.1kHz
Ch2+Ch3 Pha 45.45°
28 Nov 2011 20:44:41
Ch1 Mean 98.5mV
Ch2 Freq 263.9kHz
Ch2+Ch3 Pha 45.21°
28 Nov 2011 20:44:57
Ch1 Mean 98.9mV
Ch2 Freq 262.0kHz
Ch2+Ch3 Pha 45.34°
28 Nov 2011 20:45:12
Ch1 Mean 97.9mV
Ch2 Freq 262.6kHz
Ch2+Ch3 Pha 45.03°
28 Nov 2011 20:45:27
Ch1 Mean 99.6mV
Ch2 Freq 262.0kHz
Ch2+Ch3 Pha 44.90°
28 Nov 2011 20:45:35
Ch1 Mean 97.9mV
Ch2 Freq 262.6kHz
Ch2+Ch3 Pha 44.53°
28 Nov 2011 20:45:43
Ch1 Mean 96.8mV
Ch2 Freq 263.2kHz
Ch2+Ch3 Pha 45.29°
28 Nov 2011 20:46:01
Ch1 Mean 98.8mV
Ch2 Freq 263.5kHz
Ch2+Ch3 Pha 45.06°
28 Nov 2011 20:46:07
Ch1 Mean 99.1mV
Ch2 Freq 262.5kHz
Ch2+Ch3 Pha 44.75°
28 Nov 2011 20:46:11
Ch1 Mean 97.5mV
Ch2 Freq 262.7kHz
Ch2+Ch3 Pha 44.58°
28 Nov 2011 20:46:19
Ch1 Mean 98.7mV
Ch2 Freq 262.7kHz
Ch2+Ch3 Pha 45.31°
28 Nov 2011 20:46:29

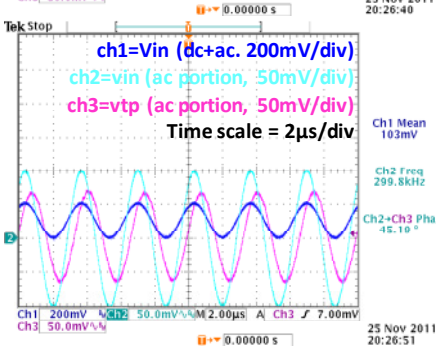
Measurements at PADONLY point with VBIAS=0.1V

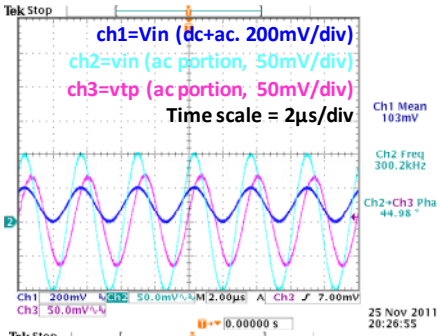
RIN= 4.697E+04

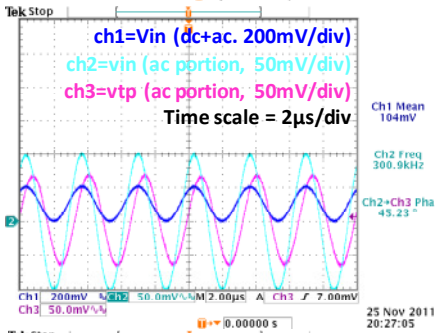
Sample No.	*phase*	*f*	*c*
1	45.24	2.994E+05	1.14E-11
2	45.00	2.990E+05	1.13E-11
3	45.19	2.988E+05	1.14E-11
4	44.98	3.002E+05	1.13E-11
5	45.23	3.009E+05	1.14E-11
6	44.66	3.006E+05	1.11E-11
7	45.23	3.009E+05	1.14E-11
8	44.65	2.996E+05	1.12E-11
9	44.52	3.004E+05	1.11E-11
10	44.87	3.008E+05	1.12E-11
11	44.84	3.020E+05	1.12E-11
12	44.99	3.003E+05	1.13E-11
13	44.50	3.011E+05	1.11E-11
14	44.63	3.014E+05	1.11E-11
15	45.17	3.013E+05	1.13E-11
16	45.12	3.008E+05	1.13E-11
17	45.08	3.014E+05	1.13E-11
18	45.48	3.001E+05	1.15E-11
19	45.61	2.996E+05	1.16E-11
20	45.24	3.001E+05	1.14E-11
Average	45.01	3.004E+05	**1.128E-11**
STD	0.31	8.499E+02	**1.349E-13**

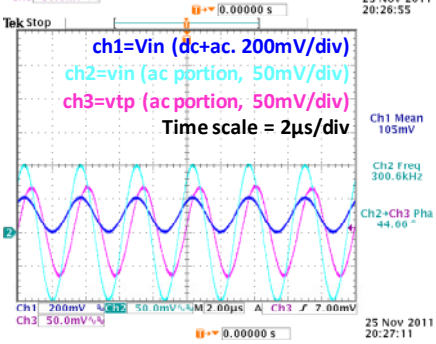


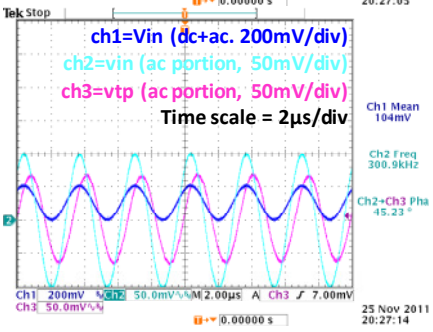


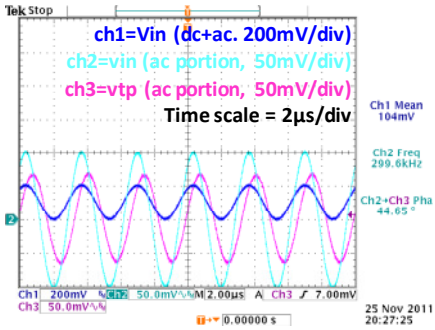


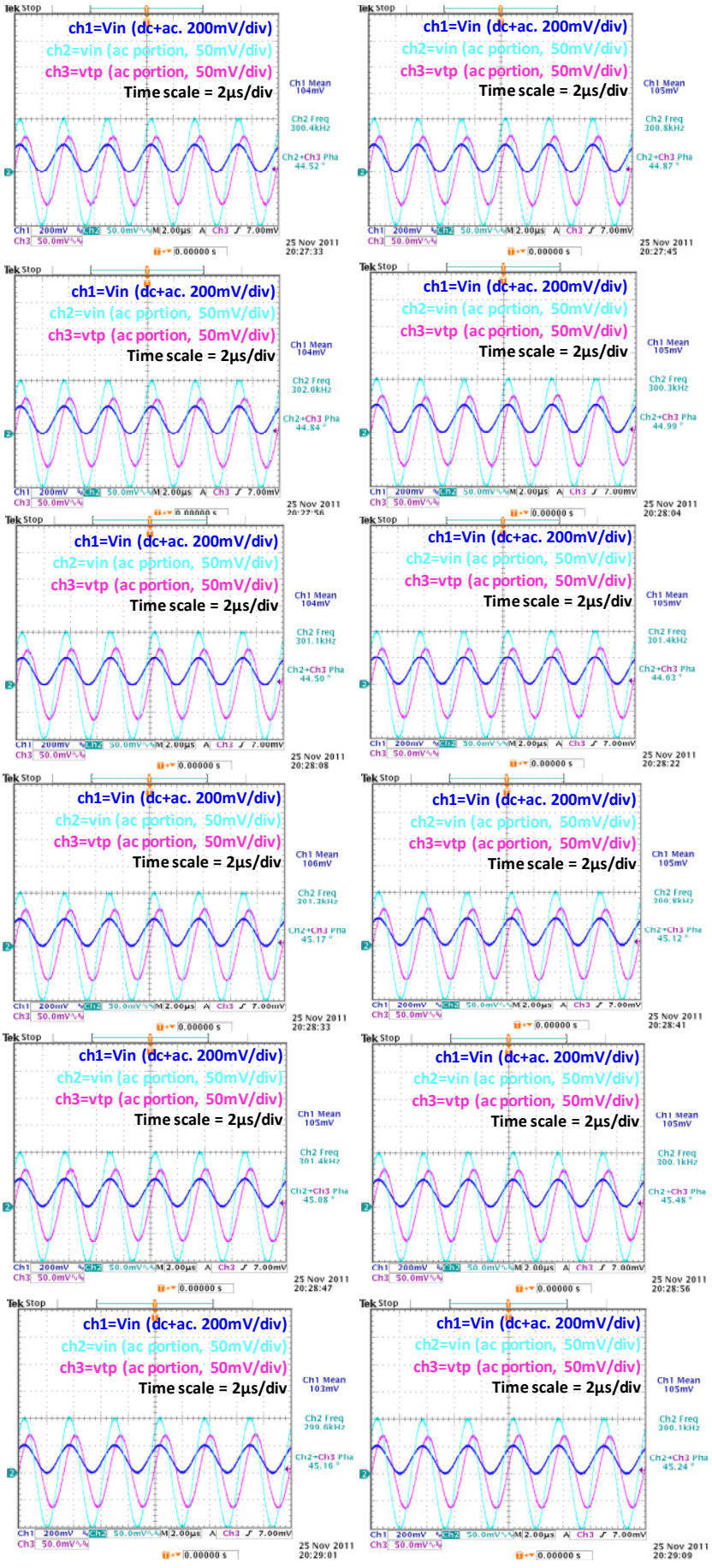








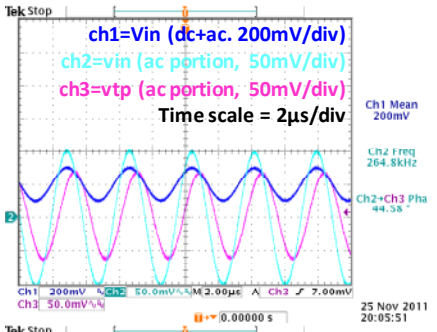


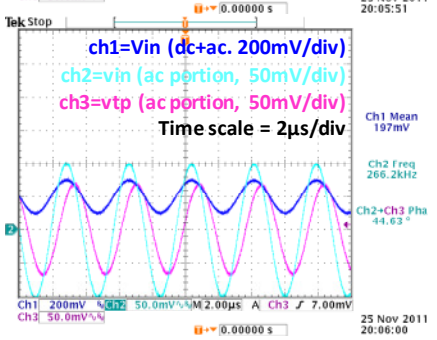

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 104mV
Ch2 Freq 300.4kHz
Ch2+Ch3 Pha 44.52 °
25 Nov 2011 20:27:33
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 300.8kHz
Ch2+Ch3 Pha 44.87 °
25 Nov 2011 20:27:45
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 104mV
Ch2 Freq 302.0kHz
Ch2+Ch3 Pha 44.84 °
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 300.3kHz
Ch2+Ch3 Pha 44.99 °
25 Nov 2011 20:28:04
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 104mV
Ch2 Freq 301.1kHz
Ch2+Ch3 Pha 44.50 °
25 Nov 2011 20:28:08
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 301.4kHz
Ch2+Ch3 Pha 44.63 °
25 Nov 2011 20:28:22
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 106mV
Ch2 Freq 301.3kHz
Ch2+Ch3 Pha 45.17 °
25 Nov 2011 20:28:33
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 300.9kHz
Ch2+Ch3 Pha 45.12 °
25 Nov 2011 20:28:41
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 301.4kHz
Ch2+Ch3 Pha 45.08 °
25 Nov 2011 20:28:47
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 300.1kHz
Ch2+Ch3 Pha 45.48 °
25 Nov 2011 20:28:56
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 103mV
Ch2 Freq 299.6kHz
Ch2+Ch3 Pha 45.16 °
25 Nov 2011 20:29:01
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 105mV
Ch2 Freq 300.1kHz
Ch2+Ch3 Pha 45.24 °
25 Nov 2011 20:29:09

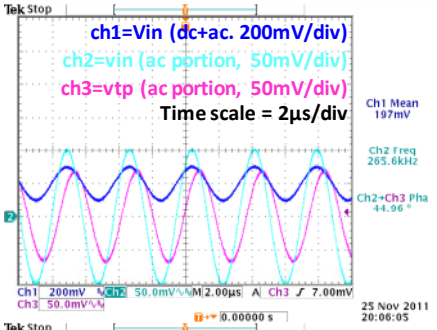
Measurements at NoQFG point with VBIAS=0.2V

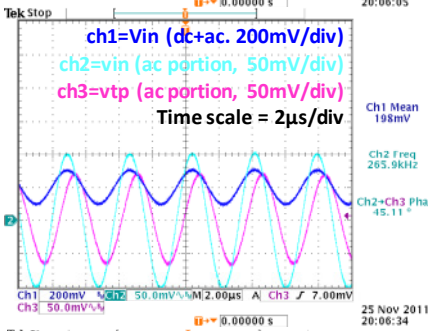
RIN= 4.697E+04

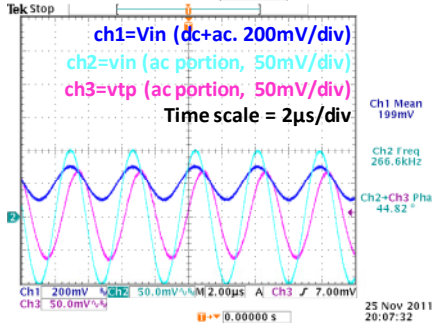
Sample No.	*phase*	*f*	*c*
1	44.58	2.648E+05	1.26E-11
2	44.63	2.662E+05	1.26E-11
3	44.96	2.656E+05	1.27E-11
4	45.21	2.651E+05	1.29E-11
5	45.11	2.659E+05	1.28E-11
6	44.51	2.652E+05	1.26E-11
7	44.82	2.666E+05	1.26E-11
8	45.26	2.658E+05	1.29E-11
9	44.85	2.669E+05	1.26E-11
10	44.56	2.668E+05	1.25E-11
11	45.16	2.674E+05	1.27E-11
12	44.55	2.671E+05	1.25E-11
13	45.32	2.654E+05	1.29E-11
14	44.69	2.660E+05	1.26E-11
15	44.90	2.674E+05	1.26E-11
16	45.13	2.667E+05	1.28E-11
17	44.68	2.672E+05	1.25E-11
18	44.58	2.677E+05	1.25E-11
19	45.01	2.667E+05	1.27E-11
20	45.18	2.671E+05	1.28E-11
Average	44.88	2.664E+05	**1.267E-11**
STD	0.27	8.606E+02	**1.326E-13**

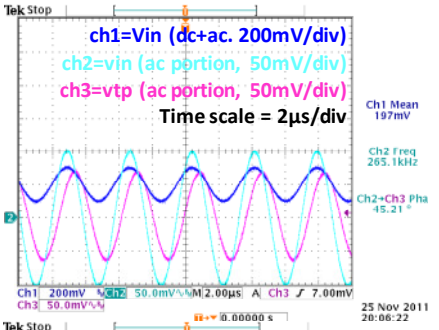


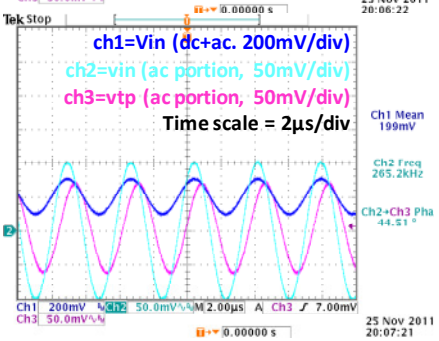


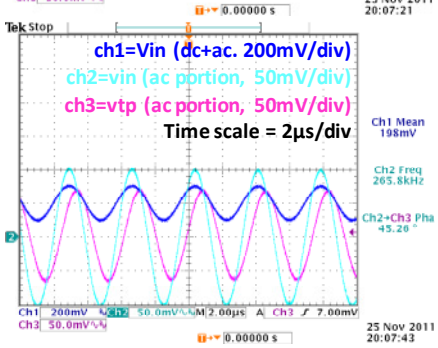


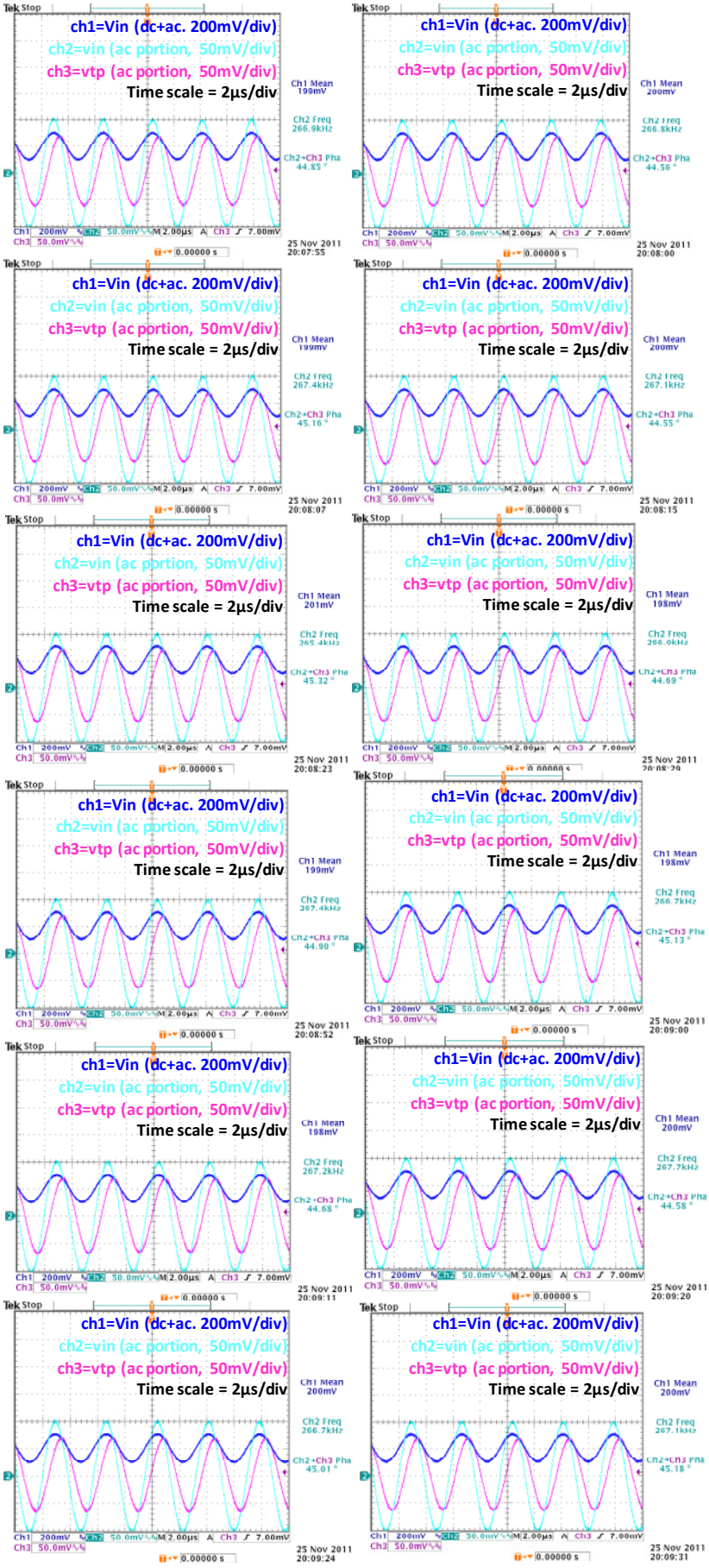








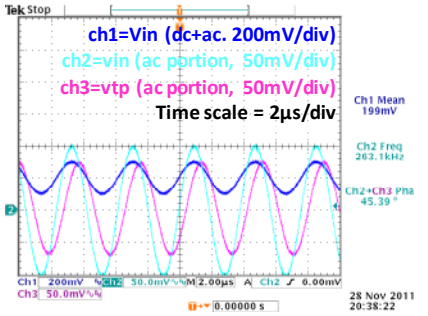


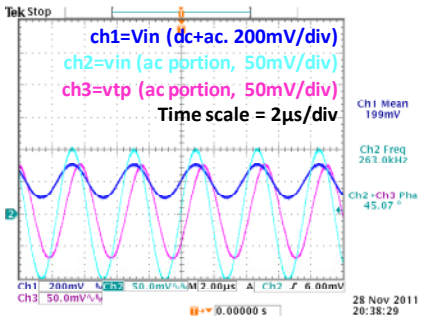

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 199mV
Ch2 Freq 266.9kHz
Ch2+Ch3 Pha 44.85 °
25 Nov 2011 20:07:55
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 266.8kHz
Ch2+Ch3 Pha 44.56 °
25 Nov 2011 20:08:00
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 199mV
Ch2 Freq 267.4kHz
Ch2+Ch3 Pha 45.16 °
25 Nov 2011 20:08:07
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 267.1kHz
Ch2+Ch3 Pha 44.55 °
25 Nov 2011 20:08:15
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 201mV
Ch2 Freq 265.4kHz
Ch2+Ch3 Pha 45.32 °
25 Nov 2011 20:08:23
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 198mV
Ch2 Freq 266.0kHz
Ch2+Ch3 Pha 44.69 °
25 Nov 2011 20:08:29
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 199mV
Ch2 Freq 267.4kHz
Ch2+Ch3 Pha 44.90 °
25 Nov 2011 20:08:52
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 198mV
Ch2 Freq 266.7kHz
Ch2+Ch3 Pha 45.13 °
25 Nov 2011 20:09:00
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 198mV
Ch2 Freq 267.2kHz
Ch2+Ch3 Pha 44.68 °
25 Nov 2011 20:09:11
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 267.7kHz
Ch2+Ch3 Pha 44.58 °
25 Nov 2011 20:09:20
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 266.7kHz
Ch2+Ch3 Pha 45.01 °
25 Nov 2011 20:09:24
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 267.1kHz
Ch2+Ch3 Pha 45.18 °
25 Nov 2011 20:09:31

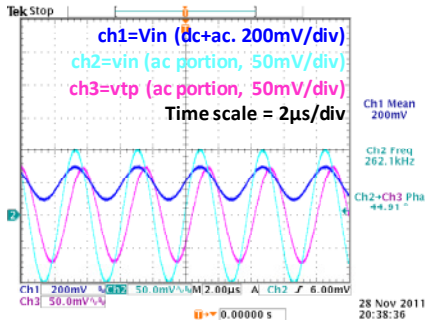
Measurements at QFG point with VBIAS=0.2V

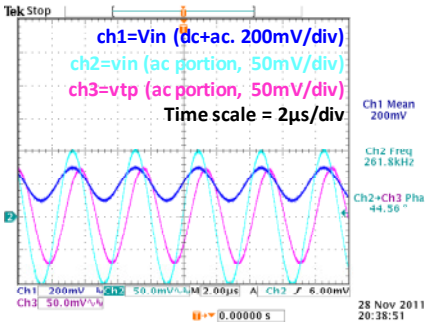
RIN= 4.697E+04

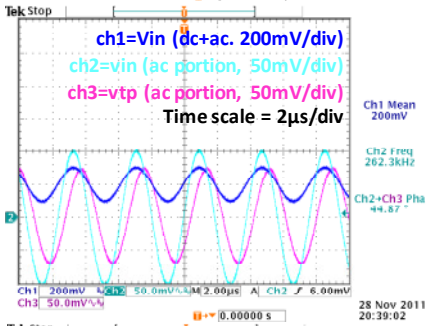
Sample No.	*phase*	*f*	*c*
1	45.39	2.631E+05	1.31E-11
2	45.07	2.630E+05	1.29E-11
3	45.91	2.621E+05	1.33E-11
4	45.56	2.618E+05	1.32E-11
5	44.87	2.623E+05	1.29E-11
6	45.09	2.625E+05	1.29E-11
7	45.03	2.611E+05	1.30E-11
8	44.82	2.613E+05	1.29E-11
9	44.84	2.605E+05	1.29E-11
10	45.13	2.619E+05	1.30E-11
11	44.85	2.608E+05	1.29E-11
12	44.85	2.612E+05	1.29E-11
13	44.83	2.627E+05	1.28E-11
14	45.28	2.623E+05	1.30E-11
15	44.56	2.619E+05	1.27E-11
16	44.82	2.628E+05	1.28E-11
17	44.52	2.620E+05	1.27E-11
18	45.00	2.626E+05	1.29E-11
19	45.30	2.619E+05	1.31E-11
20	44.62	2.618E+05	1.28E-11
Average	45.02	2.620E+05	**1.294E-11**
STD	0.34	7.208E+02	**1.520E-13**

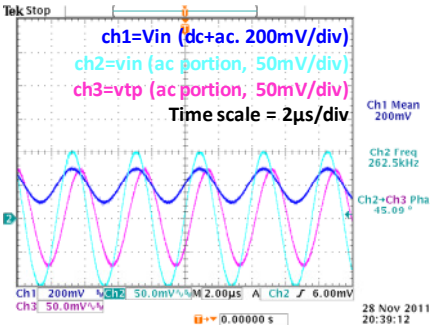


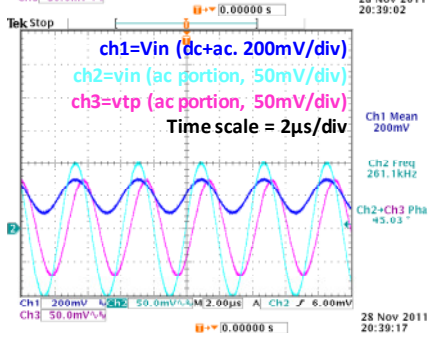


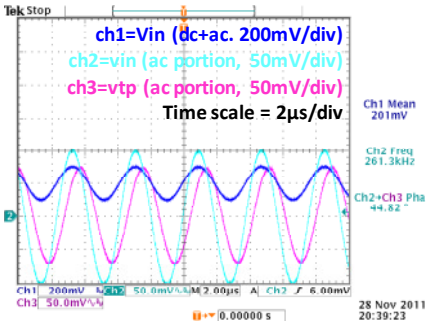


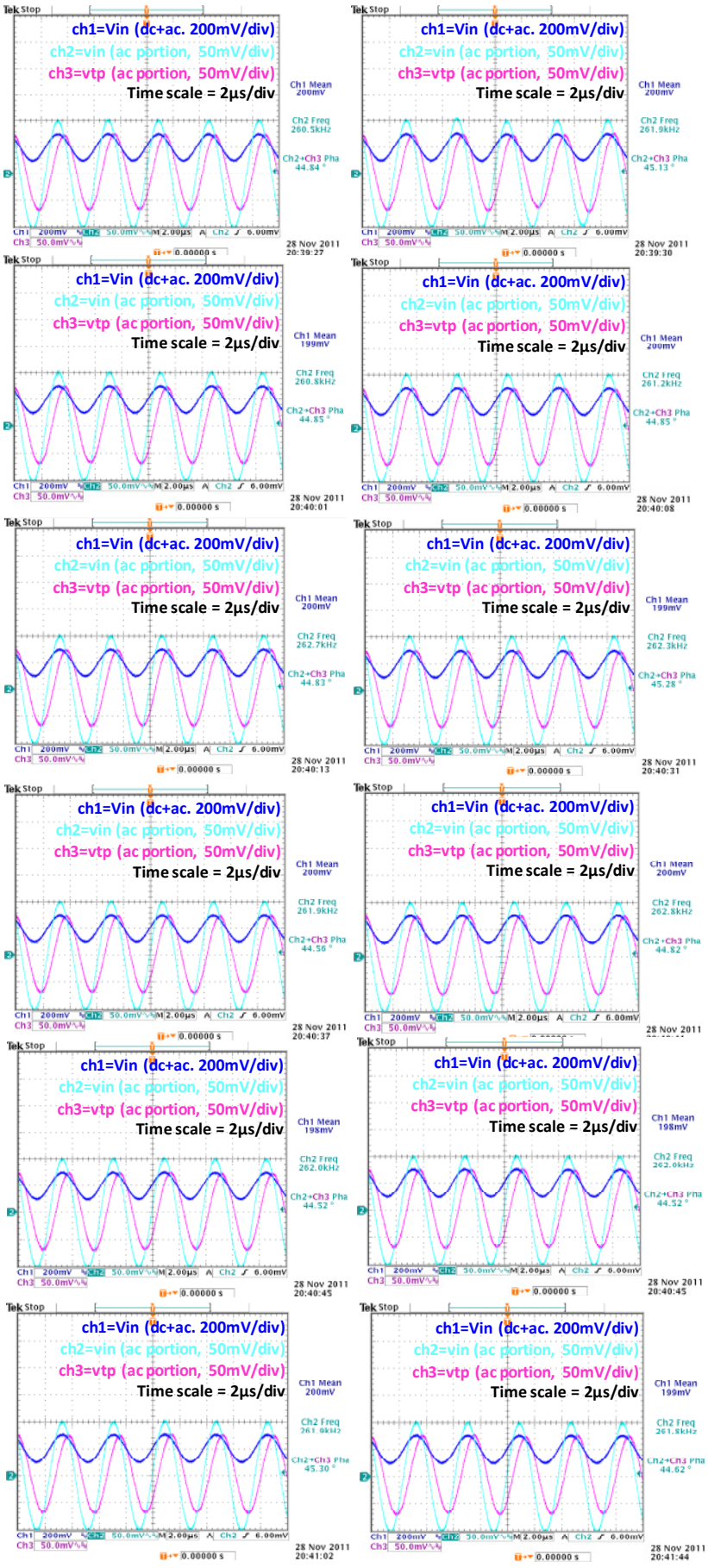








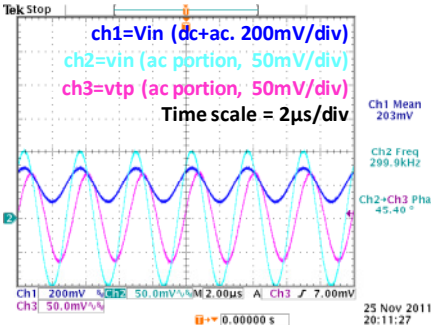


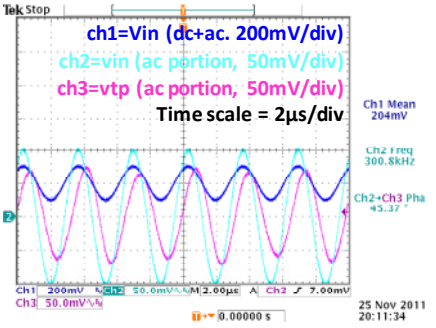

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 200mV
Ch2 Freq 260.5kHz
Ch2+Ch3 Pha 44.84 °
28 Nov 2011 20:39:27
Ch1 Mean 200mV
Ch2 Freq 261.9kHz
Ch2+Ch3 Pha 45.13 °
28 Nov 2011 20:39:30
Ch1 Mean 199mV
Ch2 Freq 260.8kHz
Ch2+Ch3 Pha 44.85 °
28 Nov 2011 20:40:01
Ch1 Mean 200mV
Ch2 Freq 261.2kHz
Ch2+Ch3 Pha 44.85 °
28 Nov 2011 20:40:08
Ch1 Mean 200mV
Ch2 Freq 262.7kHz
Ch2+Ch3 Pha 44.83 °
28 Nov 2011 20:40:13
Ch1 Mean 199mV
Ch2 Freq 262.3kHz
Ch2+Ch3 Pha 45.28 °
28 Nov 2011 20:40:31
Ch1 Mean 200mV
Ch2 Freq 261.9kHz
Ch2+Ch3 Pha 44.56 °
28 Nov 2011 20:40:37
Ch1 Mean 200mV
Ch2 Freq 262.8kHz
Ch2+Ch3 Pha 44.82 °
Ch1 Mean 198mV
Ch2 Freq 262.0kHz
Ch2+Ch3 Pha 44.52 °
28 Nov 2011 20:40:45
Ch1 Mean 198mV
Ch2 Freq 262.0kHz
Ch2+Ch3 Pha 44.52 °
28 Nov 2011 20:40:45
Ch1 Mean 200mV
Ch2 Freq 261.9kHz
Ch2+Ch3 Pha 45.30 °
28 Nov 2011 20:41:02
Ch1 Mean 199mV
Ch2 Freq 261.8kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 20:41:44

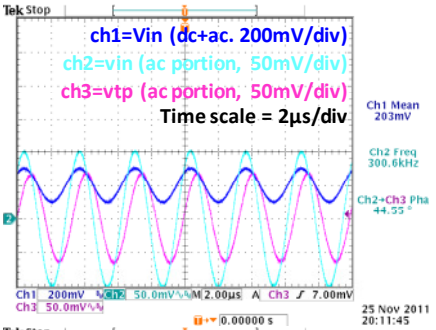
Measurements at PADONLY point with VBIAS=0.2V

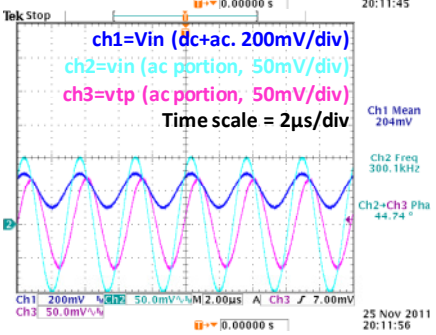
RIN= 4.697E+04

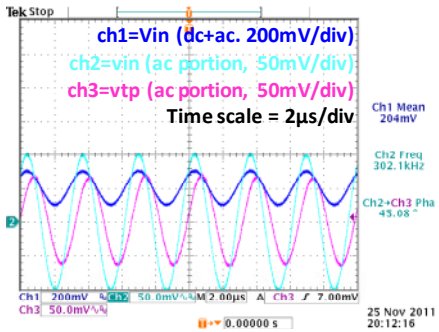
Sample No.	*phase*	*f*	*c*
1	45.40	2.999E+05	1.15E-11
2	45.37	3.008E+05	1.14E-11
3	44.55	3.006E+05	1.11E-11
4	45.32	2.994E+05	1.14E-11
5	44.74	3.001E+05	1.12E-11
6	44.73	3.000E+05	1.12E-11
7	45.08	3.021E+05	1.12E-11
8	44.68	3.018E+05	1.11E-11
9	45.17	2.998E+05	1.14E-11
10	44.65	2.996E+05	1.12E-11
11	45.03	3.014E+05	1.13E-11
12	45.44	2.992E+05	1.15E-11
13	44.60	3.014E+05	1.11E-11
14	45.46	3.017E+05	1.14E-11
15	45.50	3.010E+05	1.15E-11
16	44.16	2.998E+05	1.10E-11
17	44.81	3.017E+05	1.12E-11
18	44.57	3.020E+05	1.11E-11
19	44.67	3.006E+05	1.11E-11
20	44.73	3.018E+05	1.11E-11
Average	44.93	3.007E+05	**1.124E-11**
STD	0.39	9.571E+02	**1.602E-13**

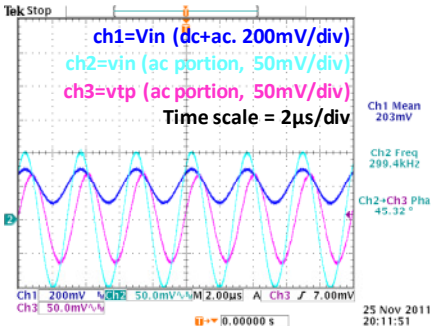


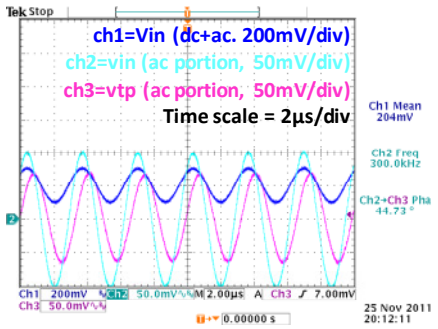


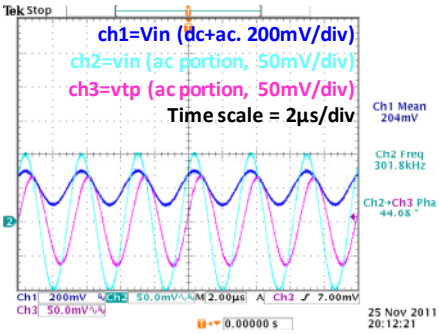


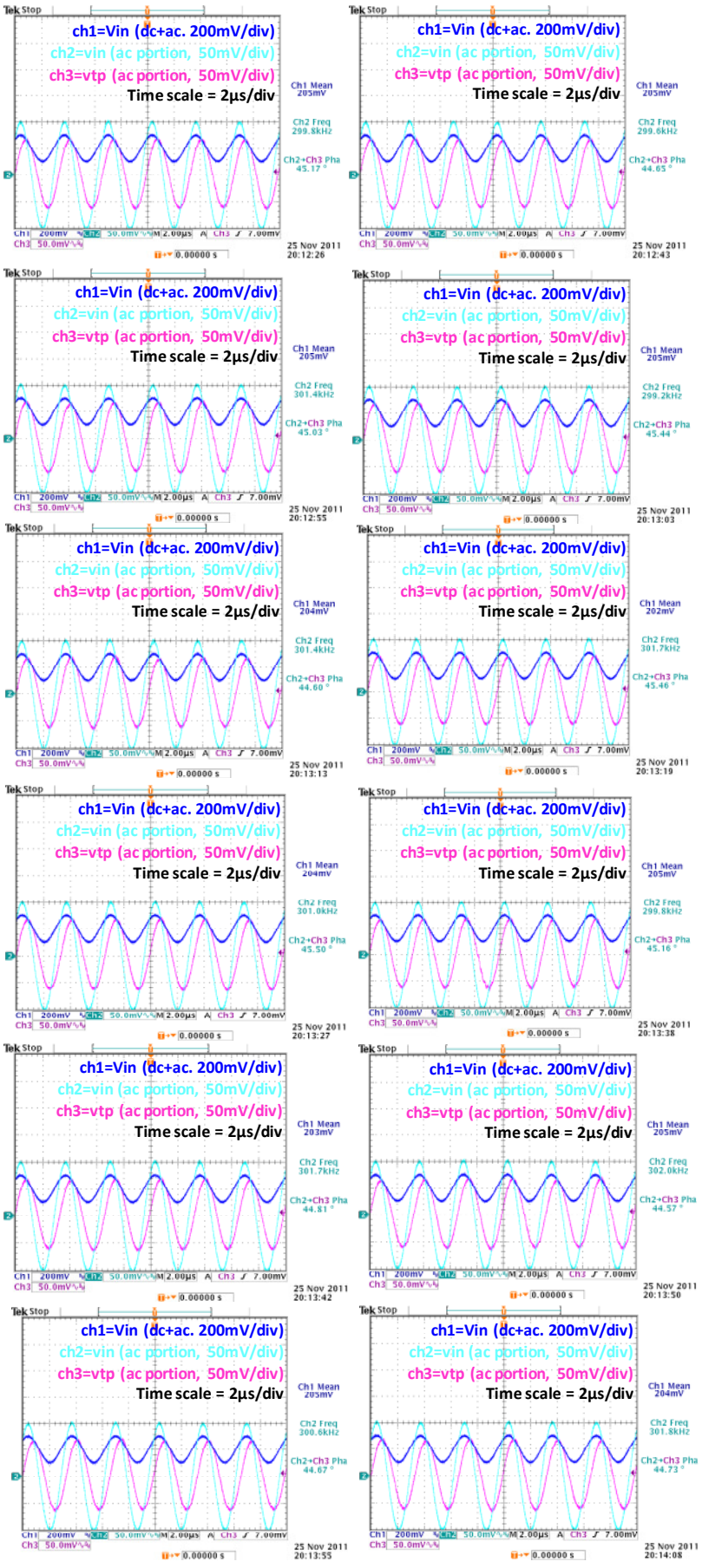








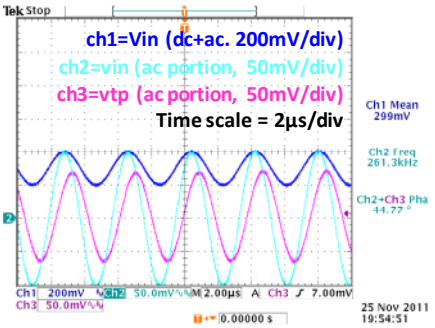


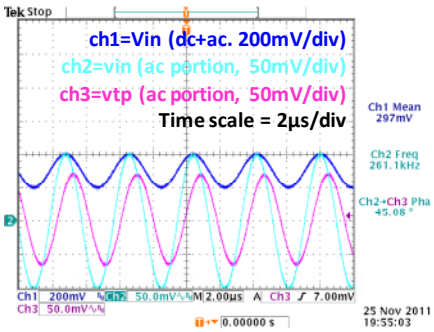

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 299.8kHz
Ch2+Ch3 Pha 45.17 °
25 Nov 2011 20:12:26
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 299.6kHz
Ch2+Ch3 Pha 44.65 °
25 Nov 2011 20:12:43
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 301.4kHz
Ch2+Ch3 Pha 45.03 °
25 Nov 2011 20:12:55
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 299.2kHz
Ch2+Ch3 Pha 45.44 °
25 Nov 2011 20:13:03
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 204mV
Ch2 Freq 301.4kHz
Ch2+Ch3 Pha 44.60 °
25 Nov 2011 20:13:13
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 202mV
Ch2 Freq 301.7kHz
Ch2+Ch3 Pha 45.46 °
25 Nov 2011 20:13:19
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 204mV
Ch2 Freq 301.0kHz
Ch2+Ch3 Pha 45.50 °
25 Nov 2011 20:13:27
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 299.8kHz
Ch2+Ch3 Pha 45.16 °
25 Nov 2011 20:13:38
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 203mV
Ch2 Freq 301.7kHz
Ch2+Ch3 Pha 44.81 °
25 Nov 2011 20:13:42
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 302.0kHz
Ch2+Ch3 Pha 44.57 °
25 Nov 2011 20:13:50
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 205mV
Ch2 Freq 300.6kHz
Ch2+Ch3 Pha 44.67 °
25 Nov 2011 20:13:55
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 204mV
Ch2 Freq 301.8kHz
Ch2+Ch3 Pha 44.73 °
25 Nov 2011 20:14:08

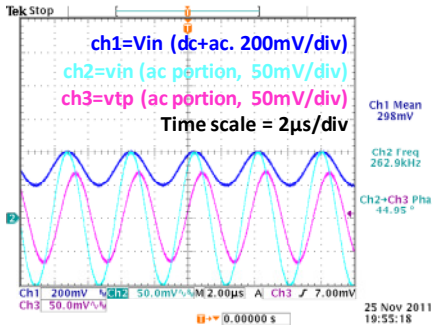
Measurements at NoQFG point with VBIAS=0.3V

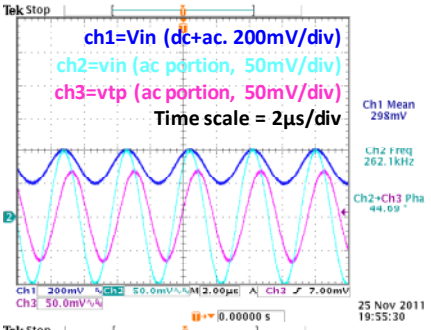
RIN= 4.697E+04

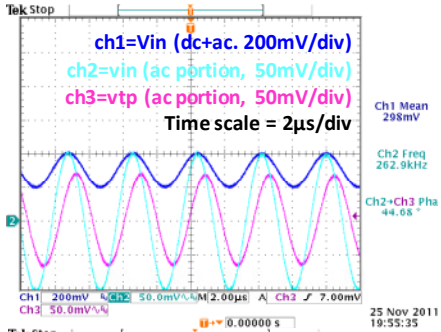
Sample No.	*phase*	*f*	*c*
1	44.77	2.613E+05	1.29E-11
2	45.08	2.611E+05	1.30E-11
3	44.95	2.629E+05	1.29E-11
4	44.69	2.621E+05	1.28E-11
5	44.68	2.629E+05	1.27E-11
6	45.25	2.622E+05	1.30E-11
7	44.62	2.620E+05	1.28E-11
8	44.63	2.624E+05	1.27E-11
9	44.98	2.616E+05	1.29E-11
10	44.63	2.623E+05	1.28E-11
11	44.88	2.628E+05	1.28E-11
12	44.81	2.624E+05	1.28E-11
13	44.61	2.606E+05	1.28E-11
14	44.46	2.627E+05	1.27E-11
15	45.13	2.642E+05	1.29E-11
16	45.04	2.641E+05	1.28E-11
17	45.37	2.652E+05	1.29E-11
18	44.78	2.647E+05	1.27E-11
19	44.67	2.654E+05	1.26E-11
20	45.02	2.655E+05	1.28E-11
Average	44.85	2.629E+05	**1.282E-11**
STD	0.24	1.456E+03	**1.090E-13**

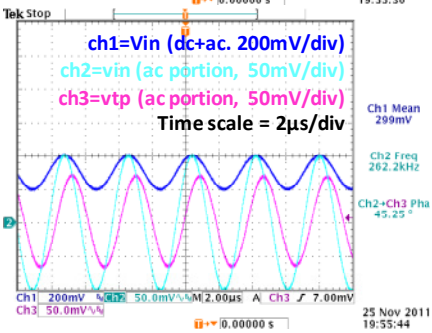


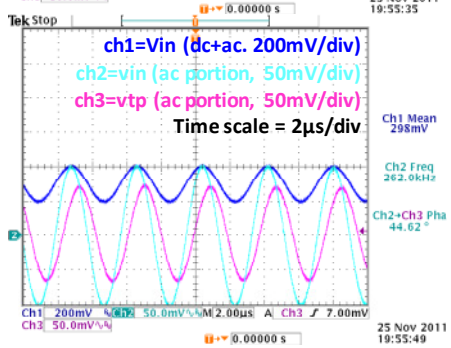


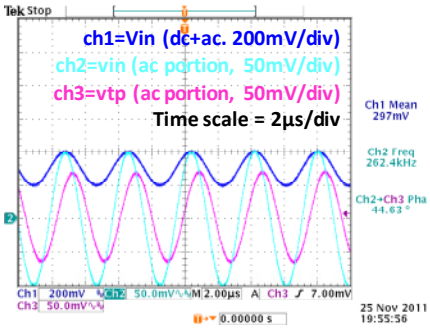


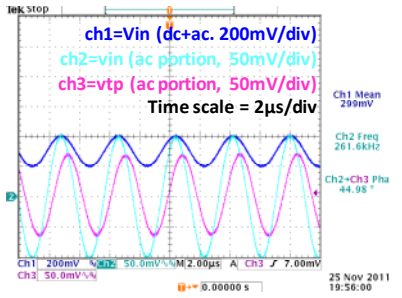


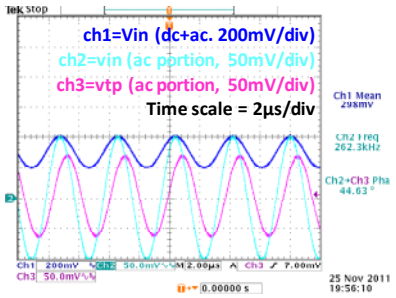


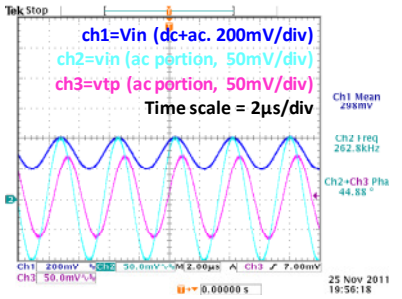


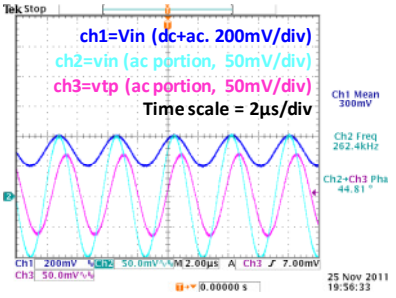


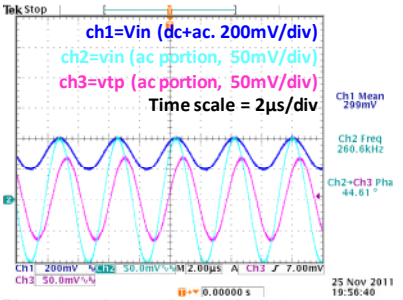


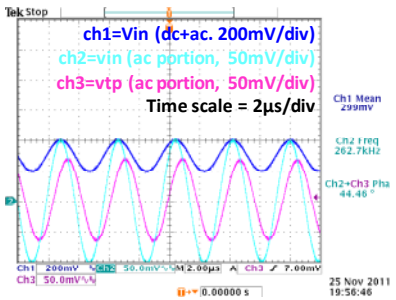

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 261.6kHz
Ch2+Ch3 Pha 44.98 °
25 Nov 2011 19:56:00

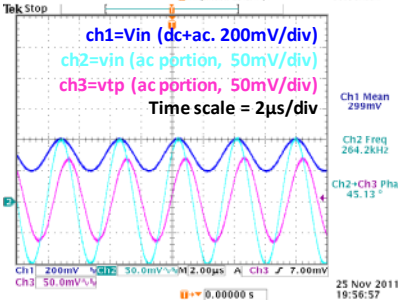

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 262.3kHz
Ch2+Ch3 Pha 44.63 °
25 Nov 2011 19:56:10

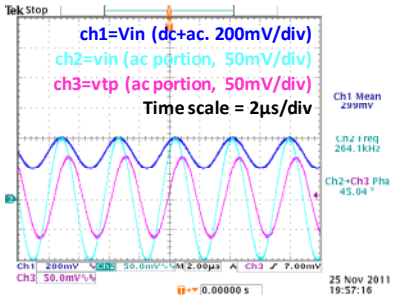

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 262.8kHz
Ch2+Ch3 Pha 44.88 °
25 Nov 2011 19:56:18

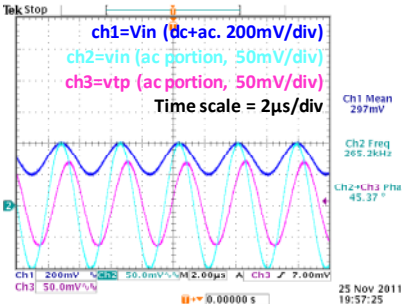

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 262.4kHz
Ch2+Ch3 Pha 44.81 °
25 Nov 2011 19:56:33

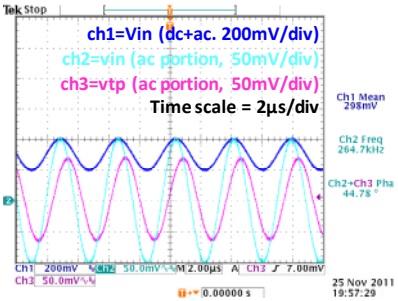

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 260.6kHz
Ch2+Ch3 Pha 44.61 °
25 Nov 2011 19:56:40

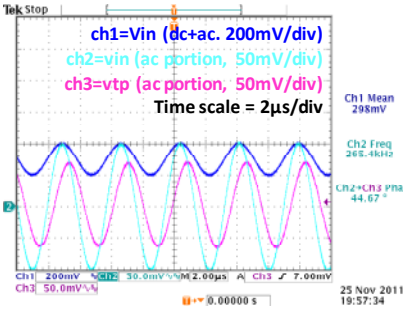

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 262.7kHz
Ch2+Ch3 Pha 44.46 °
25 Nov 2011 19:56:46

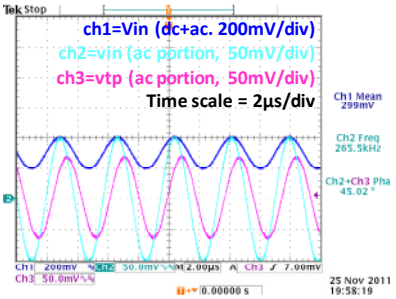

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 264.2kHz
Ch2+Ch3 Pha 45.13 °
25 Nov 2011 19:56:57


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 264.1kHz
Ch2+Ch3 Pha 45.04 °
25 Nov 2011 19:57:16


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 297mV
Ch2 Freq 265.2kHz
Ch2+Ch3 Pha 45.37 °
25 Nov 2011 19:57:25


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 264.7kHz
Ch2+Ch3 Pha 44.78 °
25 Nov 2011 19:57:29

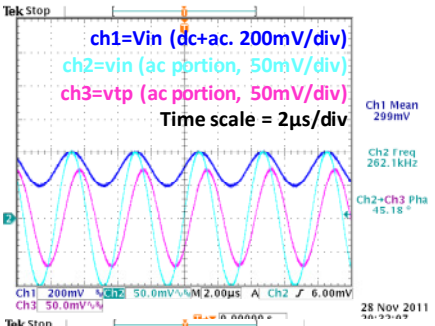

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 265.4kHz
Ch2+Ch3 Pha 44.67 °
25 Nov 2011 19:57:34

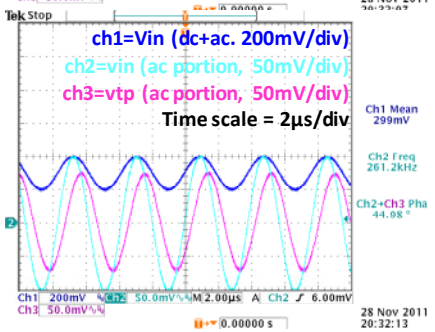

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 265.5kHz
Ch2+Ch3 Pha 45.02 °
25 Nov 2011 19:58:19

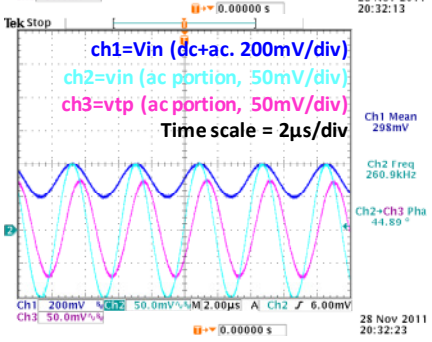
Measurements at QFG point with VBIAS=0.3V

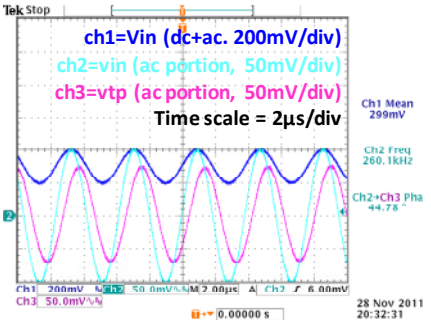
RIN= 4.697E+04

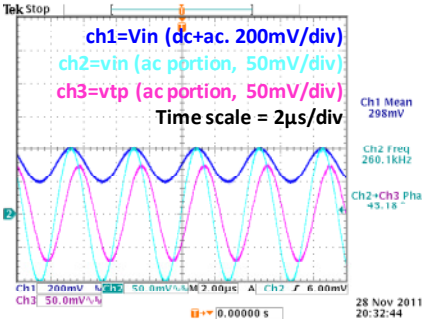
Sample No.	*phase*	*f*	*c*
1	45.18	2.621E+05	1.30E-11
2	44.98	2.612E+05	1.30E-11
3	44.89	2.609E+05	1.29E-11
4	44.78	2.601E+05	1.29E-11
5	45.18	2.601E+05	1.31E-11
6	44.68	2.607E+05	1.29E-11
7	44.81	2.616E+05	1.29E-11
8	45.03	2.611E+05	1.30E-11
9	45.11	2.611E+05	1.30E-11
10	45.34	2.620E+05	1.31E-11
11	45.06	2.616E+05	1.30E-11
12	44.55	2.603E+05	1.28E-11
13	44.55	2.603E+05	1.28E-11
14	44.54	2.627E+05	1.27E-11
15	44.59	2.590E+05	1.29E-11
16	45.22	2.602E+05	1.31E-11
17	44.89	2.608E+05	1.29E-11
18	44.75	2.615E+05	1.28E-11
19	44.78	2.609E+05	1.29E-11
20	44.73	2.608E+05	1.29E-11
Average	44.88	2.610E+05	**1.293E-11**
STD	0.25	8.432E+02	**1.085E-13**

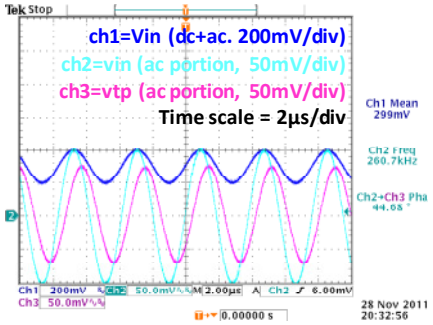


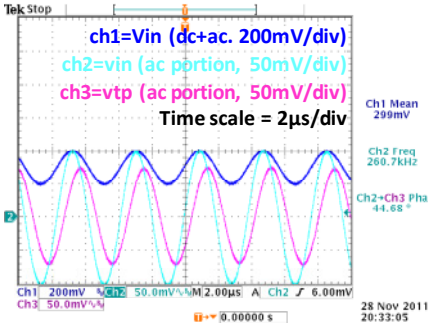


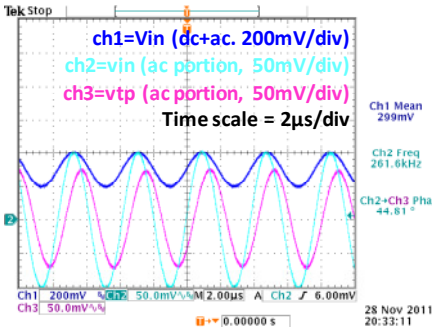


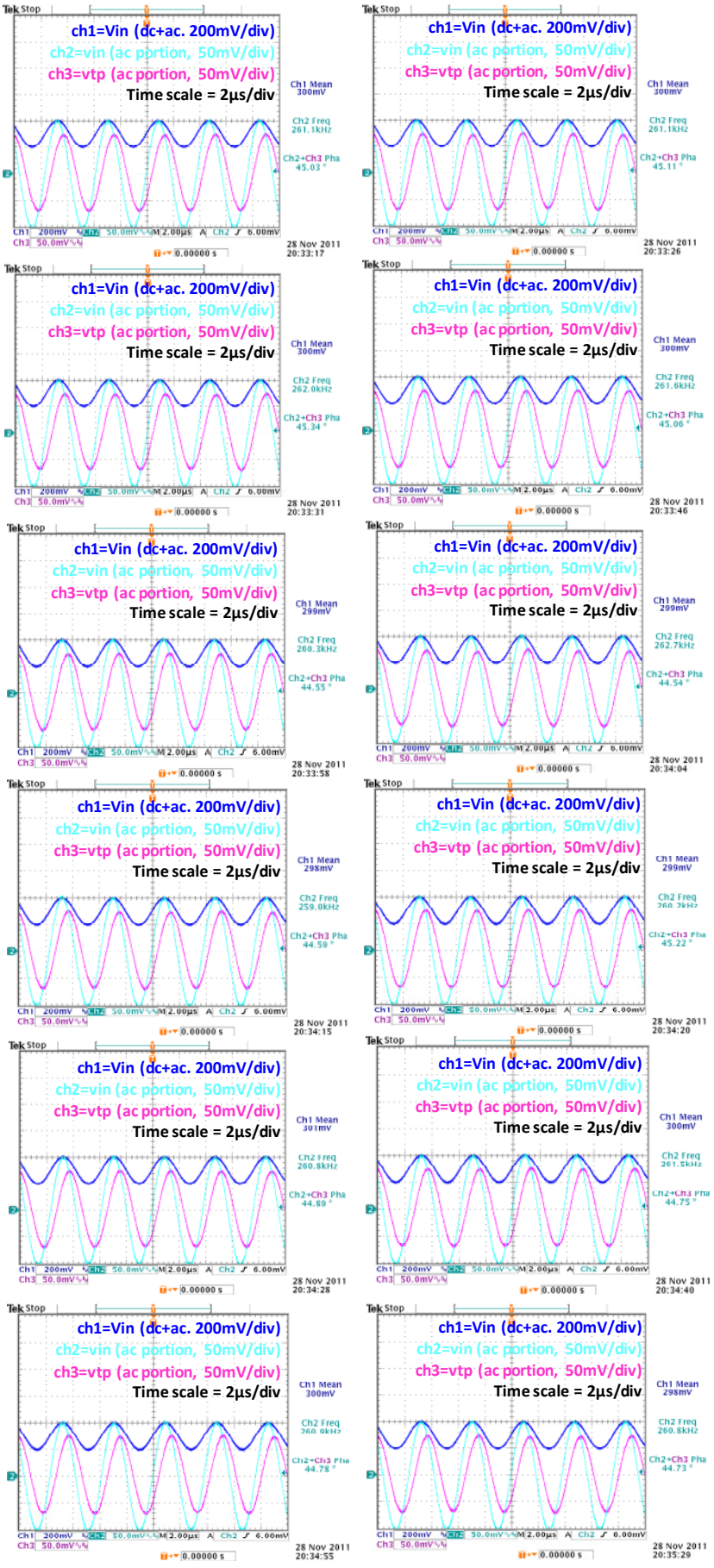








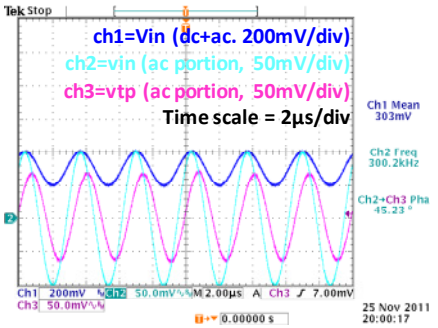


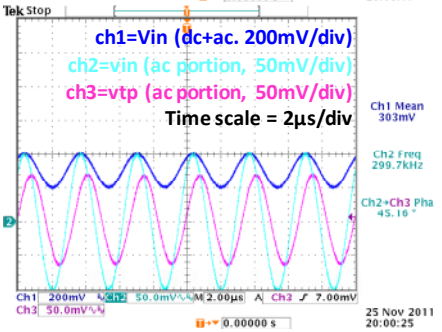

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 261.1kHz
Ch2+Ch3 Pha 45.03 °
28 Nov 2011 20:33:17
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 261.1kHz
Ch2+Ch3 Pha 45.11 °
28 Nov 2011 20:33:26
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 262.0kHz
Ch2+Ch3 Pha 45.34 °
28 Nov 2011 20:33:31
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 261.6kHz
Ch2+Ch3 Pha 45.06 °
28 Nov 2011 20:33:46
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 260.3kHz
Ch2+Ch3 Pha 44.55 °
28 Nov 2011 20:33:58
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 262.7kHz
Ch2+Ch3 Pha 44.54 °
28 Nov 2011 20:34:04
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 259.0kHz
Ch2+Ch3 Pha 44.59 °
28 Nov 2011 20:34:15
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 299mV
Ch2 Freq 260.3kHz
Ch2+Ch3 Pha 45.22 °
28 Nov 2011 20:34:20
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 301mV
Ch2 Freq 260.8kHz
Ch2+Ch3 Pha 44.89 °
28 Nov 2011 20:34:28
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 261.5kHz
Ch2+Ch3 Pha 44.75 °
28 Nov 2011 20:34:40
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 300mV
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 44.78 °
28 Nov 2011 20:34:55
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 298mV
Ch2 Freq 260.8kHz
Ch2+Ch3 Pha 44.73 °
28 Nov 2011 20:35:29

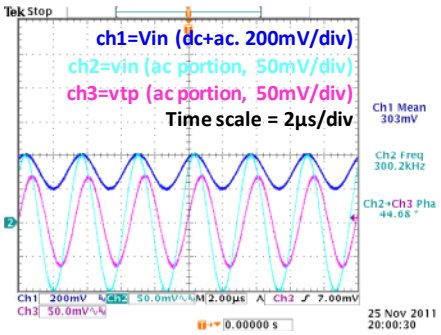
Measurements at PADONLY point with VBIAS=0.3V

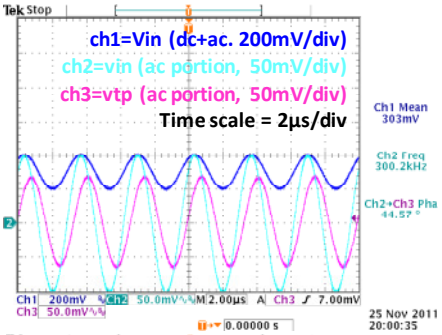
RIN= 4.697E+04

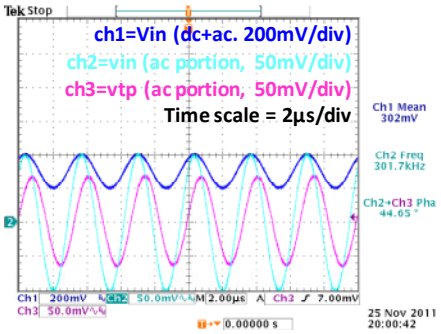
Sample No.	*phase*	*f*	*c*
1	45.23	3.002E+05	1.14E-11
2	45.16	2.997E+05	1.14E-11
3	44.68	3.002E+05	1.12E-11
4	45.57	3.002E+05	1.15E-11
5	44.65	3.017E+05	1.11E-11
6	45.32	3.004E+05	1.14E-11
7	44.80	2.990E+05	1.13E-11
8	44.56	2.995E+05	1.11E-11
9	44.92	2.996E+05	1.13E-11
10	44.98	3.003E+05	1.13E-11
11	45.50	3.010E+05	1.15E-11
12	45.04	3.003E+05	1.13E-11
13	44.79	3.015E+05	1.12E-11
14	44.95	3.018E+05	1.12E-11
15	44.66	3.016E+05	1.11E-11
16	44.56	3.012E+05	1.11E-11
17	44.81	3.002E+05	1.12E-11
18	45.00	3.012E+05	1.12E-11
19	45.30	3.014E+05	1.14E-11
20	44.83	3.020E+05	1.12E-11
Average	44.97	3.007E+05	**1.126E-11**
STD	0.30	8.685E+02	**1.253E-13**

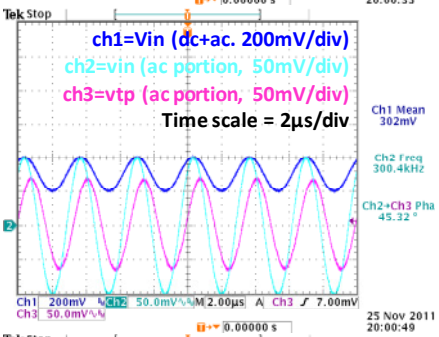


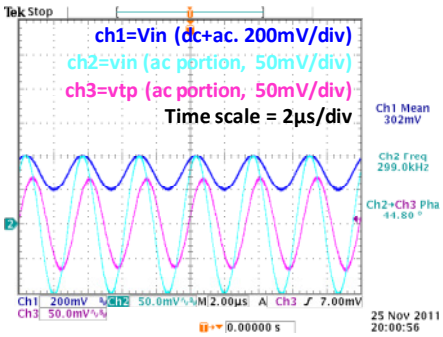


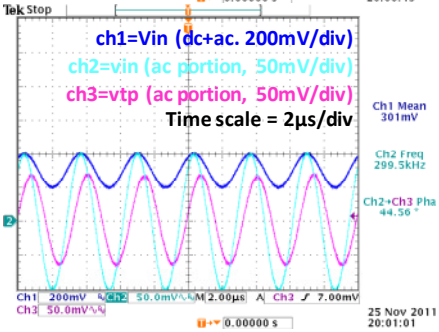


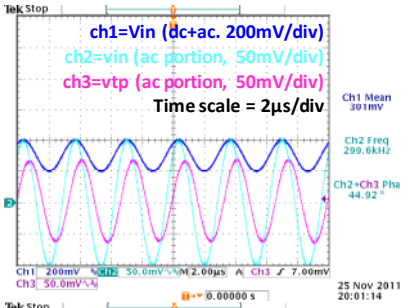


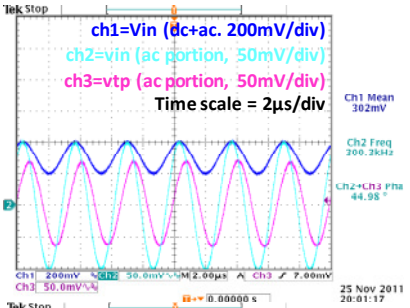


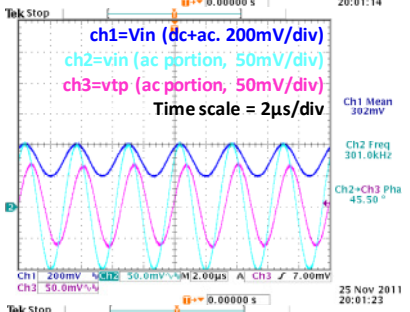


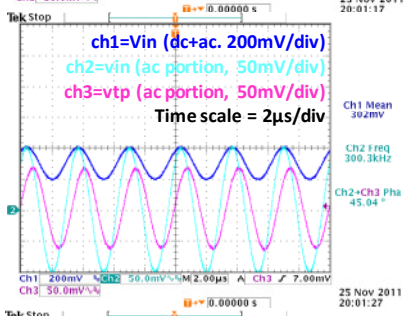


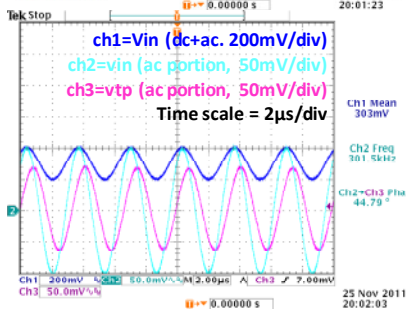


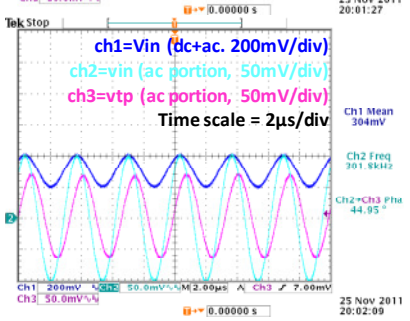

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 301mV
Ch2 Freq 299.6kHz
Ch2+Ch3 Pha 44.92°
25 Nov 2011 20:01:14

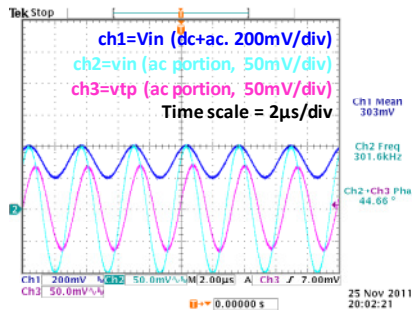

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 302mV
Ch2 Freq 300.2kHz
Ch2+Ch3 Pha 44.98°
25 Nov 2011 20:01:17

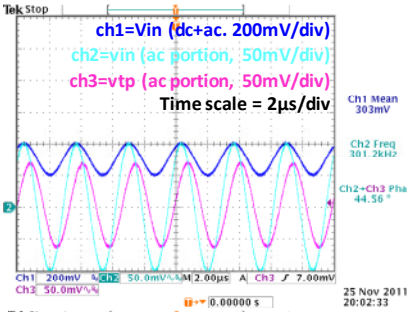

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 302mV
Ch2 Freq 301.0kHz
Ch2+Ch3 Pha 45.50°
25 Nov 2011 20:01:23

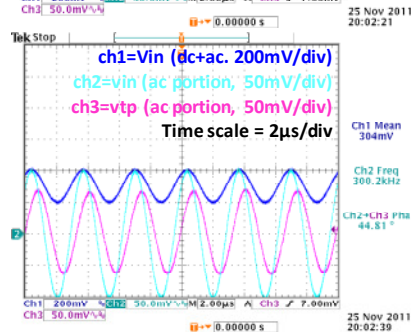

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 302mV
Ch2 Freq 300.3kHz
Ch2+Ch3 Pha 45.04°
25 Nov 2011 20:01:27

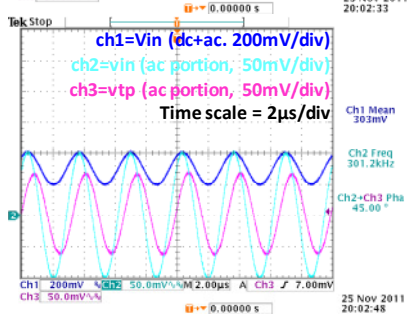

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 303mV
Ch2 Freq 301.5kHz
Ch2+Ch3 Pha 44.79°
25 Nov 2011 20:02:03

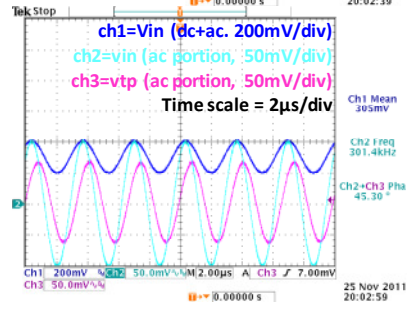

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 304mV
Ch2 Freq 301.5kHz
Ch2+Ch3 Pha 44.95°
25 Nov 2011 20:02:09

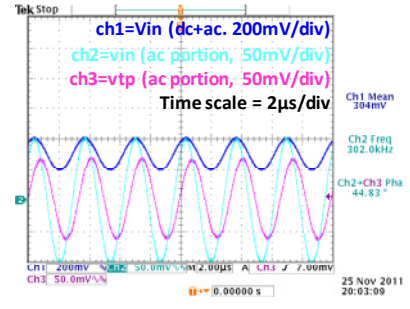

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 303mV
Ch2 Freq 301.6kHz
Ch2+Ch3 Pha 44.66°
25 Nov 2011 20:02:21


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 303mV
Ch2 Freq 301.2kHz
Ch2+Ch3 Pha 44.56°
25 Nov 2011 20:02:33


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 304mV
Ch2 Freq 300.2kHz
Ch2+Ch3 Pha 44.81°
25 Nov 2011 20:02:39


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 303mV
Ch2 Freq 301.2kHz
Ch2+Ch3 Pha 45.00°
25 Nov 2011 20:02:48

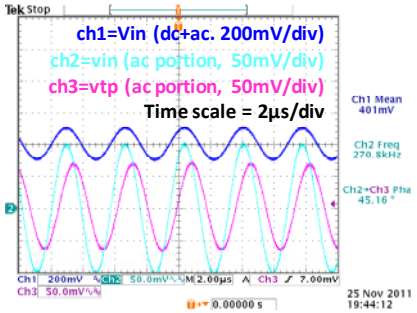

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 305mV
Ch2 Freq 301.4kHz
Ch2+Ch3 Pha 45.30°
25 Nov 2011 20:02:59

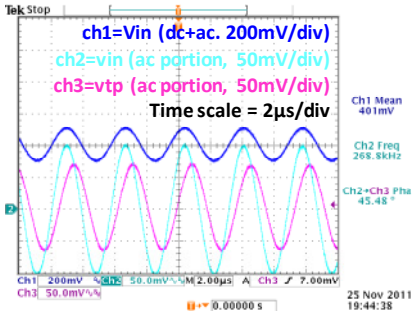

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 304mV
Ch2 Freq 302.0kHz
Ch2+Ch3 Pha 44.83°
25 Nov 2011 20:03:09

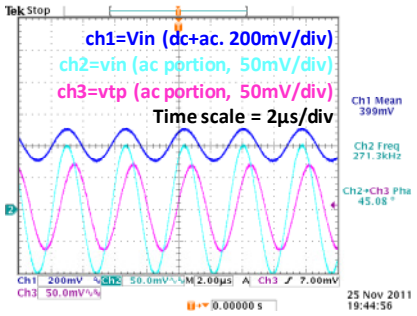
Measurements at NoQFG point with VBIAS=0.4V

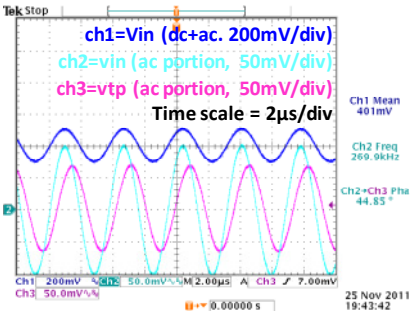
RIN= 4.697E+04

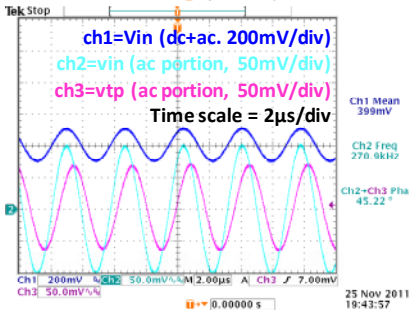
Sample No.	*phase*	*f*	*c*
1	44.85	2.699E+05	1.25E-11
2	45.22	2.709E+05	1.26E-11
3	44.68	2.688E+05	1.25E-11
4	45.16	2.708E+05	1.26E-11
5	44.68	2.690E+05	1.25E-11
6	45.48	2.688E+05	1.28E-11
7	44.98	2.705E+05	1.25E-11
8	45.08	2.713E+05	1.25E-11
9	45.23	2.700E+05	1.27E-11
10	45.25	2.687E+05	1.27E-11
11	44.81	2.703E+05	1.25E-11
12	45.02	2.710E+05	1.25E-11
13	44.94	2.702E+05	1.25E-11
14	45.11	2.699E+05	1.26E-11
15	45.48	2.715E+05	1.27E-11
16	44.94	2.709E+05	1.25E-11
17	45.42	2.706E+05	1.27E-11
18	44.56	2.714E+05	1.23E-11
19	44.63	2.718E+05	1.23E-11
20	45.23	2.710E+05	1.26E-11
Average	45.04	2.704E+05	**1.255E-11**
STD	0.28	9.477E+02	**1.315E-13**

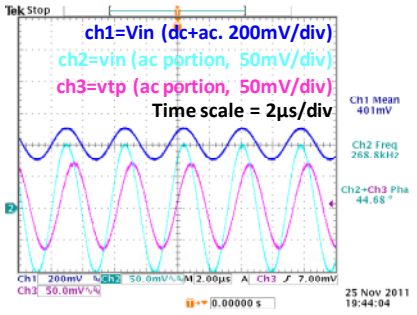


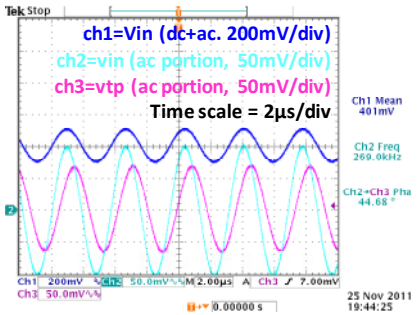


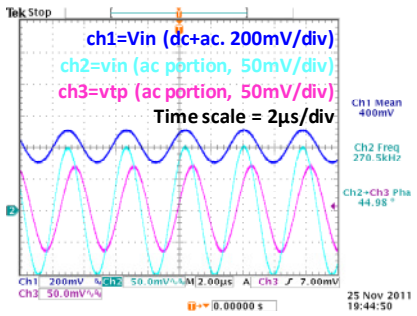


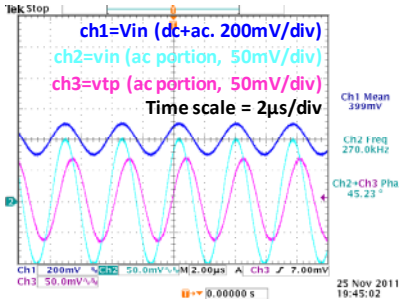


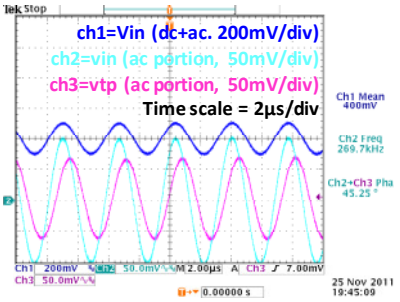


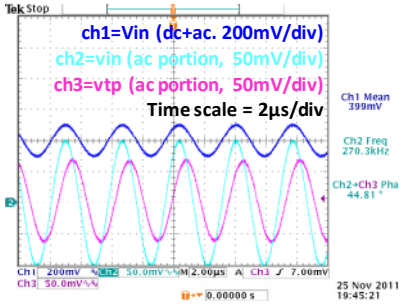


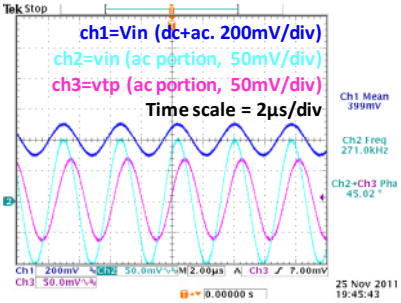


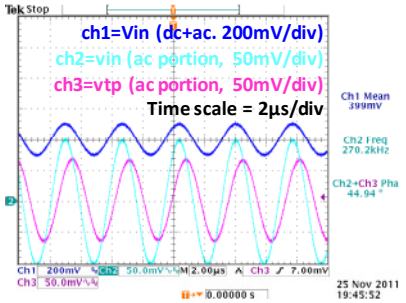


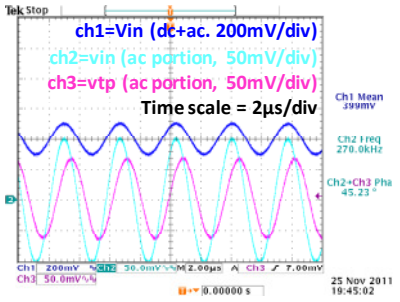

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.0kHz
Ch2+Ch3 Pha 45.23 °
25 Nov 2011 19:45:02

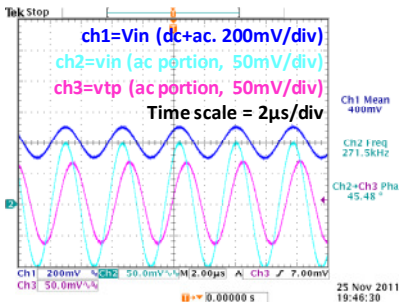

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 400mV
Ch2 Freq 269.7kHz
Ch2+Ch3 Pha 45.25 °
25 Nov 2011 19:45:09

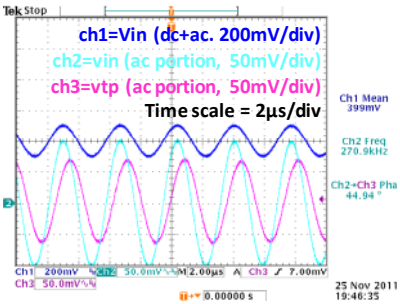

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.3kHz
Ch2+Ch3 Pha 44.81 °
25 Nov 2011 19:45:21

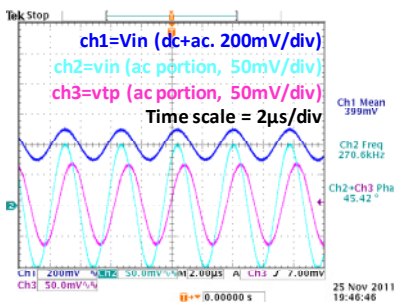

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 271.0kHz
Ch2+Ch3 Pha 45.02 °
25 Nov 2011 19:45:43

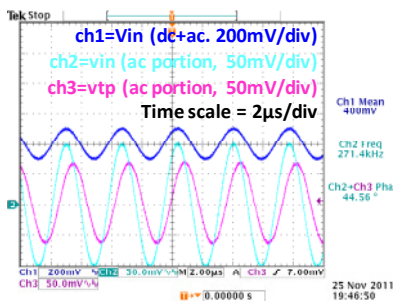

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.2kHz
Ch2+Ch3 Pha 44.94 °
25 Nov 2011 19:45:52

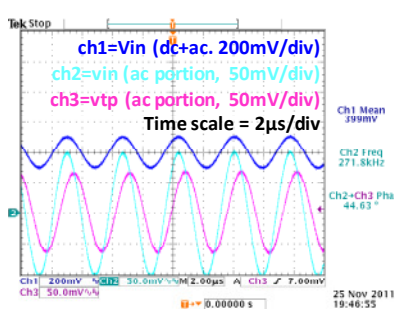

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.0kHz
Ch2+Ch3 Pha 45.23 °
25 Nov 2011 19:45:02

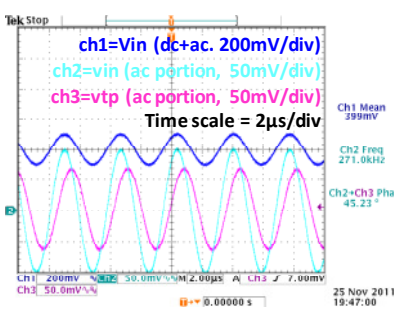

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 400mV
Ch2 Freq 271.5kHz
Ch2+Ch3 Pha 45.48 °
25 Nov 2011 19:46:30


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.9kHz
Ch2+Ch3 Pha 44.94 °
25 Nov 2011 19:46:35


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 270.6kHz
Ch2+Ch3 Pha 45.42 °
25 Nov 2011 19:46:46


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 400mV
Ch2 Freq 271.4kHz
Ch2+Ch3 Pha 44.56 °
25 Nov 2011 19:46:50

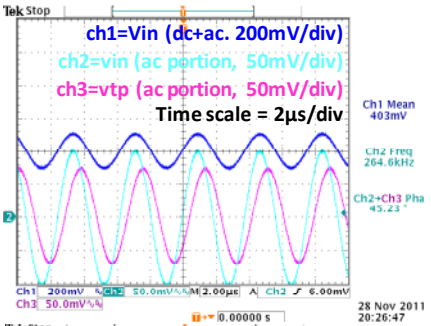

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 271.8kHz
Ch2+Ch3 Pha 44.63 °
25 Nov 2011 19:46:55

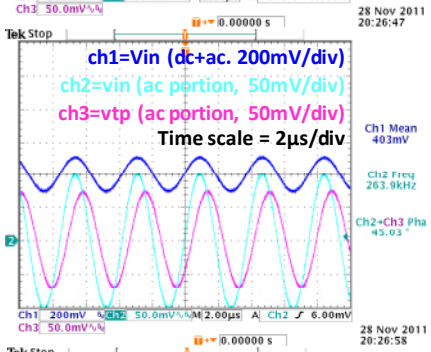

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 399mV
Ch2 Freq 271.0kHz
Ch2+Ch3 Pha 45.23 °
25 Nov 2011 19:47:00

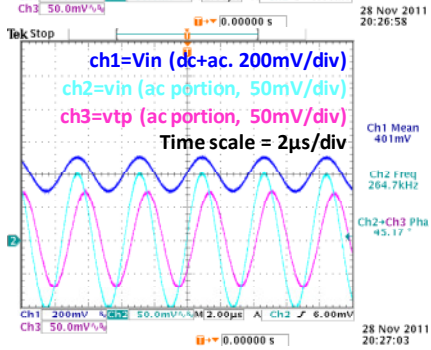
Measurements at QFG point with VBIAS=0.4V

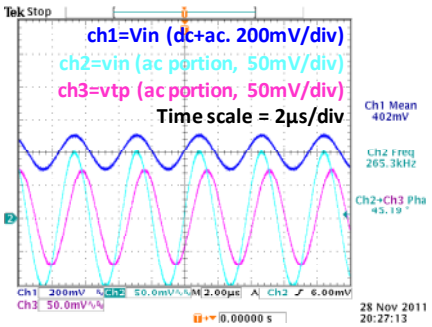
RIN= 4.697E+04

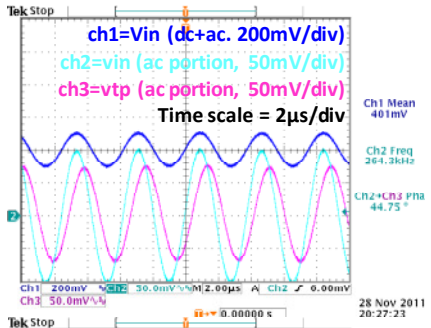
Sample No.	*phase*	*f*	*c*
1	45.23	2.646E+05	1.29E-11
2	45.03	2.639E+05	1.29E-11
3	45.17	2.647E+05	1.29E-11
4	45.19	2.653E+05	1.29E-11
5	44.75	2.643E+05	1.27E-11
6	44.73	2.651E+05	1.27E-11
7	45.02	2.644E+05	1.28E-11
8	44.54	2.646E+05	1.26E-11
9	45.07	2.642E+05	1.29E-11
10	45.38	2.648E+05	1.30E-11
11	44.72	2.649E+05	1.27E-11
12	44.84	2.641E+05	1.28E-11
13	44.62	2.649E+05	1.26E-11
14	44.84	2.651E+05	1.27E-11
15	45.43	2.654E+05	1.30E-11
16	44.60	2.655E+05	1.26E-11
17	45.43	2.649E+05	1.30E-11
18	44.88	2.645E+05	1.28E-11
19	44.59	2.658E+05	1.26E-11
20	44.84	2.643E+05	1.27E-11
Average	44.95	2.648E+05	**1.277E-11**
STD	0.29	5.019E+02	**1.322E-13**

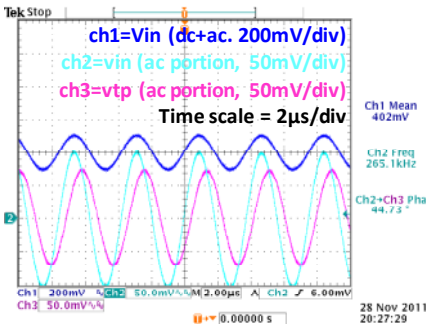


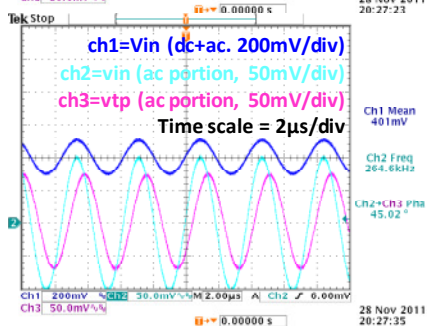


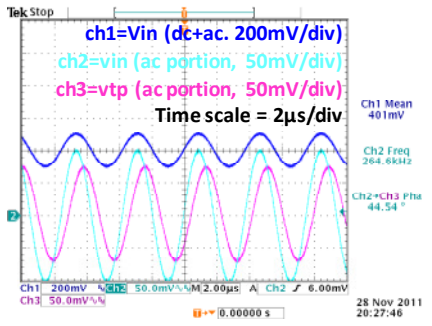


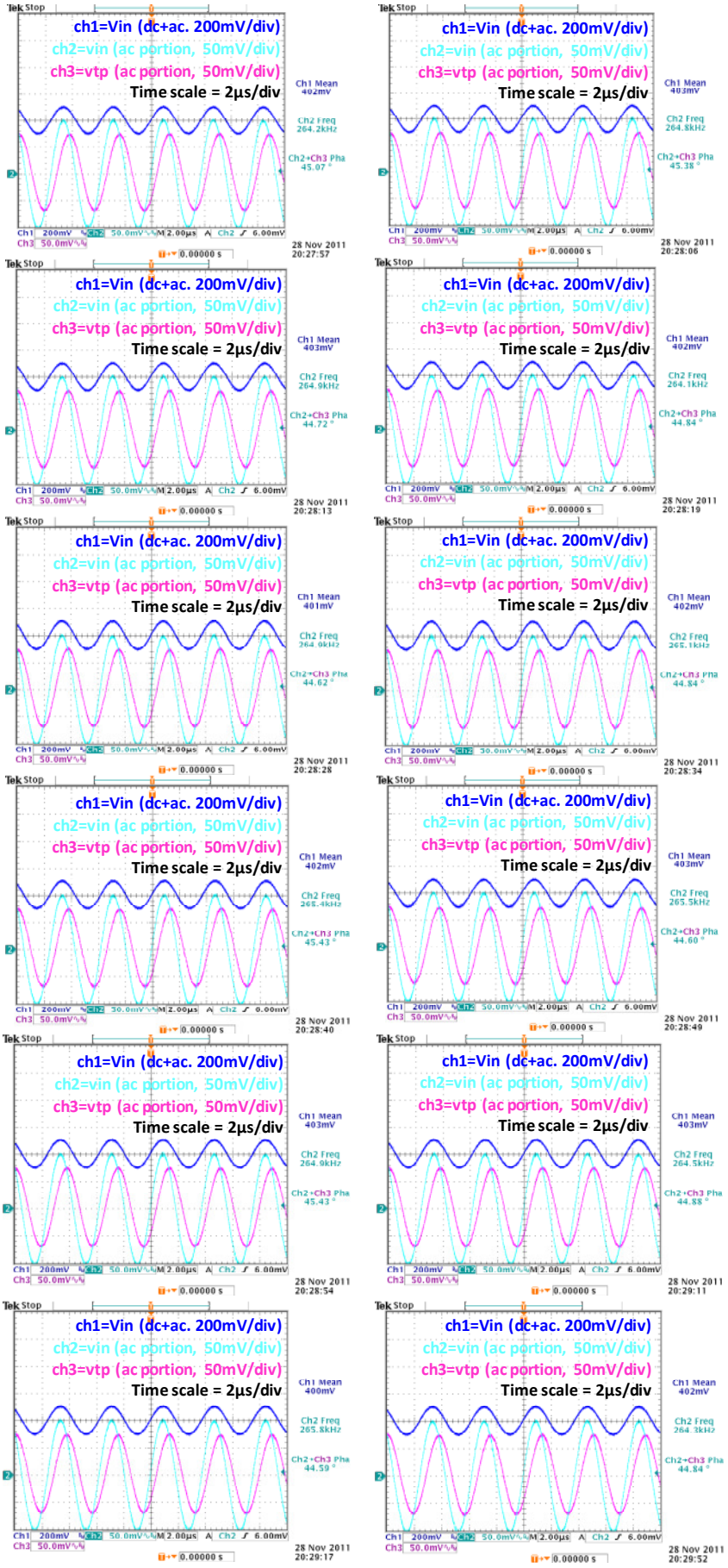








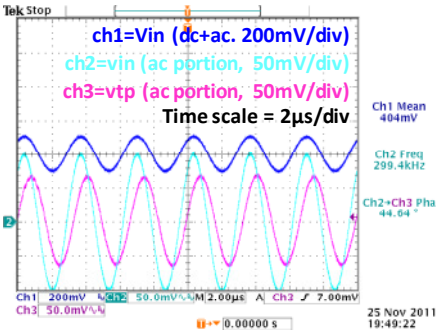


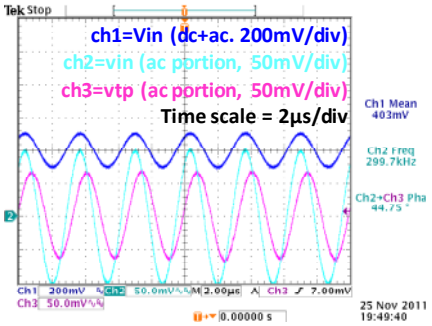

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 402mV
Ch2 Freq 264.2kHz
Ch2+Ch3 Pha 45.07 °
28 Nov 2011 20:27:57
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 264.8kHz
Ch2+Ch3 Pha 45.38 °
28 Nov 2011 20:28:06
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 264.9kHz
Ch2+Ch3 Pha 44.72 °
28 Nov 2011 20:28:13
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 402mV
Ch2 Freq 264.1kHz
Ch2+Ch3 Pha 44.84 °
28 Nov 2011 20:28:19
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 401mV
Ch2 Freq 264.9kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 20:28:28
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 402mV
Ch2 Freq 265.1kHz
Ch2+Ch3 Pha 44.84 °
28 Nov 2011 20:28:34
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 402mV
Ch2 Freq 265.4kHz
Ch2+Ch3 Pha 45.43 °
28 Nov 2011 20:28:40
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 265.5kHz
Ch2+Ch3 Pha 44.60 °
28 Nov 2011 20:28:49
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 264.9kHz
Ch2+Ch3 Pha 45.43 °
28 Nov 2011 20:28:54
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 264.5kHz
Ch2+Ch3 Pha 44.88 °
28 Nov 2011 20:29:11
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 400mV
Ch2 Freq 265.8kHz
Ch2+Ch3 Pha 44.59 °
28 Nov 2011 20:29:17
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 402mV
Ch2 Freq 264.3kHz
Ch2+Ch3 Pha 44.84 °
28 Nov 2011 20:29:52

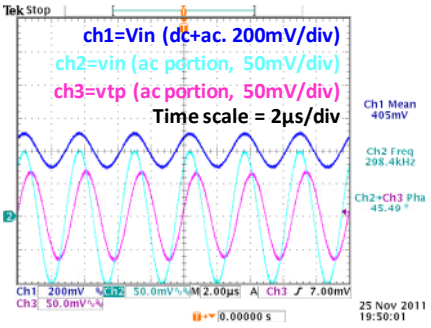
Measurements at PADONLY point with VBIAS=0.4V

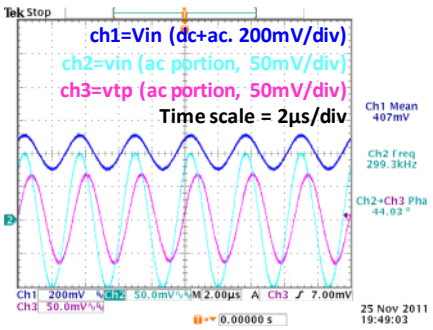
RIN= 4.697E+04

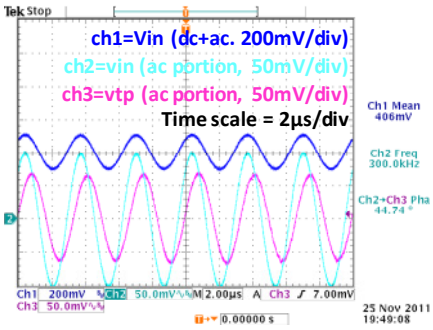
Sample No.	*phase*	*f*	*c*
1	44.93	2.993E+05	1.13E-11
2	44.74	3.000E+05	1.12E-11
3	44.64	2.994E+05	1.12E-11
4	44.64	3.007E+05	1.11E-11
5	44.64	3.007E+05	1.11E-11
6	44.75	2.997E+05	1.12E-11
7	44.75	3.010E+05	1.12E-11
8	45.49	2.984E+05	1.16E-11
9	44.81	2.987E+05	1.13E-11
10	44.67	2.990E+05	1.12E-11
11	44.84	2.993E+05	1.13E-11
12	44.60	2.999E+05	1.11E-11
13	45.23	3.005E+05	1.14E-11
14	44.50	3.005E+05	1.11E-11
15	45.34	3.009E+05	1.14E-11
16	45.10	3.005E+05	1.13E-11
17	44.64	3.017E+05	1.11E-11
18	45.39	2.991E+05	1.15E-11
19	45.11	3.001E+05	1.13E-11
20	44.93	3.004E+05	1.13E-11
Average	44.89	3.000E+05	**1.125E-11**
STD	0.29	8.614E+02	**1.278E-13**

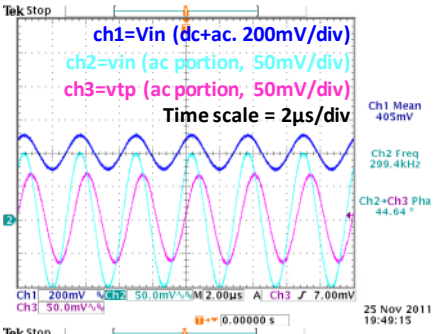


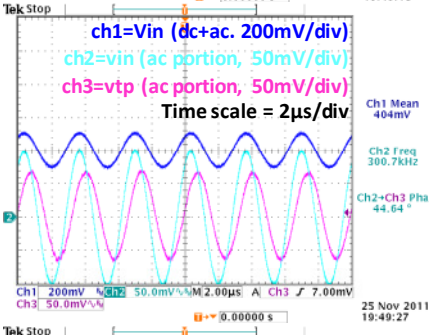


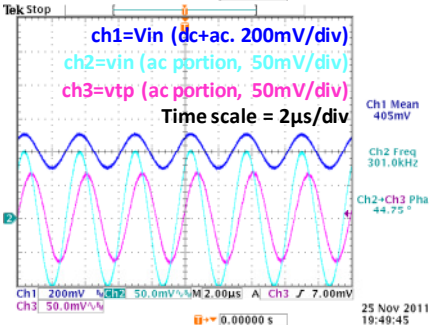


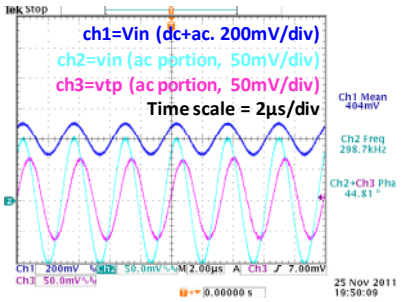


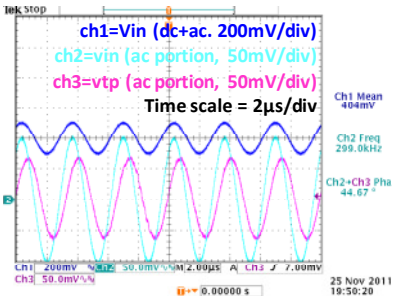


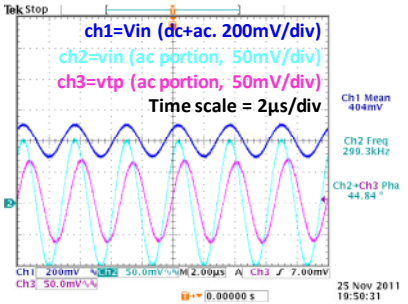


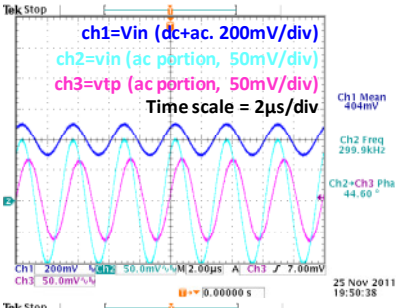


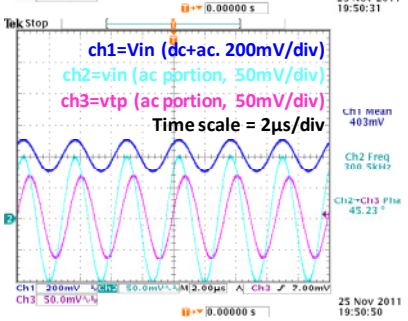


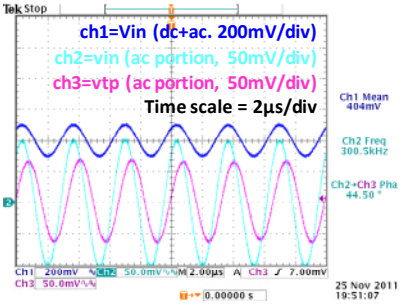

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 298.7kHz
Ch2+Ch3 Pha 44.81°
25 Nov 2011 19:50:09

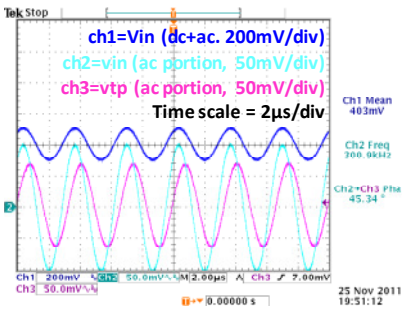

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 299.0kHz
Ch2+Ch3 Pha 44.67°
25 Nov 2011 19:50:20

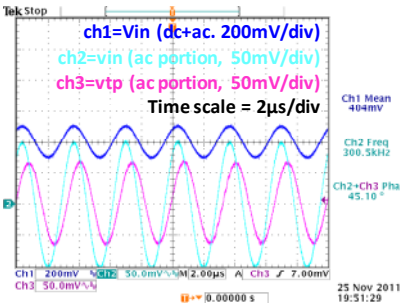

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 299.3kHz
Ch2+Ch3 Pha 44.84°
25 Nov 2011 19:50:31

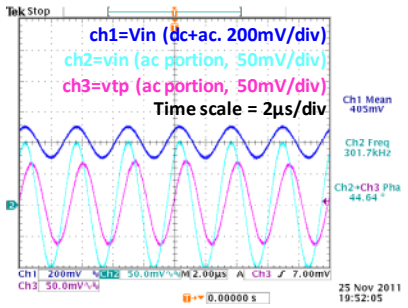

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 299.9kHz
Ch2+Ch3 Pha 44.60°
25 Nov 2011 19:50:38

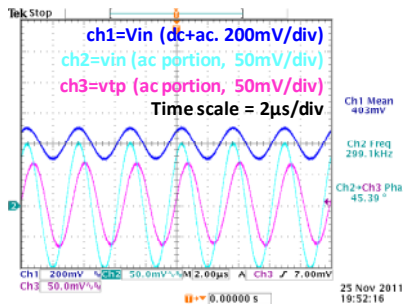

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 300.5kHz
Ch2+Ch3 Pha 45.23°
25 Nov 2011 19:50:50

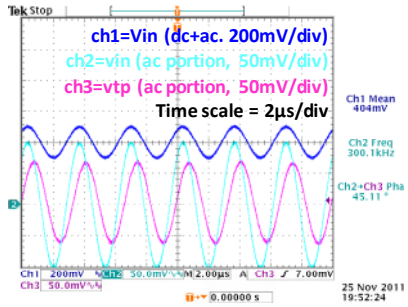

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 300.5kHz
Ch2+Ch3 Pha 44.50°
25 Nov 2011 19:51:07

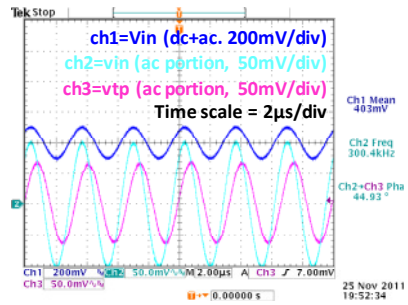

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 300.0kHz
Ch2+Ch3 Pha 45.34°
25 Nov 2011 19:51:12


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 300.5kHz
Ch2+Ch3 Pha 45.10°
25 Nov 2011 19:51:29


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 405mV
Ch2 Freq 301.7kHz
Ch2+Ch3 Pha 44.64°
25 Nov 2011 19:52:05


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 299.1kHz
Ch2+Ch3 Pha 45.30°
25 Nov 2011 19:52:16

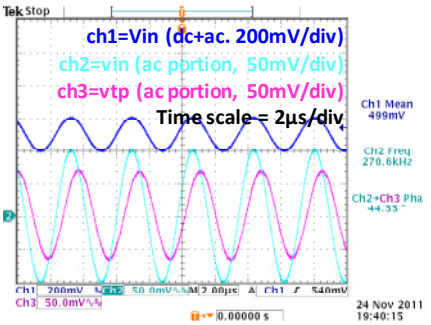

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 404mV
Ch2 Freq 300.1kHz
Ch2+Ch3 Pha 45.11°
25 Nov 2011 19:52:24

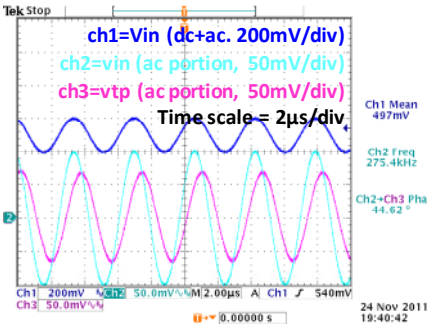

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 403mV
Ch2 Freq 300.4kHz
Ch2+Ch3 Pha 44.93°
25 Nov 2011 19:52:34

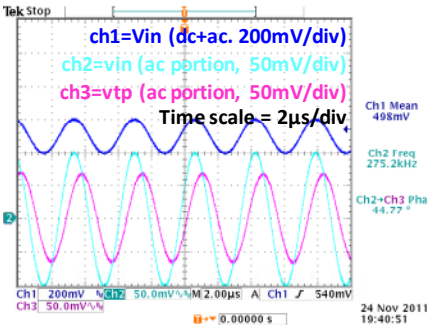
Measurements at NoQFG point with VBIAS=0.5V

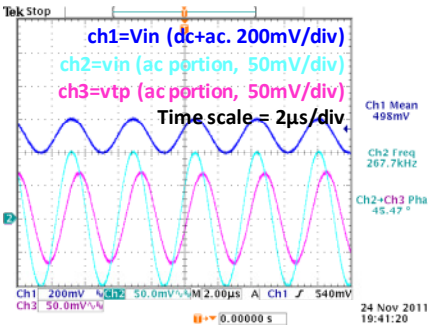
RIN= 4.697E+04

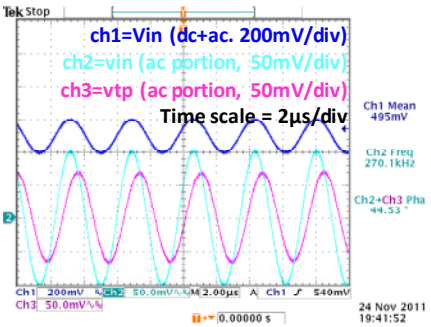
Sample No.	*phase*	*f*	*c*
1	44.55	2.706E+05	1.23E-11
2	44.62	2.754E+05	1.21E-11
3	44.77	2.752E+05	1.22E-11
4	45.80	2.678E+05	1.30E-11
5	45.47	2.677E+05	1.29E-11
6	45.02	2.695E+05	1.26E-11
7	44.53	2.701E+05	1.23E-11
8	45.22	2.678E+05	1.28E-11
9	45.42	2.693E+05	1.28E-11
10	45.25	2.695E+05	1.27E-11
11	44.52	2.699E+05	1.23E-11
12	44.87	2.697E+05	1.25E-11
13	44.63	2.703E+05	1.24E-11
14	44.83	2.709E+05	1.24E-11
15	44.60	2.705E+05	1.24E-11
16	45.33	2.708E+05	1.27E-11
17	45.38	2.699E+05	1.27E-11
18	45.24	2.722E+05	1.26E-11
19	45.44	2.707E+05	1.27E-11
20	44.63	2.713E+05	1.23E-11
Average	45.01	2.705E+05	**1.253E-11**
STD	0.40	2.017E+03	**2.328E-13**

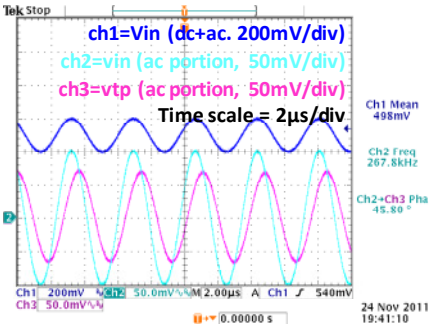


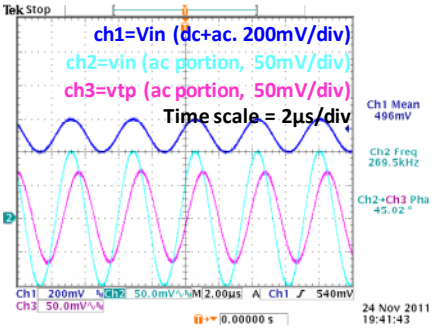


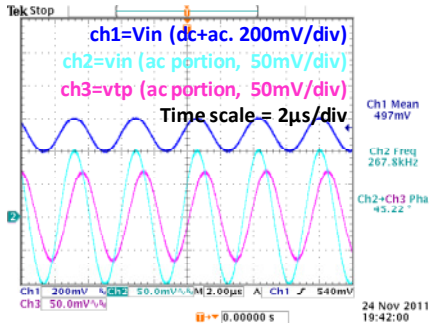


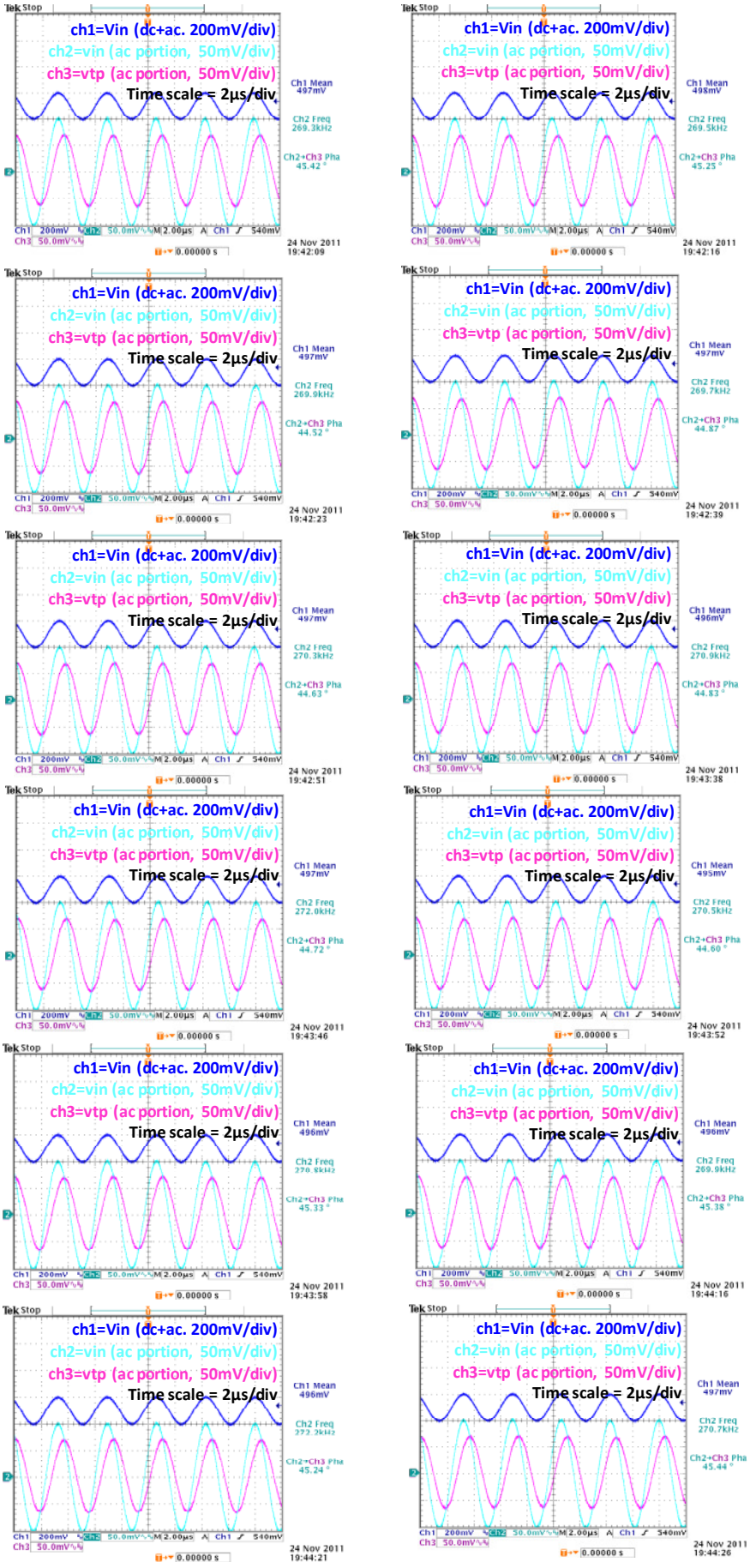








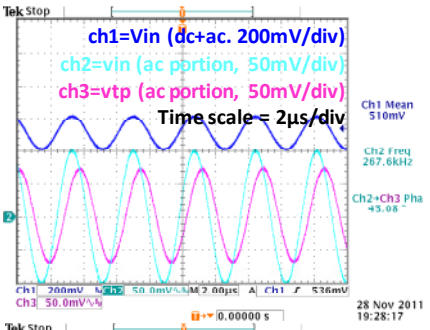


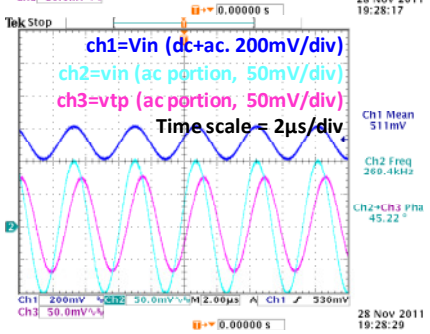

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 497mV
Ch2 Freq 269.3kHz
Ch2+Ch3 Pha 45.42 °
24 Nov 2011 19:42:09
Ch1 Mean 498mV
Ch2 Freq 269.5kHz
Ch2+Ch3 Pha 45.25 °
24 Nov 2011 19:42:16
Ch1 Mean 497mV
Ch2 Freq 269.9kHz
Ch2+Ch3 Pha 44.52 °
24 Nov 2011 19:42:23
Ch1 Mean 497mV
Ch2 Freq 269.7kHz
Ch2+Ch3 Pha 44.87 °
24 Nov 2011 19:42:39
Ch1 Mean 497mV
Ch2 Freq 270.3kHz
Ch2+Ch3 Pha 44.63 °
24 Nov 2011 19:42:51
Ch1 Mean 496mV
Ch2 Freq 270.9kHz
Ch2+Ch3 Pha 44.83 °
24 Nov 2011 19:43:38
Ch1 Mean 497mV
Ch2 Freq 272.0kHz
Ch2+Ch3 Pha 44.72 °
24 Nov 2011 19:43:46
Ch1 Mean 495mV
Ch2 Freq 270.5kHz
Ch2+Ch3 Pha 44.60 °
24 Nov 2011 19:43:52
Ch1 Mean 496mV
Ch2 Freq 270.8kHz
Ch2+Ch3 Pha 45.33 °
24 Nov 2011 19:43:58
Ch1 Mean 496mV
Ch2 Freq 269.9kHz
Ch2+Ch3 Pha 45.38 °
24 Nov 2011 19:44:16
Ch1 Mean 496mV
Ch2 Freq 272.2kHz
Ch2+Ch3 Pha 45.24 °
24 Nov 2011 19:44:21
Ch1 Mean 497mV
Ch2 Freq 270.7kHz
Ch2+Ch3 Pha 45.44 °
24 Nov 2011 19:44:26

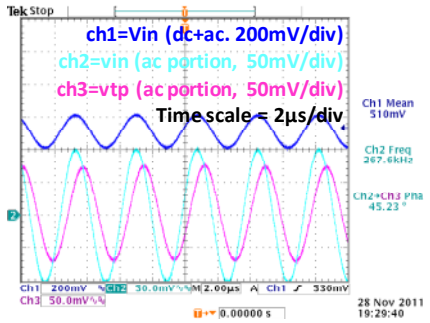
Measurements at QFG point with VBIAS=0.5V

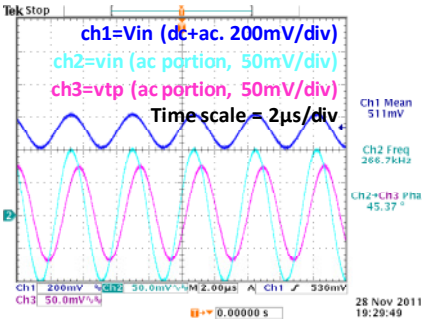
RIN= 4.697E+04

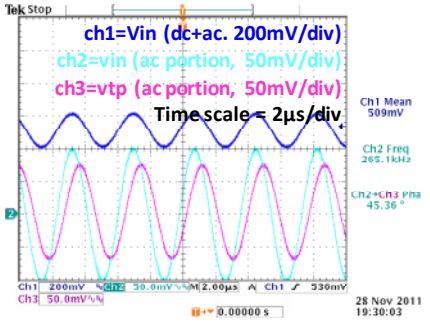
Sample No.	*phase*	*f*	*c*
1	45.08	2.676E+05	1.27E-11
2	45.22	2.694E+05	1.27E-11
3	45.23	2.677E+05	1.28E-11
4	45.37	2.667E+05	1.29E-11
5	45.36	2.651E+05	1.29E-11
6	44.71	2.639E+05	1.27E-11
7	45.29	2.650E+05	1.29E-11
8	44.81	2.643E+05	1.27E-11
9	45.41	2.648E+05	1.30E-11
10	45.09	2.659E+05	1.28E-11
11	44.54	2.667E+05	1.25E-11
12	44.91	2.652E+05	1.27E-11
13	44.73	2.656E+05	1.26E-11
14	44.84	2.646E+05	1.27E-11
15	45.52	2.643E+05	1.31E-11
16	45.12	2.639E+05	1.29E-11
17	44.50	2.653E+05	1.26E-11
18	44.74	2.650E+05	1.27E-11
19	45.15	2.646E+05	1.29E-11
20	44.96	2.654E+05	1.27E-11
Average	45.03	2.656E+05	**1.277E-11**
STD	0.30	1.421E+03	**1.417E-13**

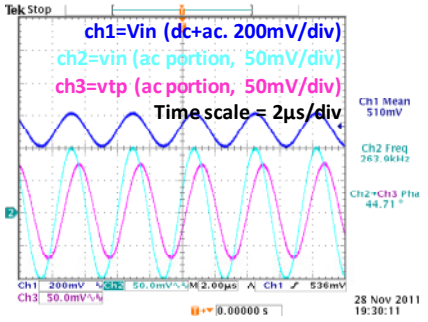


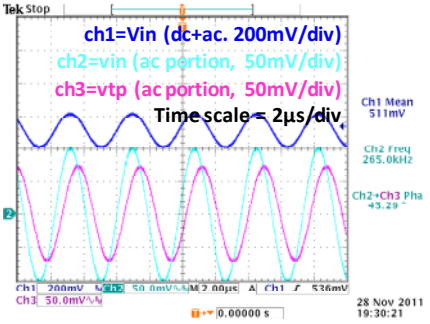


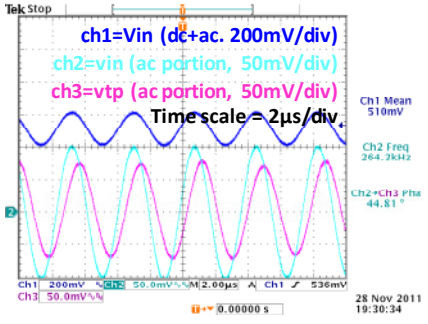


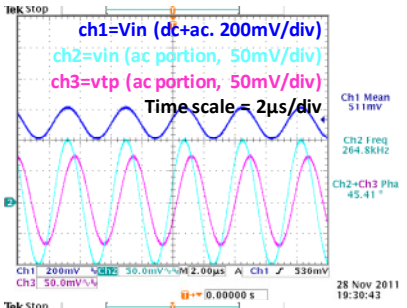


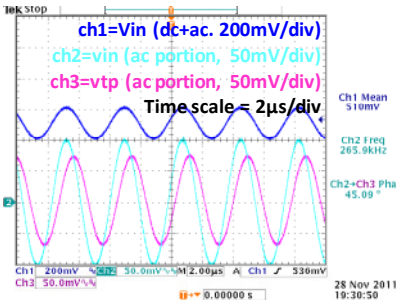


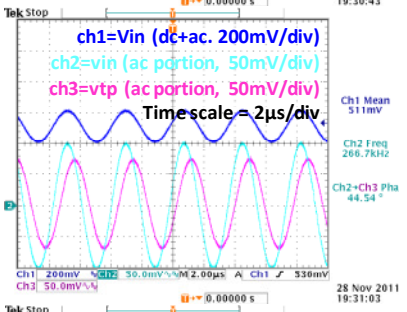


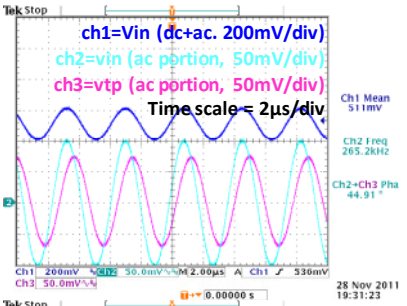


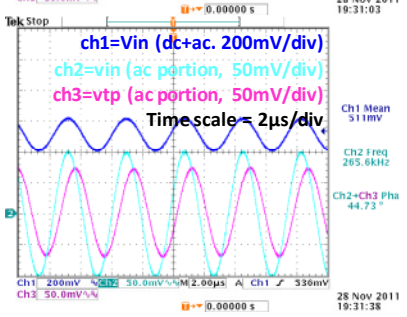


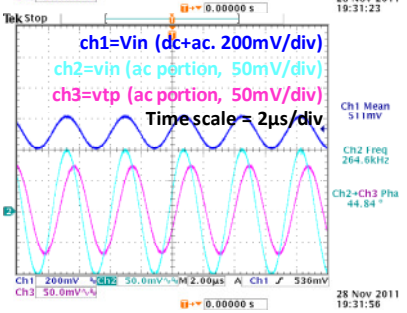

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 264.8kHz
Ch2+Ch3 Pha 45.41 °
28 Nov 2011
19:30:43

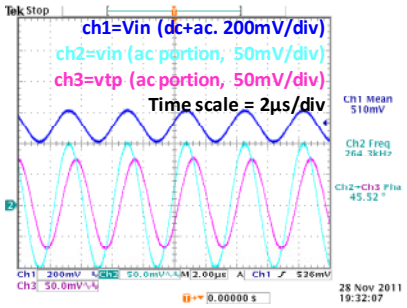

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 510mV
Ch2 Freq 265.9kHz
Ch2+Ch3 Pha 45.09 °
28 Nov 2011
19:30:50

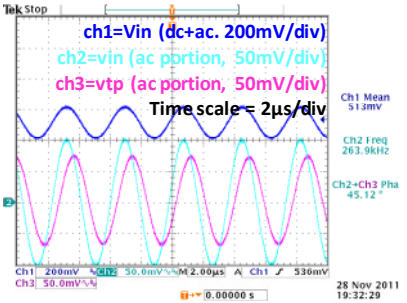

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 266.7kHz
Ch2+Ch3 Pha 44.54 °
28 Nov 2011
19:31:03

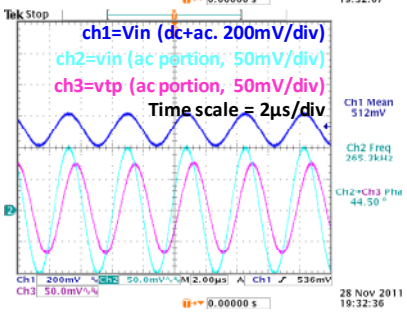

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 265.2kHz
Ch2+Ch3 Pha 44.91 °
28 Nov 2011
19:31:23

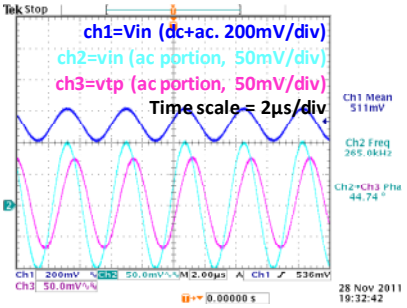

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 265.6kHz
Ch2+Ch3 Pha 44.73 °
28 Nov 2011
19:31:38

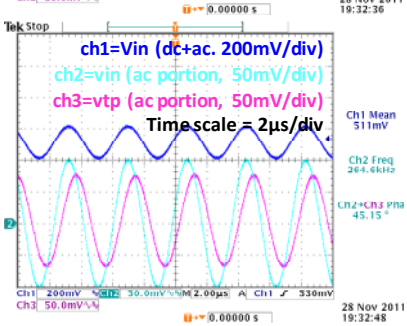

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 264.6kHz
Ch2+Ch3 Pha 44.84 °
28 Nov 2011
19:31:56

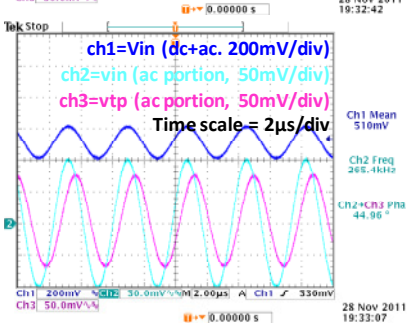

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 510mV
Ch2 Freq 264.3kHz
Ch2+Ch3 Pha 45.52 °
28 Nov 2011
19:32:07


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 513mV
Ch2 Freq 263.9kHz
Ch2+Ch3 Pha 45.12 °
28 Nov 2011
19:32:29


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 512mV
Ch2 Freq 265.3kHz
Ch2+Ch3 Pha 44.50 °
28 Nov 2011
19:32:36


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 265.0kHz
Ch2+Ch3 Pha 44.74 °
28 Nov 2011
19:32:42

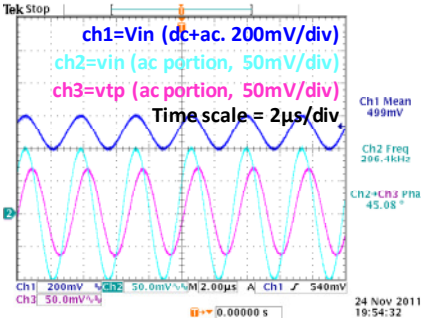

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 511mV
Ch2 Freq 264.6kHz
Ch2+Ch3 Pha 45.15 °
28 Nov 2011
19:32:48

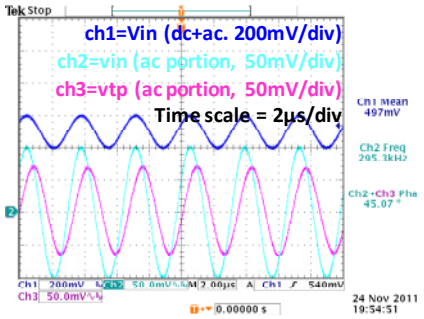

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 510mV
Ch2 Freq 265.4kHz
Ch2+Ch3 Pha 44.96 °
28 Nov 2011
19:33:07

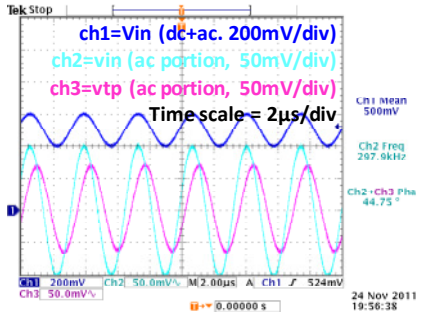
Measurements at PADONLY point with VBIAS=0.5V

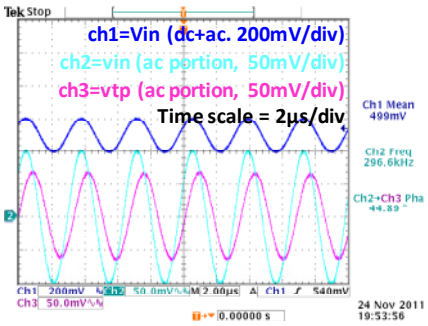
RIN= 4.697E+04

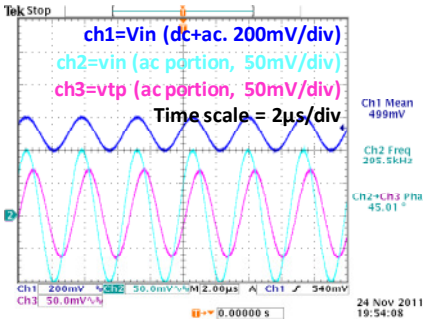
Sample No.	*phase*	*f*	*c*
1	44.89	2.966E+05	1.14E-11
2	45.01	2.955E+05	1.15E-11
3	44.91	2.972E+05	1.14E-11
4	45.08	2.964E+05	1.15E-11
5	45.45	2.950E+05	1.17E-11
6	45.07	2.953E+05	1.15E-11
7	45.42	2.952E+05	1.16E-11
8	44.75	2.979E+05	1.13E-11
9	45.16	2.956E+05	1.15E-11
10	45.40	2.971E+05	1.16E-11
11	45.12	2.958E+05	1.15E-11
12	44.99	2.967E+05	1.14E-11
13	44.56	2.955E+05	1.13E-11
14	45.04	2.975E+05	1.14E-11
15	45.51	2.966E+05	1.16E-11
16	45.08	2.963E+05	1.15E-11
17	45.45	2.960E+05	1.16E-11
18	44.95	2.960E+05	1.14E-11
19	44.79	2.968E+05	1.13E-11
20	45.20	2.964E+05	1.15E-11
Average	45.09	2.963E+05	**1.147E-11**
STD	0.26	7.994E+02	**1.155E-13**

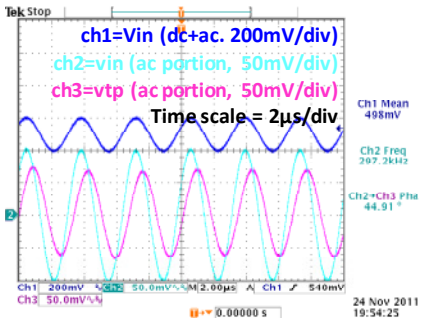


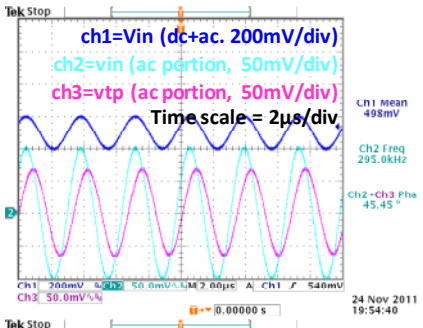


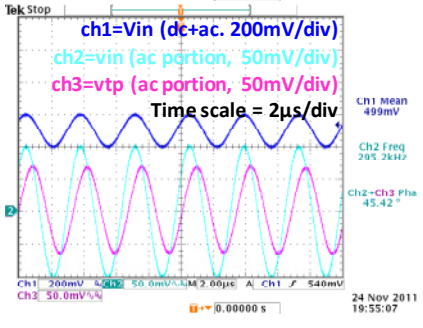


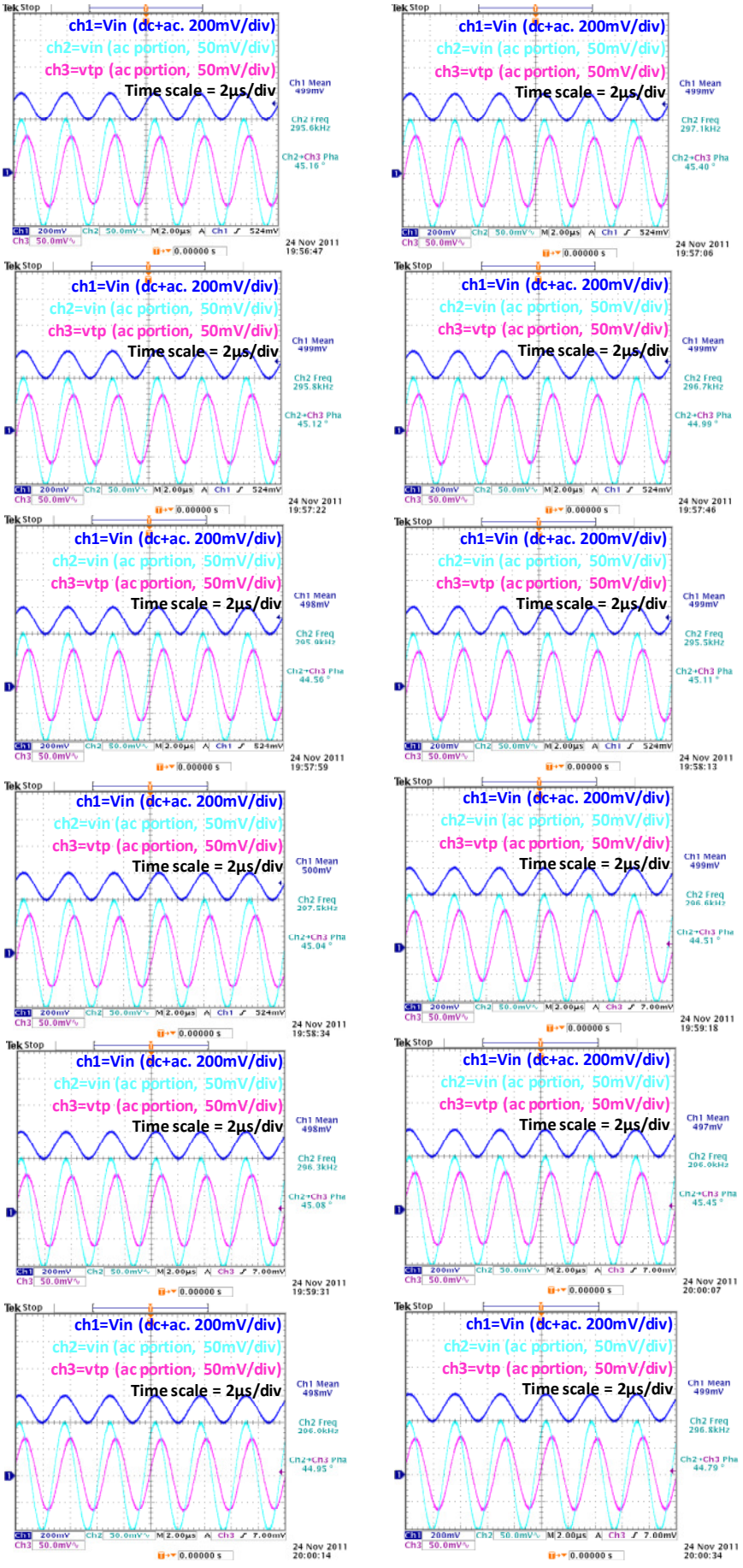








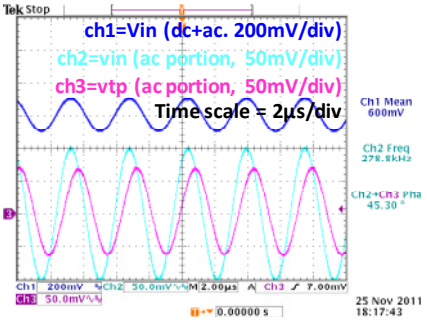


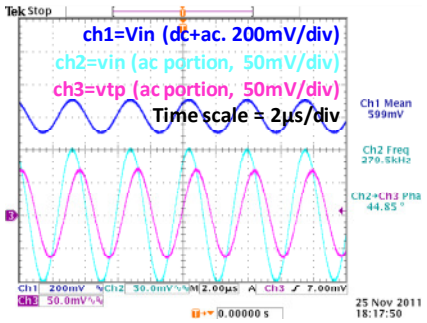

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 295.6kHz
Ch2+Ch3 Pha 45.16 °
24 Nov 2011 19:56:47
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 297.1kHz
Ch2+Ch3 Pha 45.40 °
24 Nov 2011 19:57:06
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 295.8kHz
Ch2+Ch3 Pha 45.12 °
24 Nov 2011 19:57:22
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 296.7kHz
Ch2+Ch3 Pha 44.99 °
24 Nov 2011 19:57:46
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 295.0kHz
Ch2+Ch3 Pha 44.56 °
24 Nov 2011 19:57:59
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 295.5kHz
Ch2+Ch3 Pha 45.11 °
24 Nov 2011 19:58:13
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 297.5kHz
Ch2+Ch3 Pha 45.04 °
24 Nov 2011 19:58:34
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 296.6kHz
Ch2+Ch3 Pha 44.51 °
24 Nov 2011 19:59:18
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 296.3kHz
Ch2+Ch3 Pha 45.08 °
24 Nov 2011 19:59:31
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 497mV
Ch2 Freq 296.0kHz
Ch2+Ch3 Pha 45.45 °
24 Nov 2011 20:00:07
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 296.0kHz
Ch2+Ch3 Pha 44.95 °
24 Nov 2011 20:00:14
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 296.8kHz
Ch2+Ch3 Pha 44.79 °
24 Nov 2011 20:00:34

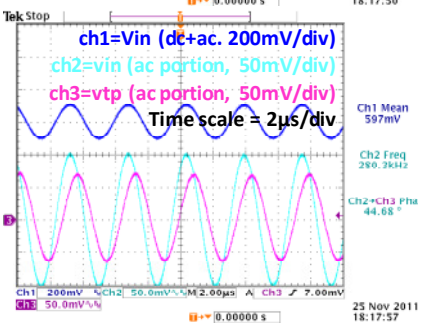
Measurements at NoQFG point with VBIAS=0.6V

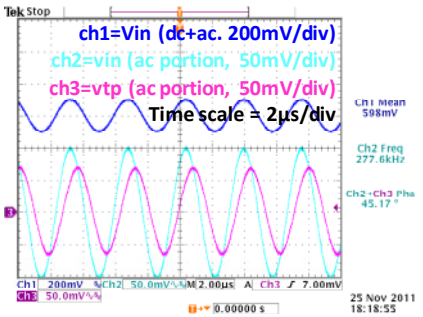
RIN= 4.697E+04

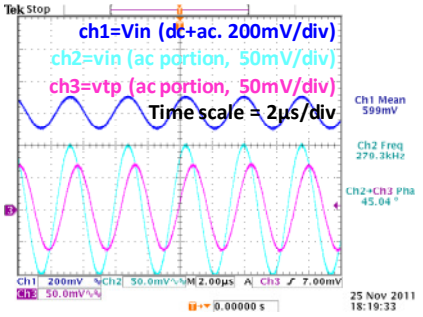
Sample No.	*phase*	*f*	*c*
1	45.30	2.788E+05	1.23E-11
2	44.85	2.795E+05	1.21E-11
3	44.68	2.803E+05	1.20E-11
4	45.04	2.814E+05	1.21E-11
5	45.17	2.776E+05	1.23E-11
6	45.00	2.778E+05	1.22E-11
7	45.04	2.793E+05	1.21E-11
8	45.07	2.771E+05	1.23E-11
9	45.37	2.788E+05	1.23E-11
10	44.62	2.772E+05	1.21E-11
11	45.06	2.779E+05	1.22E-11
12	44.58	2.786E+05	1.20E-11
13	44.55	2.784E+05	1.20E-11
14	44.99	2.783E+05	1.22E-11
15	44.74	2.782E+05	1.21E-11
16	44.93	2.767E+05	1.22E-11
17	45.07	2.780E+05	1.22E-11
18	44.98	2.792E+05	1.21E-11
19	44.63	2.779E+05	1.20E-11
20	44.79	2.790E+05	1.21E-11
Average	44.92	2.785E+05	**1.213E-11**
STD	0.24	1.113E+03	**1.100E-13**

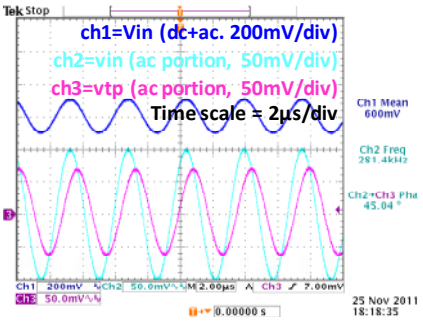


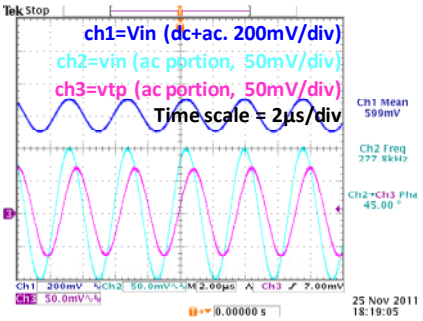


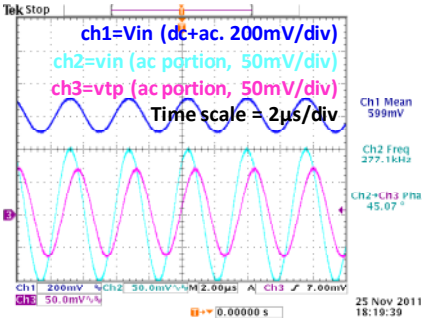


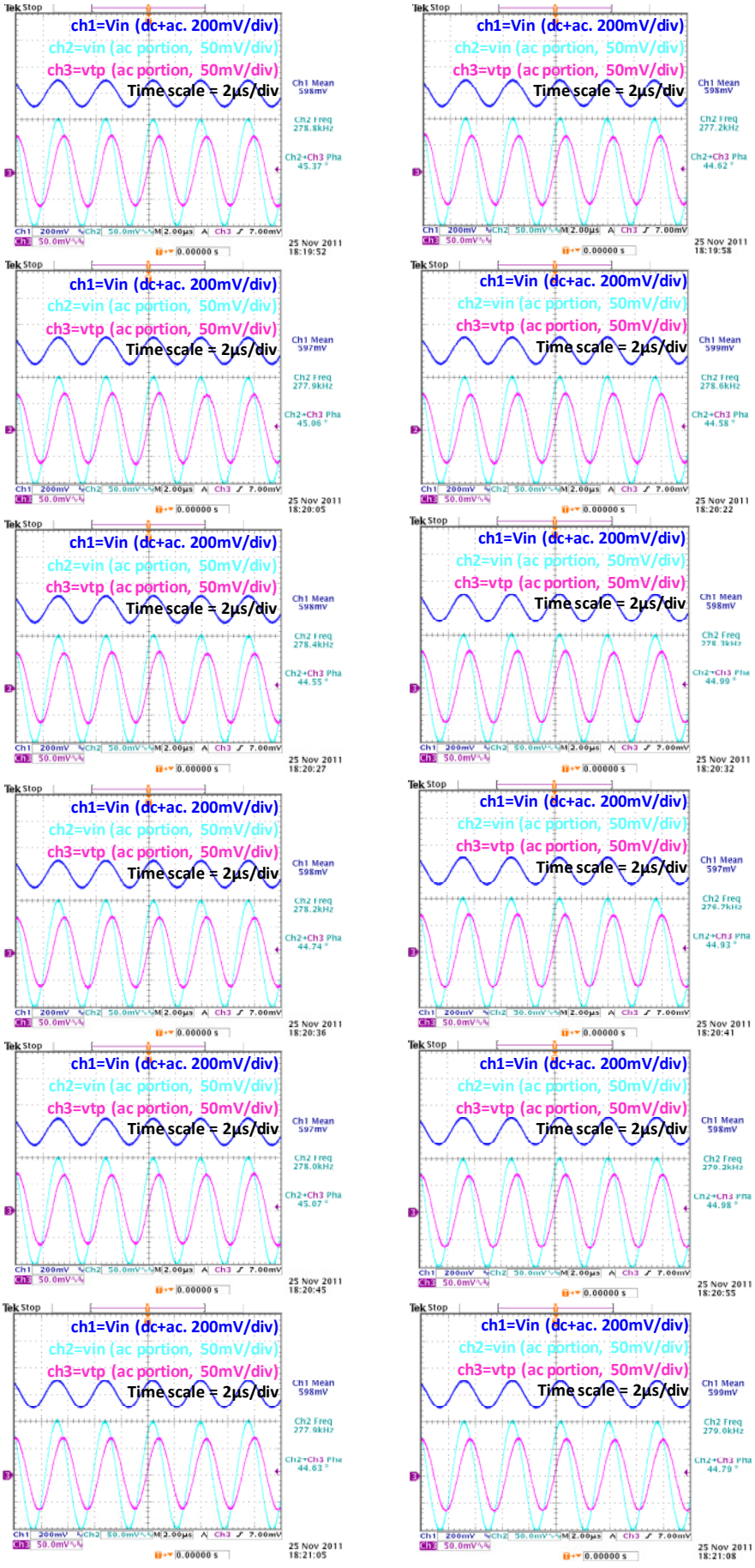








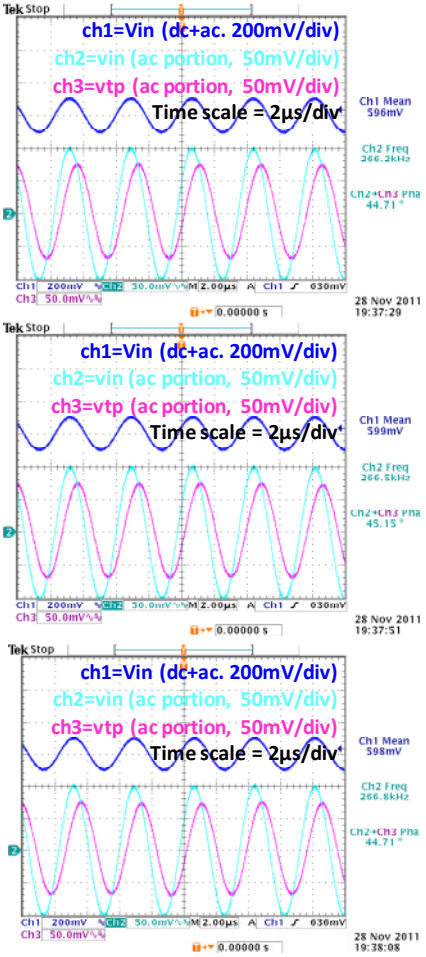


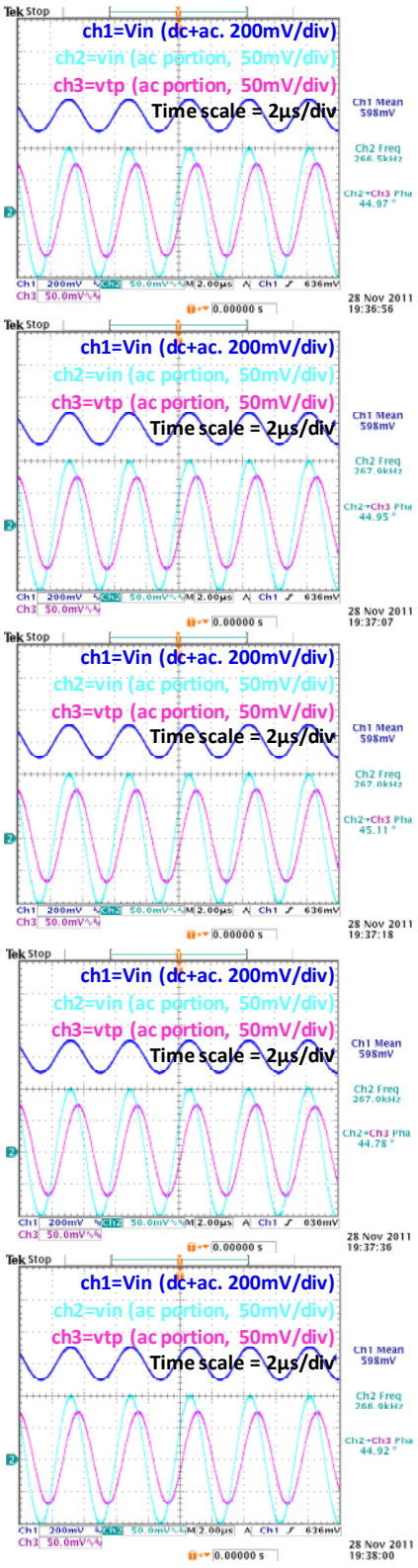

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 278.8kHz
Ch2+Ch3 Pha 45.37 °
25 Nov 2011 18:19:52
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 277.2kHz
Ch2+Ch3 Pha 44.62 °
25 Nov 2011 18:19:58
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 277.9kHz
Ch2+Ch3 Pha 45.06 °
25 Nov 2011 18:20:05
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 599mV
Ch2 Freq 278.6kHz
Ch2+Ch3 Pha 44.58 °
25 Nov 2011 18:20:22
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 278.4kHz
Ch2+Ch3 Pha 44.55 °
25 Nov 2011 18:20:27
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq
Ch2+Ch3 Pha 44.99 °
25 Nov 2011 18:20:32
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 278.2kHz
Ch2+Ch3 Pha 44.74 °
25 Nov 2011 18:20:36
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 276.7kHz
Ch2+Ch3 Pha 44.93 °
25 Nov 2011 18:20:41
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 278.0kHz
Ch2+Ch3 Pha 45.07 °
25 Nov 2011 18:20:45
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 278.2kHz
Ch2+Ch3 Pha 44.98 °
25 Nov 2011 18:20:55
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 277.9kHz
Ch2+Ch3 Pha 44.63 °
25 Nov 2011 18:21:05
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 599mV
Ch2 Freq 279.0kHz
Ch2+Ch3 Pha 44.79 °
25 Nov 2011 18:21:08

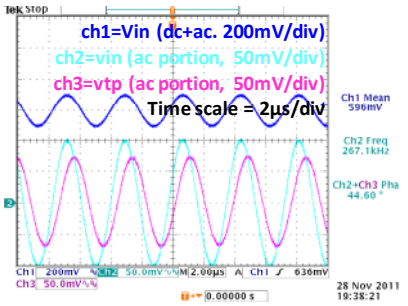
Measurements at QFG point with VBIAS=0.6V

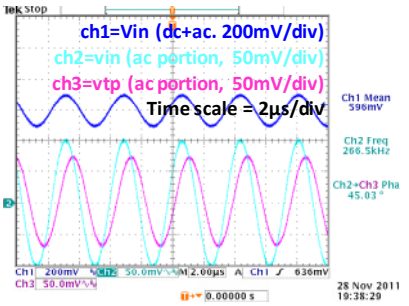
RIN= 4.697E+04

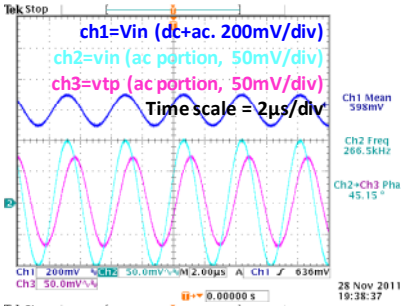
Sample No.	*phase*	*f*	*c*
1	44.97	2.665E+05	1.27E-11
2	44.95	2.679E+05	1.26E-11
3	45.11	2.670E+05	1.27E-11
4	44.71	2.662E+05	1.26E-11
5	44.78	2.670E+05	1.26E-11
6	45.15	2.665E+05	1.28E-11
7	44.92	2.669E+05	1.27E-11
8	44.71	2.668E+05	1.26E-11
9	44.60	2.671E+05	1.25E-11
10	45.03	2.665E+05	1.27E-11
11	45.15	2.665E+05	1.28E-11
12	45.00	2.680E+05	1.26E-11
13	45.26	2.675E+05	1.28E-11
14	45.09	2.673E+05	1.27E-11
15	45.02	2.666E+05	1.27E-11
16	44.68	2.661E+05	1.26E-11
17	45.04	2.684E+05	1.26E-11
18	45.22	2.671E+05	1.28E-11
19	44.55	2.678E+05	1.25E-11
20	44.70	2.665E+05	1.26E-11
Average	44.93	2.670E+05	**1.266E-11**
STD	0.21	6.357E+02	**9.494E-14**

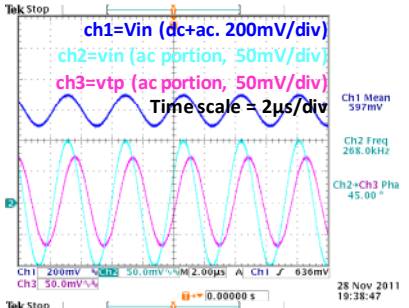


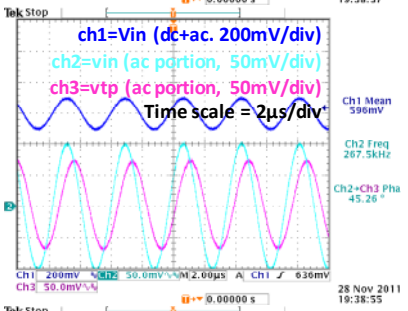


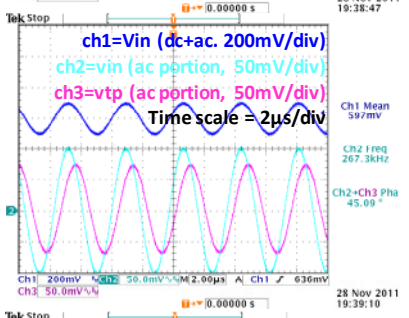

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 596mV
Ch2 Freq 267.1kHz
Ch2+Ch3 Pha 44.60 °
28 Nov 2011 19:38:21

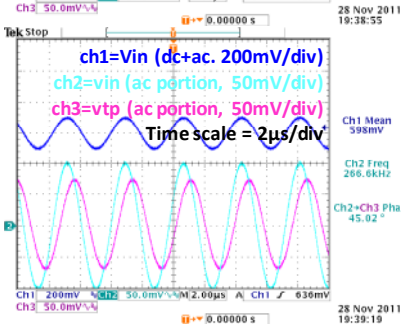

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 596mV
Ch2 Freq 266.5kHz
Ch2+Ch3 Pha 45.03 °
28 Nov 2011 19:38:29

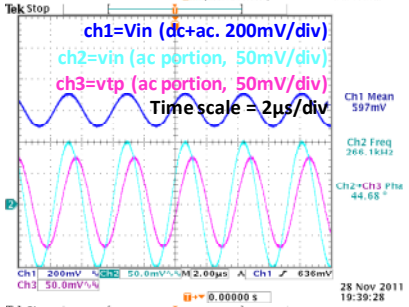

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 266.5kHz
Ch2+Ch3 Pha 45.15 °
28 Nov 2011 19:38:37

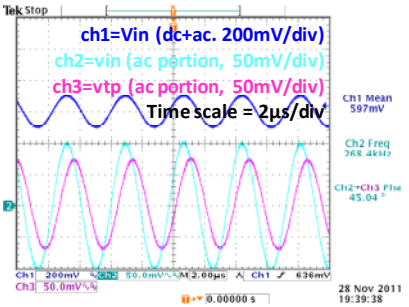

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 268.0kHz
Ch2+Ch3 Pha 45.00 °
28 Nov 2011 19:38:47

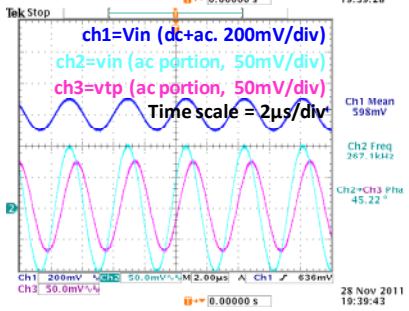

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 596mV
Ch2 Freq 267.5kHz
Ch2+Ch3 Pha 45.26 °
28 Nov 2011 19:38:55

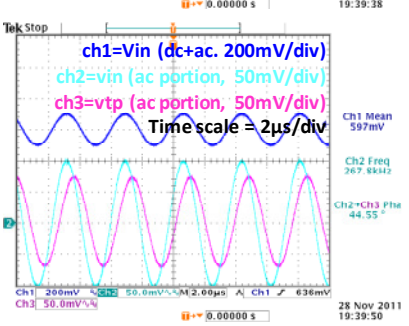

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 267.3kHz
Ch2+Ch3 Pha 45.09 °
28 Nov 2011 19:39:10

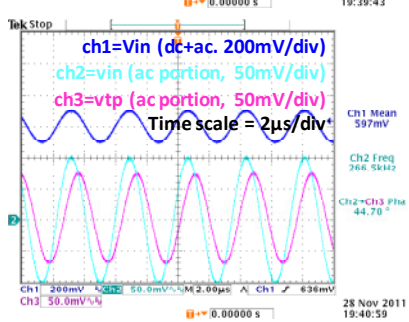

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 266.6kHz
Ch2+Ch3 Pha 45.02 °
28 Nov 2011 19:39:19


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 268.1kHz
Ch2+Ch3 Pha 44.68 °
28 Nov 2011 19:39:28


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 268.4kHz
Ch2+Ch3 Pha 45.04 °
28 Nov 2011 19:39:38


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 598mV
Ch2 Freq 267.1kHz
Ch2+Ch3 Pha 45.22 °
28 Nov 2011 19:39:43

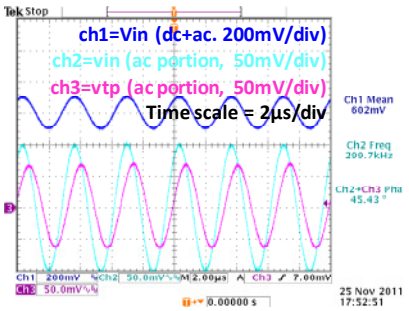

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 267.8kHz
Ch2+Ch3 Pha 44.55 °
28 Nov 2011 19:39:50

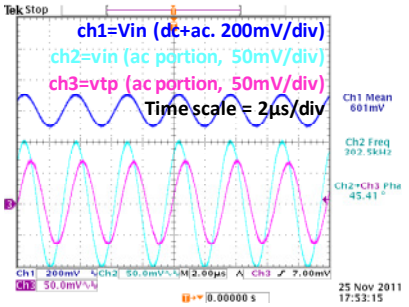

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 597mV
Ch2 Freq 266.5kHz
Ch2+Ch3 Pha 44.70 °
28 Nov 2011 19:40:59

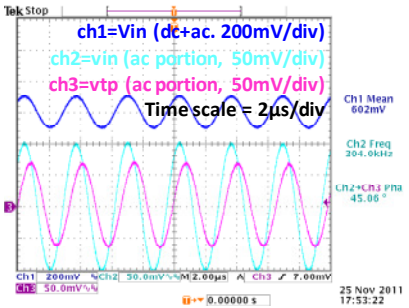
Measurements at PADONLY point with VBIAS=0.6V

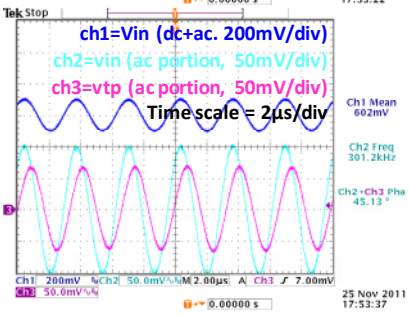
RIN= 4.697E+04

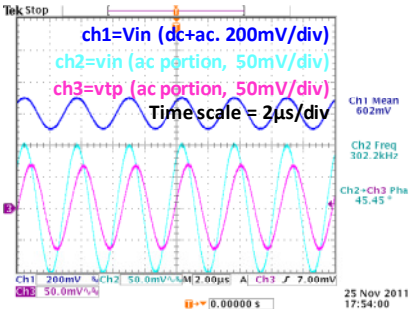
Sample No.	*phase*	*f*	*c*
1	45.43	2.997E+05	1.15E-11
2	45.41	3.025E+05	1.14E-11
3	45.06	3.040E+05	1.12E-11
4	44.86	3.032E+05	1.11E-11
5	45.13	3.012E+05	1.13E-11
6	45.56	3.017E+05	1.15E-11
7	45.45	3.022E+05	1.14E-11
8	44.88	3.025E+05	1.12E-11
9	44.92	3.013E+05	1.12E-11
10	44.98	3.030E+05	1.12E-11
11	44.85	3.020E+05	1.12E-11
12	44.94	3.034E+05	1.11E-11
13	44.77	3.033E+05	1.11E-11
14	45.32	3.027E+05	1.13E-11
15	44.75	3.032E+05	1.11E-11
16	44.69	3.013E+05	1.11E-11
17	44.50	3.000E+05	1.11E-11
18	44.68	3.020E+05	1.11E-11
19	44.74	3.024E+05	1.11E-11
20	44.98	3.018E+05	1.12E-11
Average	45.00	3.022E+05	**1.121E-11**
STD	0.30	1.105E+03	**1.265E-13**

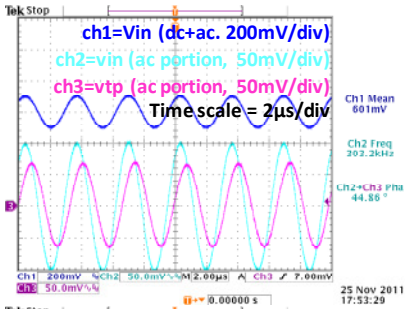


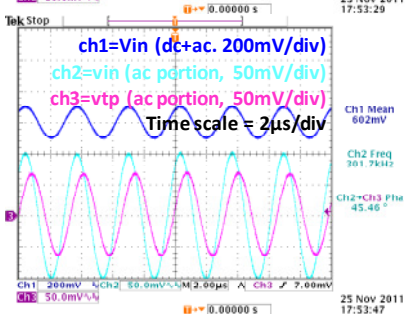


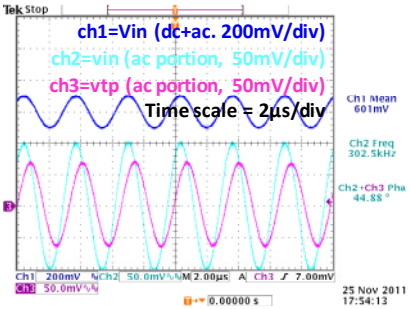


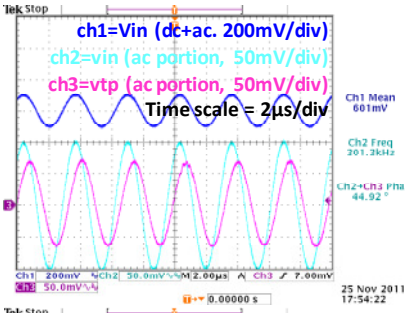


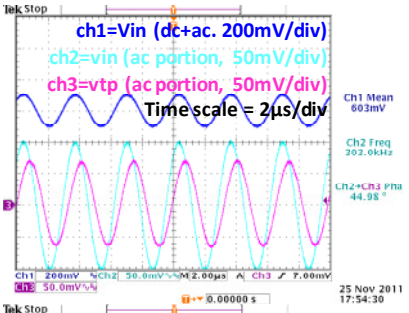


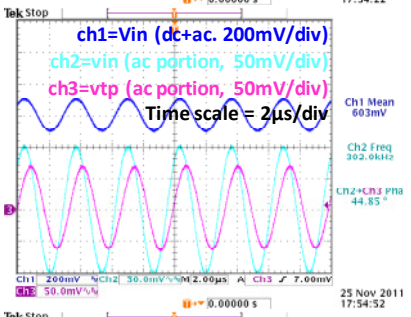


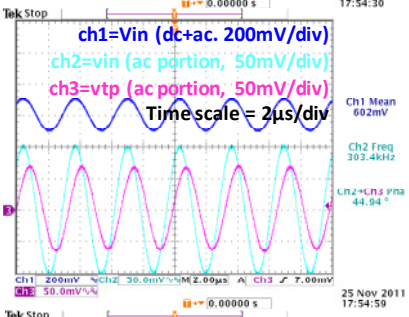


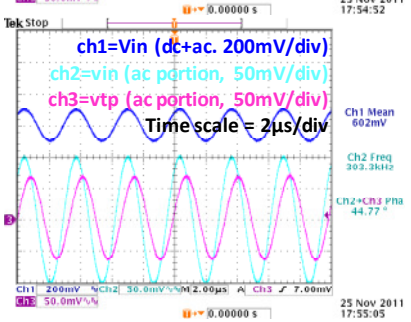


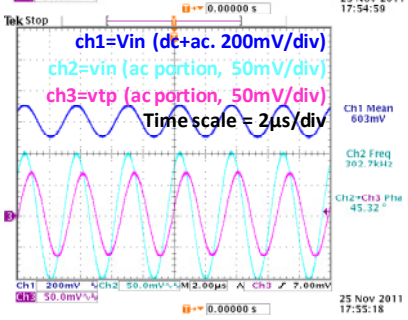

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
601mV
Ch2 Freq
201.2kHz
Ch2+Ch3 Pha
44.92 °
25 Nov 2011
17:54:22

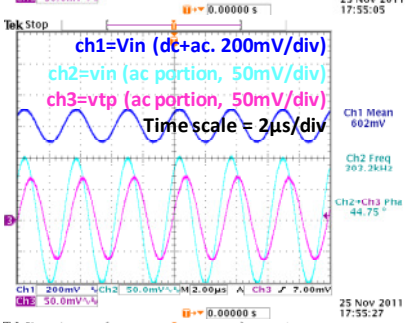

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
603mV
Ch2 Freq
202.0kHz
Ch2+Ch3 Pha
44.98 °
25 Nov 2011
17:54:30

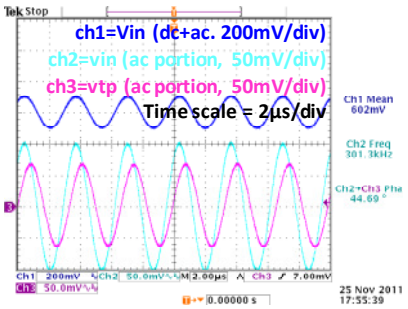

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
603mV
Ch2 Freq
202.0kHz
Ch2+Ch3 Pha
44.85 °
25 Nov 2011
17:54:52

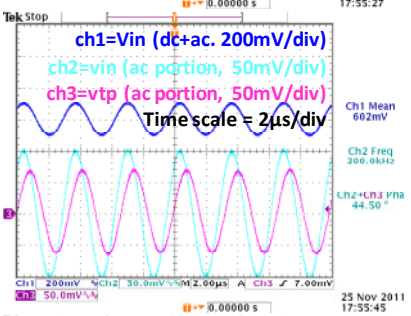

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
303.4kHz
Ch2+Ch3 Pha
44.94 °
25 Nov 2011
17:54:59

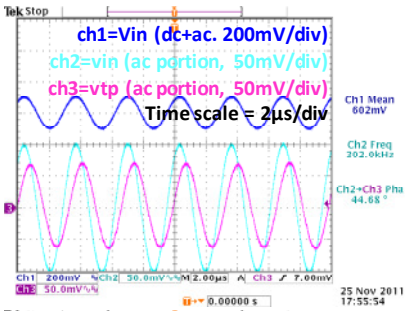

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
303.3kHz
Ch2+Ch3 Pha
44.77 °
25 Nov 2011
17:55:05

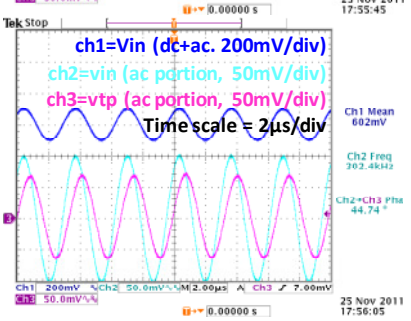

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
603mV
Ch2 Freq
302.7kHz
Ch2+Ch3 Pha
45.32 °
25 Nov 2011
17:55:18

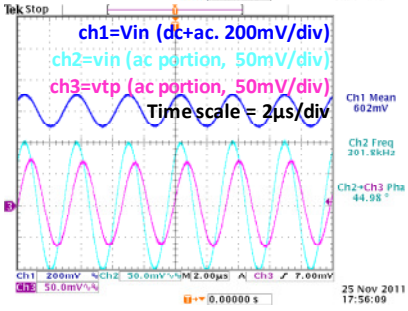

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
303.2kHz
Ch2+Ch3 Pha
44.75 °
25 Nov 2011
17:55:27


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
301.3kHz
Ch2+Ch3 Pha
44.69 °
25 Nov 2011
17:55:39


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
300.0kHz
Ch2+Ch3 Pha
44.50 °
25 Nov 2011
17:55:45


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
302.0kHz
Ch2+Ch3 Pha
44.68 °
25 Nov 2011
17:55:54

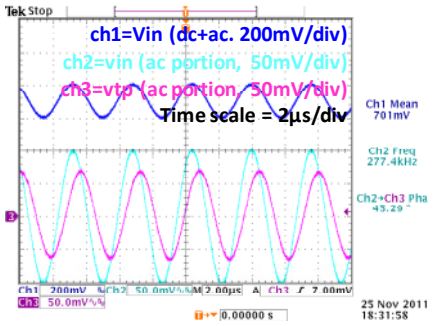

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
302.4kHz
Ch2+Ch3 Pha
44.74 °
25 Nov 2011
17:56:05

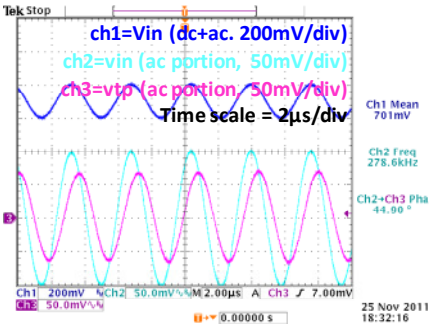

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
602mV
Ch2 Freq
301.8kHz
Ch2+Ch3 Pha
44.98 °
25 Nov 2011
17:56:09

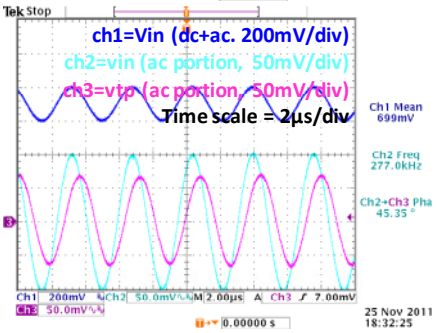
Measurements at NoQFG point with VBIAS=0.7V

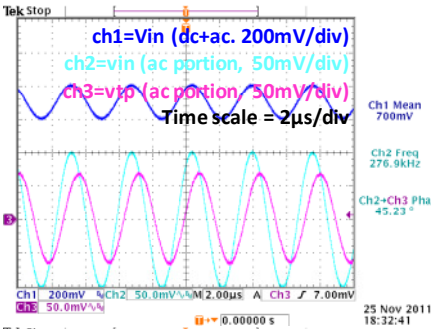
RIN= 4.697E+04

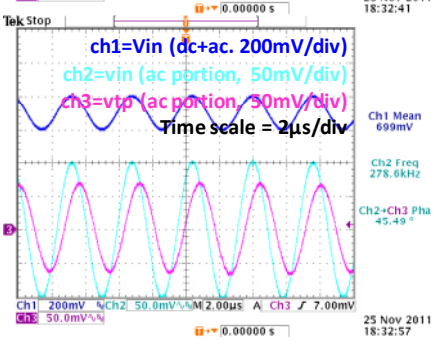
Sample No.	*phase*	*f*	*c*
1	45.29	2.774E+05	1.23E-11
2	44.90	2.786E+05	1.21E-11
3	45.35	2.770E+05	1.24E-11
4	44.63	2.782E+05	1.20E-11
5	45.23	2.769E+05	1.23E-11
6	44.86	2.781E+05	1.21E-11
7	45.49	2.786E+05	1.24E-11
8	44.85	2.784E+05	1.21E-11
9	44.88	2.769E+05	1.22E-11
10	44.97	2.764E+05	1.22E-11
11	45.16	2.783E+05	1.22E-11
12	44.74	2.793E+05	1.20E-11
13	45.08	2.775E+05	1.22E-11
14	44.64	2.767E+05	1.21E-11
15	44.52	2.760E+05	1.21E-11
16	44.59	2.765E+05	1.21E-11
17	45.43	2.770E+05	1.24E-11
18	45.20	2.769E+05	1.23E-11
19	45.20	2.778E+05	1.23E-11
20	45.44	2.771E+05	1.24E-11
Average	45.02	2.775E+05	**1.222E-11**
STD	0.31	8.853E+02	**1.337E-13**

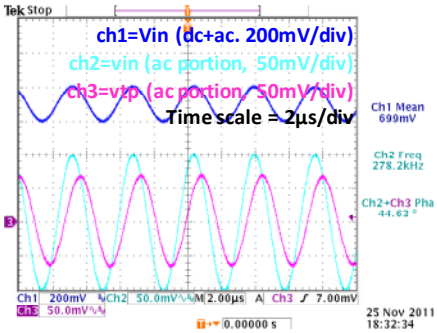


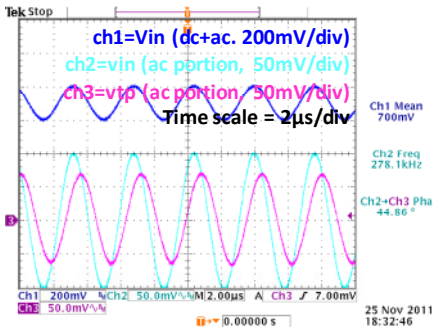


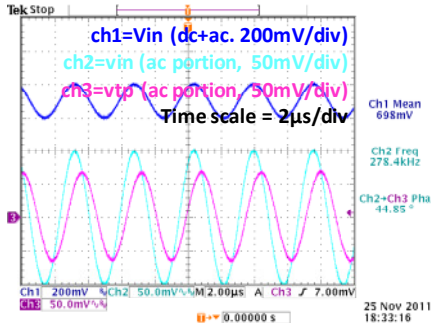


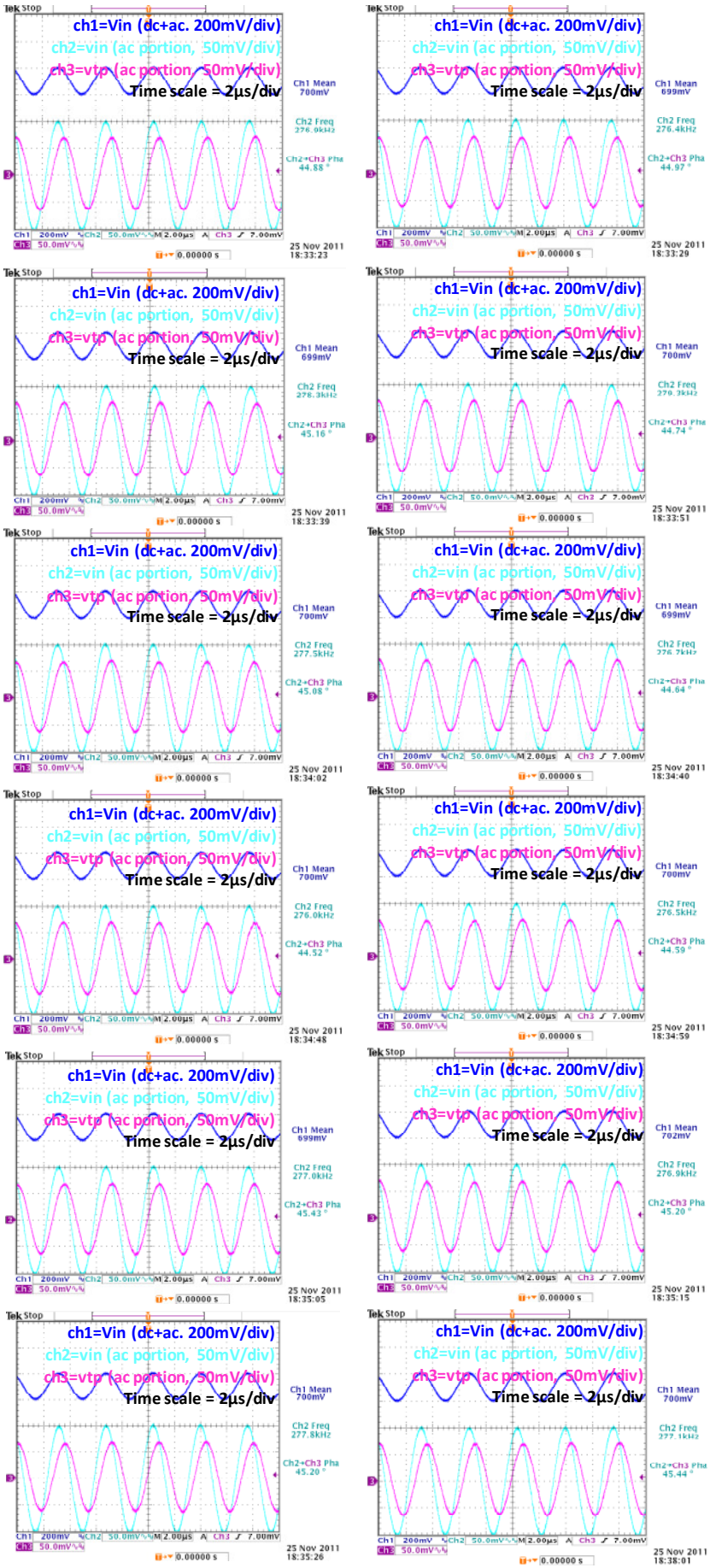








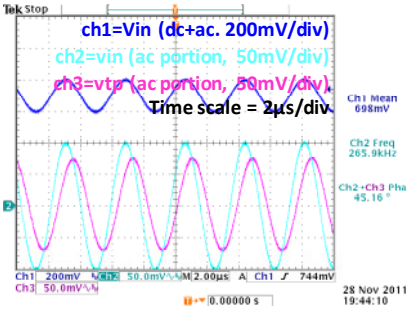


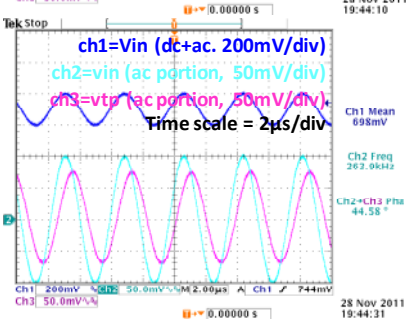

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 276.0kHz
Ch2+Ch3 Pha 44.88°
25 Nov 2011 18:33:23
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 276.4kHz
Ch2+Ch3 Pha 44.97°
25 Nov 2011 18:33:29
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 276.3kHz
Ch2+Ch3 Pha 45.16°
25 Nov 2011 18:33:39
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 276.3kHz
Ch2+Ch3 Pha 44.74°
25 Nov 2011 18:33:51
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 277.5kHz
Ch2+Ch3 Pha 45.08°
25 Nov 2011 18:34:02
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 276.7kHz
Ch2+Ch3 Pha 44.64°
25 Nov 2011 18:34:40
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 276.0kHz
Ch2+Ch3 Pha 44.52°
25 Nov 2011 18:34:48
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 276.5kHz
Ch2+Ch3 Pha 44.59°
25 Nov 2011 18:34:59
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 277.0kHz
Ch2+Ch3 Pha 45.43°
25 Nov 2011 18:35:05
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 702mV
Ch2 Freq 276.9kHz
Ch2+Ch3 Pha 45.20°
25 Nov 2011 18:35:15
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 277.8kHz
Ch2+Ch3 Pha 45.20°
25 Nov 2011 18:35:26
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 277.1kHz
Ch2+Ch3 Pha 45.44°
25 Nov 2011 18:38:01

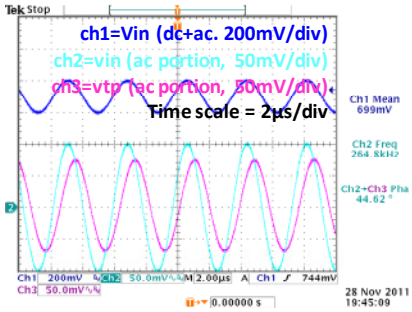
Measurements at QFG point with VBIAS=0.7V

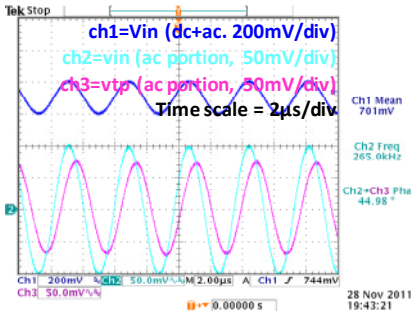
RIN= 4.697E+04

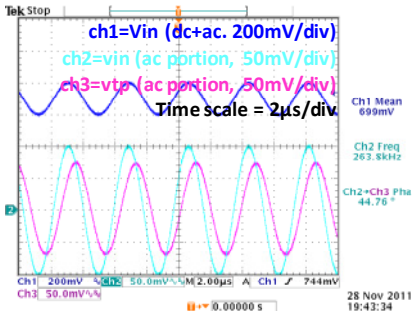
Sample No.	*phase*	*f*	*c*
1	44.98	2.650E+05	1.28E-11
2	44.76	2.638E+05	1.27E-11
3	44.71	2.651E+05	1.27E-11
4	45.16	2.659E+05	1.28E-11
5	44.70	2.634E+05	1.27E-11
6	44.58	2.639E+05	1.27E-11
7	44.57	2.662E+05	1.25E-11
8	44.62	2.648E+05	1.26E-11
9	45.10	2.660E+05	1.28E-11
10	44.96	2.651E+05	1.28E-11
11	44.68	2.651E+05	1.26E-11
12	44.89	2.655E+05	1.27E-11
13	44.98	2.652E+05	1.28E-11
14	45.26	2.641E+05	1.29E-11
15	45.03	2.647E+05	1.28E-11
16	45.31	2.655E+05	1.29E-11
17	45.05	2.648E+05	1.28E-11
18	44.58	2.645E+05	1.26E-11
19	45.26	2.648E+05	1.29E-11
20	44.62	2.660E+05	1.26E-11
Average	44.89	2.650E+05	**1.274E-11**
STD	0.25	7.706E+02	**1.128E-13**

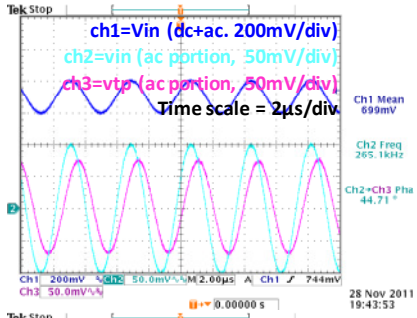


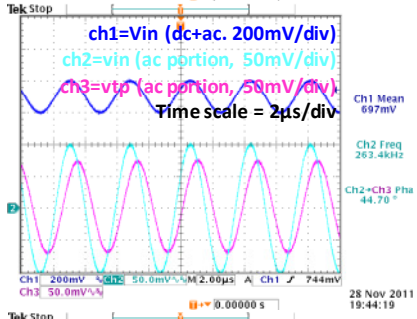


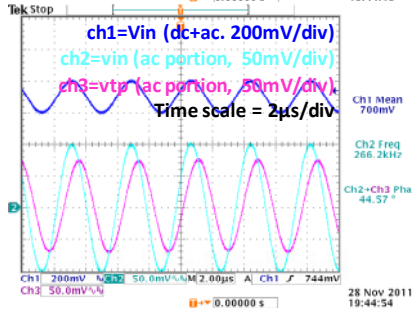


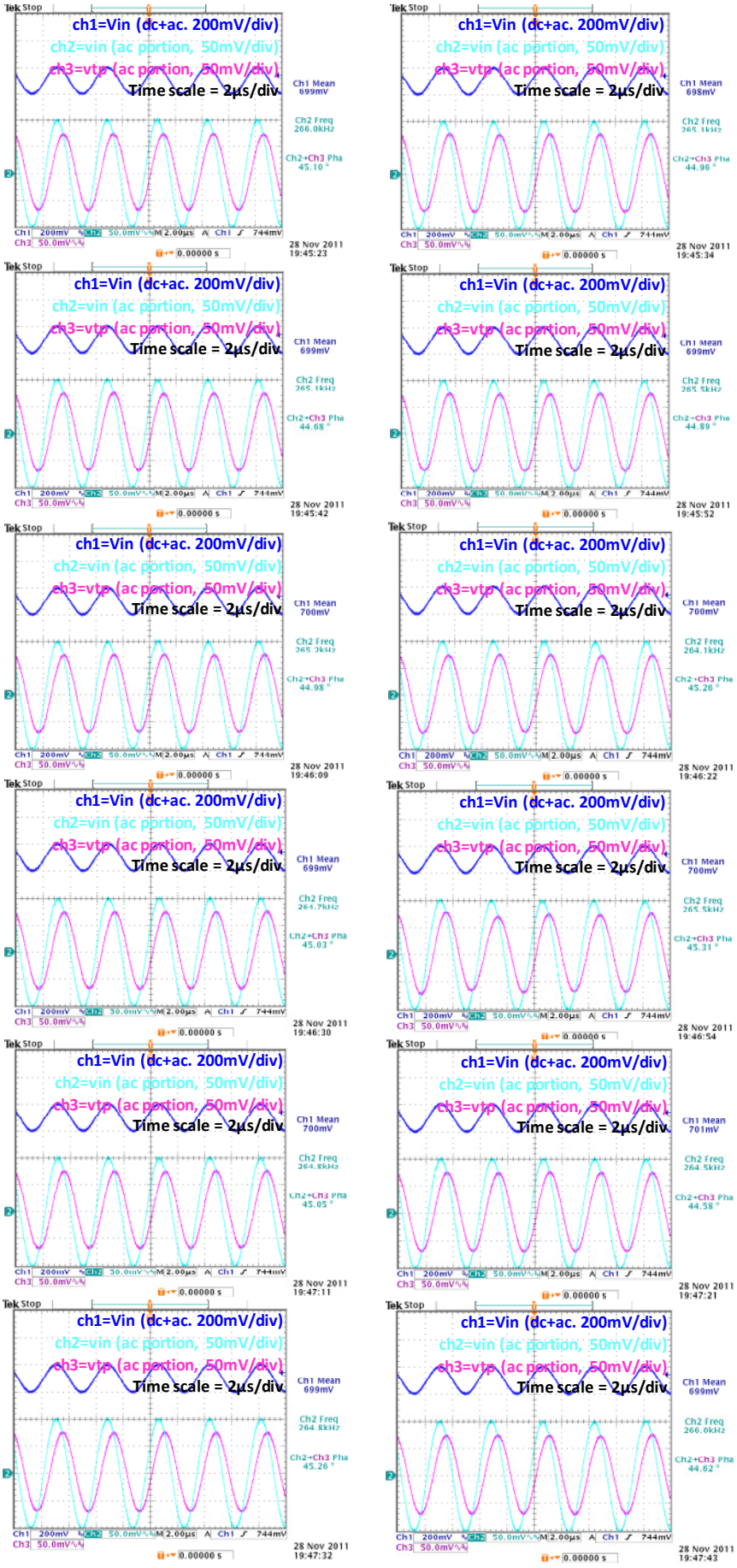








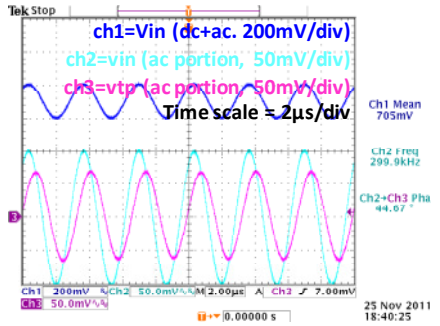


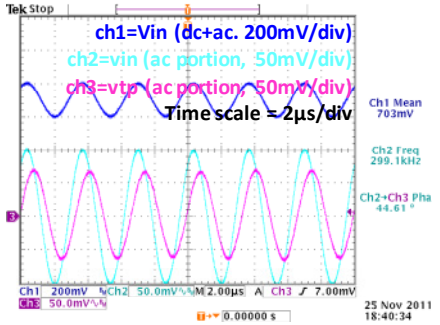

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 266.0kHz
Ch2+Ch3 Pha 45.10 °
28 Nov 2011 19:45:23
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 698mV
Ch2 Freq 265.1kHz
Ch2+Ch3 Pha 44.90 °
28 Nov 2011 19:45:34
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 265.1kHz
Ch2+Ch3 Pha 44.68 °
28 Nov 2011 19:45:42
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 265.5kHz
Ch2+Ch3 Pha 44.89 °
28 Nov 2011 19:45:52
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 265.2kHz
Ch2+Ch3 Pha 44.98 °
28 Nov 2011 19:46:09
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 264.1kHz
Ch2+Ch3 Pha 45.26 °
28 Nov 2011 19:46:22
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 264.7kHz
Ch2+Ch3 Pha 45.03 °
28 Nov 2011 19:46:30
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 265.5kHz
Ch2+Ch3 Pha 45.31 °
28 Nov 2011 19:46:54
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 700mV
Ch2 Freq 264.8kHz
Ch2+Ch3 Pha 45.05 °
28 Nov 2011 19:47:11
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 701mV
Ch2 Freq 264.5kHz
Ch2+Ch3 Pha 44.58 °
28 Nov 2011 19:47:21
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 264.8kHz
Ch2+Ch3 Pha 45.26 °
28 Nov 2011 19:47:32
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 699mV
Ch2 Freq 266.0kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 19:47:43

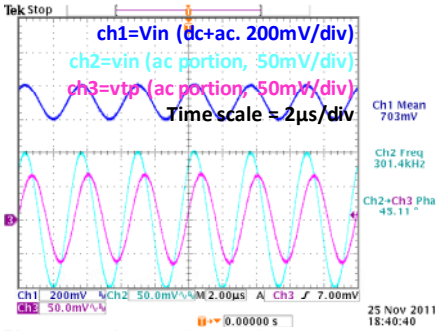
Measurements at PADONLY point with VBIAS=0.7V

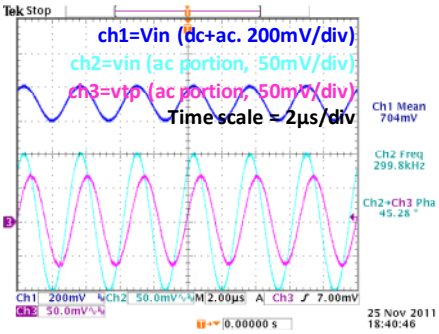
RIN= 4.697E+04

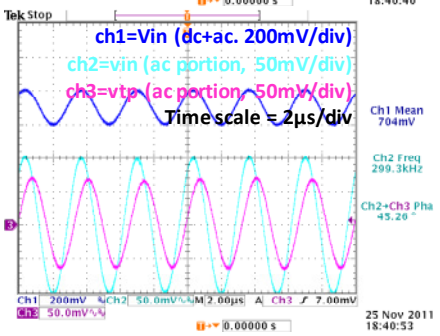
Sample No.	*phase*	*f*	*c*
1	44.67	2.999E+05	1.12E-11
2	44.61	2.991E+05	1.12E-11
3	45.11	3.014E+05	1.13E-11
4	45.28	2.998E+05	1.14E-11
5	45.26	2.993E+05	1.14E-11
6	44.68	3.010E+05	1.11E-11
7	45.43	3.003E+05	1.15E-11
8	45.49	3.005E+05	1.15E-11
9	45.39	2.999E+05	1.15E-11
10	45.17	2.998E+05	1.14E-11
11	44.50	2.988E+05	1.11E-11
12	45.05	2.998E+05	1.13E-11
13	45.49	3.009E+05	1.15E-11
14	44.94	3.001E+05	1.13E-11
15	44.55	3.006E+05	1.11E-11
16	44.91	3.001E+05	1.13E-11
17	45.13	2.999E+05	1.13E-11
18	45.38	2.999E+05	1.14E-11
19	45.02	2.997E+05	1.13E-11
20	45.49	2.998E+05	1.15E-11
Average	45.08	3.000E+05	**1.132E-11**
STD	0.33	6.284E+02	**1.288E-13**

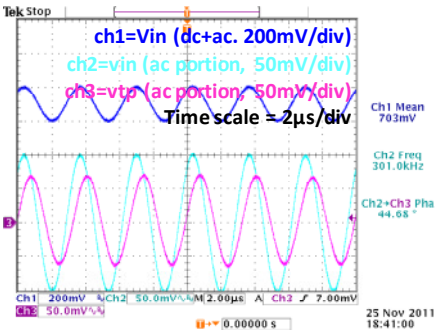


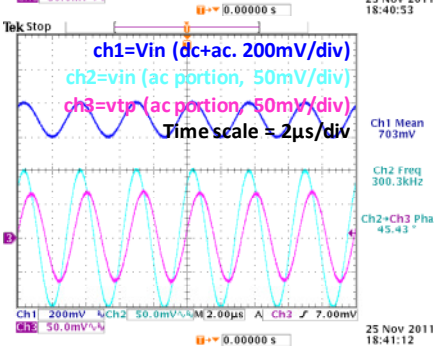


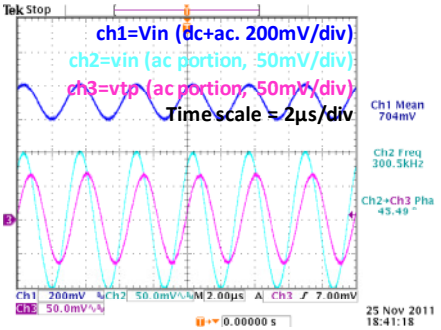


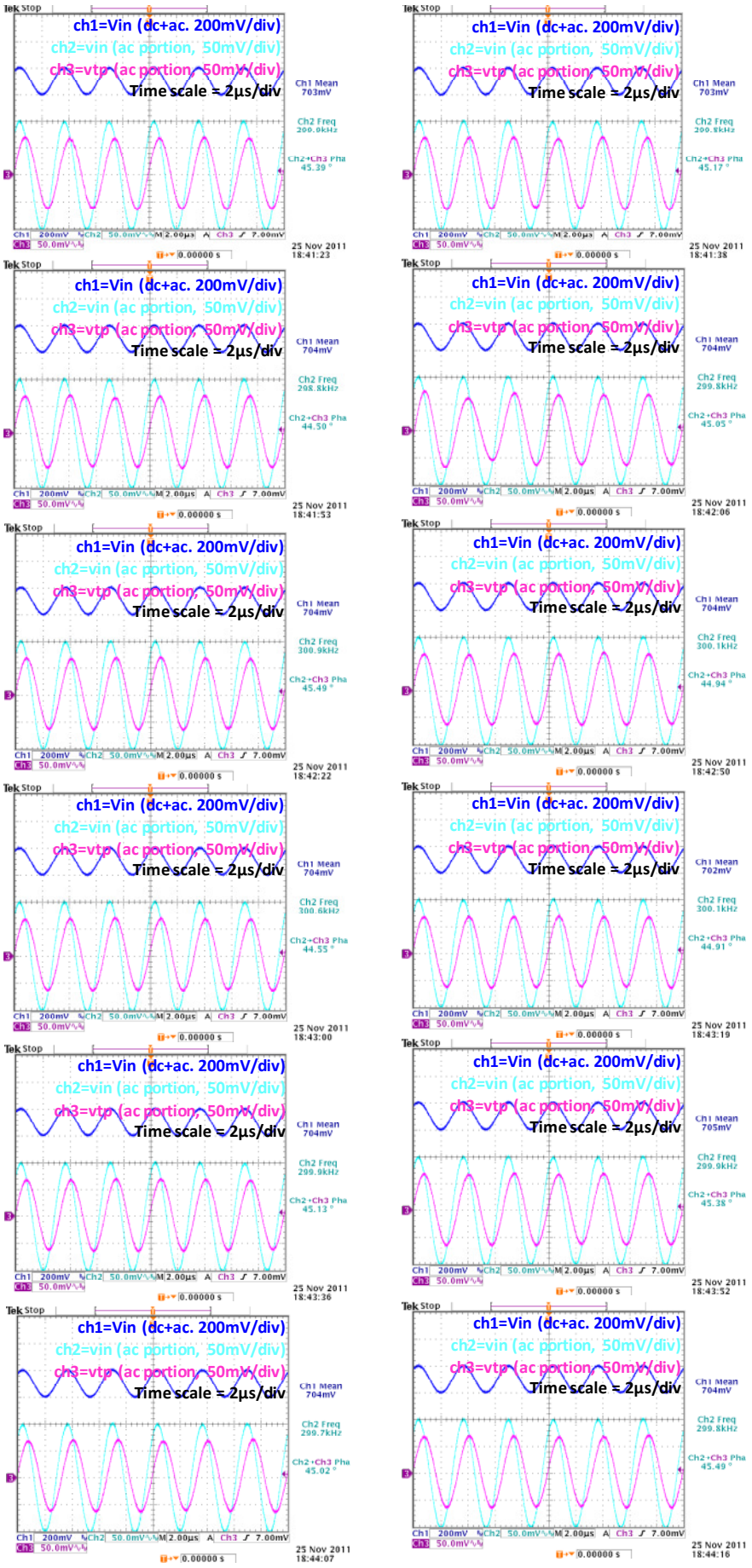








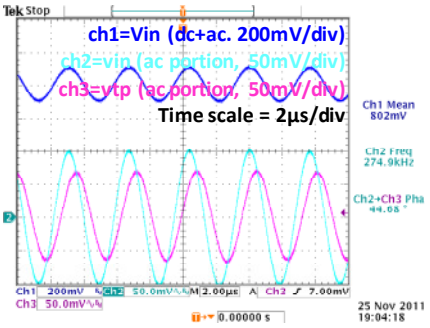


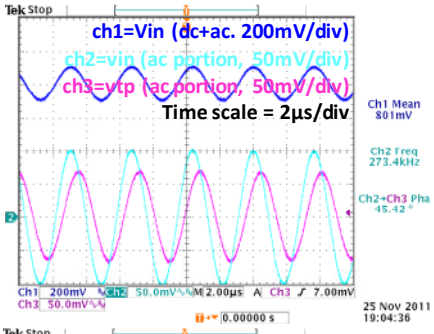

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 703mV
Ch2 Freq 200.0kHz
Ch2+Ch3 Pha 45.39 °
25 Nov 2011 18:41:23
Ch1 Mean 703mV
Ch2 Freq 209.8kHz
Ch2+Ch3 Pha 45.17 °
25 Nov 2011 18:41:38
Ch1 Mean 704mV
Ch2 Freq 298.8kHz
Ch2+Ch3 Pha 44.50 °
25 Nov 2011 18:41:53
Ch1 Mean 704mV
Ch2 Freq 299.8kHz
Ch2+Ch3 Pha 45.05 °
25 Nov 2011 18:42:06
Ch1 Mean 704mV
Ch2 Freq 300.9kHz
Ch2+Ch3 Pha 45.49 °
25 Nov 2011 18:42:22
Ch1 Mean 704mV
Ch2 Freq 300.1kHz
Ch2+Ch3 Pha 44.94 °
25 Nov 2011 18:42:50
Ch1 Mean 704mV
Ch2 Freq 300.6kHz
Ch2+Ch3 Pha 44.55 °
25 Nov 2011 18:43:00
Ch1 Mean 702mV
Ch2 Freq 300.1kHz
Ch2+Ch3 Pha 44.91 °
25 Nov 2011 18:43:19
Ch1 Mean 704mV
Ch2 Freq 299.9kHz
Ch2+Ch3 Pha 45.13 °
25 Nov 2011 18:43:36
Ch1 Mean 705mV
Ch2 Freq 299.9kHz
Ch2+Ch3 Pha 45.38 °
25 Nov 2011 18:43:52
Ch1 Mean 704mV
Ch2 Freq 299.7kHz
Ch2+Ch3 Pha 45.02 °
25 Nov 2011 18:44:07
Ch1 Mean 704mV
Ch2 Freq 299.8kHz
Ch2+Ch3 Pha 45.49 °
25 Nov 2011 18:44:16

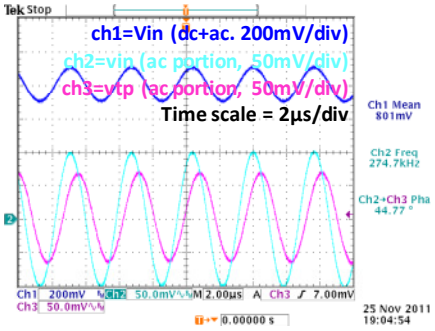
Measurements at NoQFG point with VBIAS=0.8V

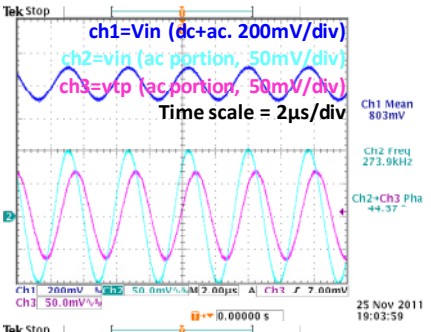
RIN= 4.697E+04

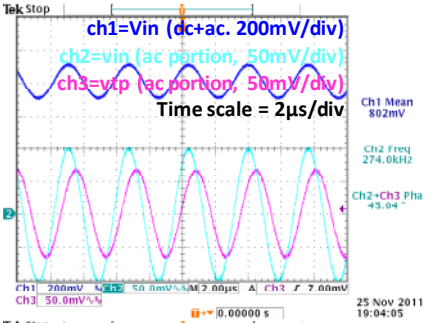
Sample No.	*phase*	*f*	*c*
1	44.57	2.739E+05	1.22E-11
2	45.04	2.740E+05	1.24E-11
3	44.70	2.732E+05	1.23E-11
4	44.68	2.749E+05	1.22E-11
5	44.78	2.725E+05	1.23E-11
6	45.42	2.734E+05	1.26E-11
7	44.64	2.737E+05	1.22E-11
8	44.77	2.747E+05	1.22E-11
9	44.98	2.735E+05	1.24E-11
10	45.08	2.735E+05	1.24E-11
11	44.92	2.742E+05	1.23E-11
12	44.51	2.729E+05	1.22E-11
13	45.12	2.738E+05	1.24E-11
14	44.55	2.747E+05	1.21E-11
15	44.86	2.726E+05	1.24E-11
16	45.46	2.739E+05	1.26E-11
17	44.77	2.732E+05	1.23E-11
18	44.94	2.750E+05	1.23E-11
19	44.57	2.739E+05	1.22E-11
20	44.90	2.732E+05	1.24E-11
Average	44.86	2.737E+05	**1.232E-11**
STD	0.27	7.177E+02	**1.213E-13**

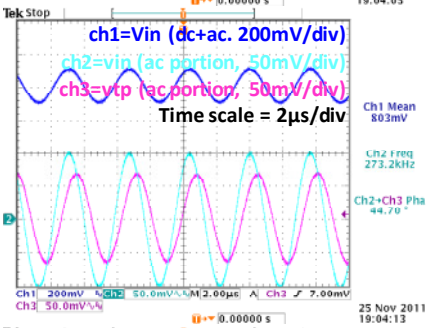


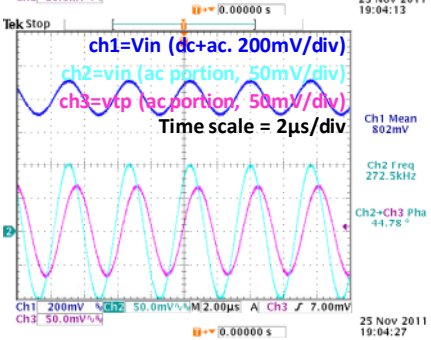


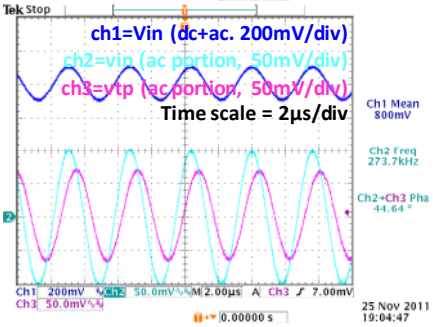


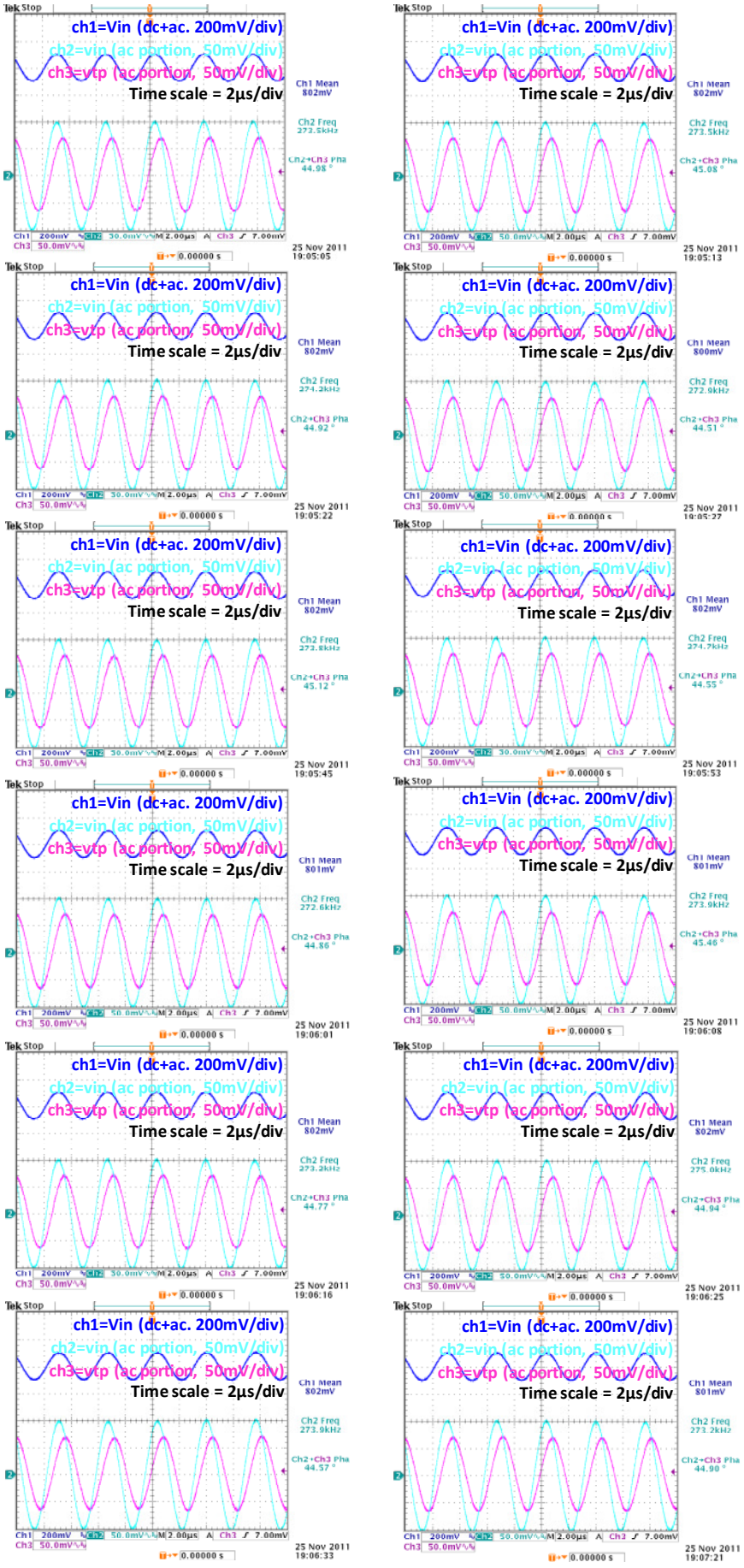








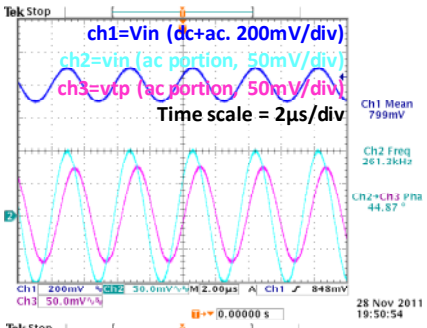


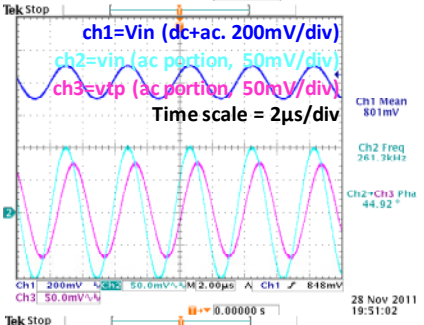

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 802mV
Ch2 Freq 272.5kHz
Ch2+Ch3 Pha 44.98 °
25 Nov 2011 19:05:05
Ch1 Mean 802mV
Ch2 Freq 273.5kHz
Ch2+Ch3 Pha 45.08 °
25 Nov 2011 19:05:13
Ch1 Mean 802mV
Ch2 Freq 274.2kHz
Ch2+Ch3 Pha 44.92 °
25 Nov 2011 19:05:22
Ch1 Mean 800mV
Ch2 Freq 272.9kHz
Ch2+Ch3 Pha 44.51 °
25 Nov 2011 19:05:27
Ch1 Mean 802mV
Ch2 Freq 273.8kHz
Ch2+Ch3 Pha 45.12 °
25 Nov 2011 19:05:45
Ch1 Mean 802mV
Ch2 Freq 274.7kHz
Ch2+Ch3 Pha 44.55 °
25 Nov 2011 19:05:53
Ch1 Mean 801mV
Ch2 Freq 272.6kHz
Ch2+Ch3 Pha 44.86 °
25 Nov 2011 19:06:01
Ch1 Mean 801mV
Ch2 Freq 273.9kHz
Ch2+Ch3 Pha 45.46 °
25 Nov 2011 19:06:08
Ch1 Mean 802mV
Ch2 Freq 273.2kHz
Ch2+Ch3 Pha 44.77 °
25 Nov 2011 19:06:16
Ch1 Mean 802mV
Ch2 Freq 275.0kHz
Ch2+Ch3 Pha 44.94 °
25 Nov 2011 19:06:25
Ch1 Mean 802mV
Ch2 Freq 273.9kHz
Ch2+Ch3 Pha 44.57 °
25 Nov 2011 19:06:33
Ch1 Mean 801mV
Ch2 Freq 273.2kHz
Ch2+Ch3 Pha 44.90 °
25 Nov 2011 19:07:21

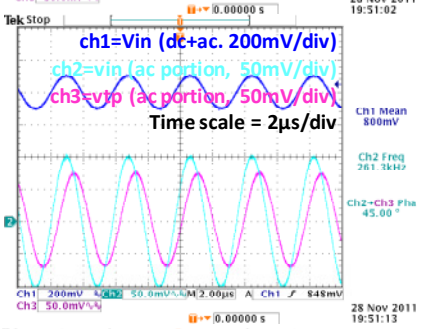
Measurements at QFG point with VBIAS=0.8V

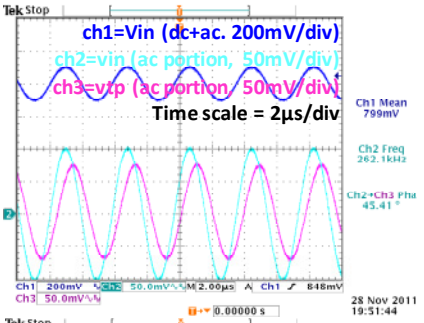
RIN= 4.697E+04

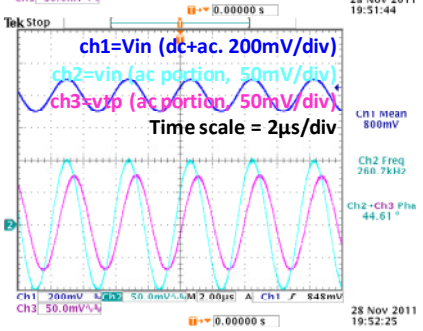
Sample No.	*phase*	*f*	*c*
1	44.87	2.613E+05	1.29E-11
2	44.92	2.613E+05	1.29E-11
3	45.00	2.613E+05	1.30E-11
4	44.60	2.614E+05	1.28E-11
5	45.41	2.621E+05	1.31E-11
6	44.97	2.605E+05	1.30E-11
7	44.61	2.607E+05	1.28E-11
8	44.59	2.601E+05	1.28E-11
9	44.79	2.617E+05	1.29E-11
10	44.77	2.597E+05	1.29E-11
11	44.86	2.602E+05	1.30E-11
12	44.72	2.604E+05	1.29E-11
13	44.62	2.611E+05	1.28E-11
14	45.18	2.602E+05	1.31E-11
15	44.56	2.609E+05	1.28E-11
16	44.98	2.609E+05	1.30E-11
17	45.10	2.610E+05	1.30E-11
18	45.21	2.600E+05	1.31E-11
19	44.62	2.610E+05	1.28E-11
20	44.62	2.622E+05	1.28E-11
Average	44.85	2.609E+05	**1.292E-11**
STD	0.24	6.836E+02	**1.147E-13**

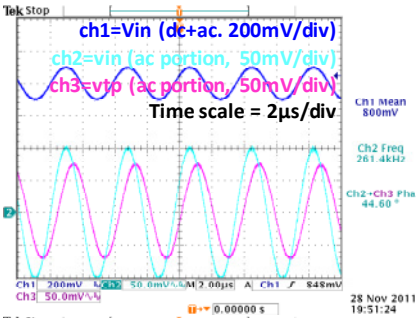


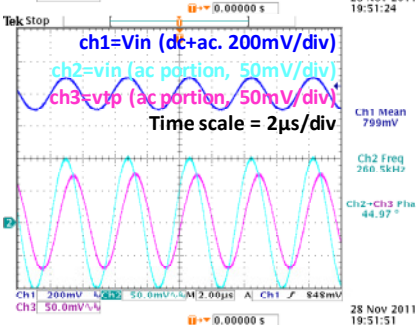


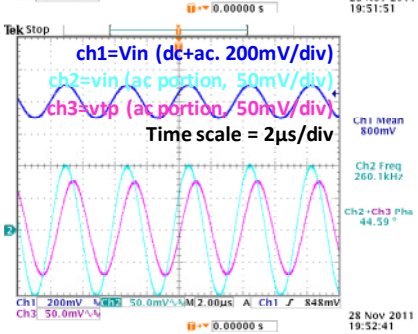


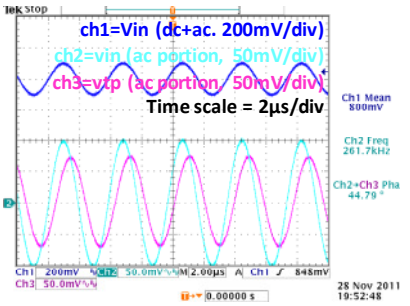


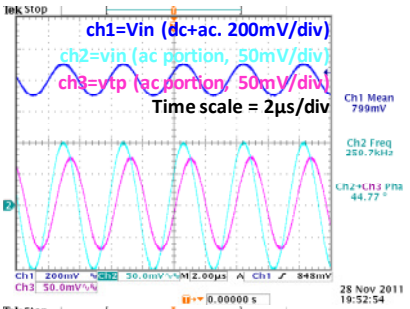


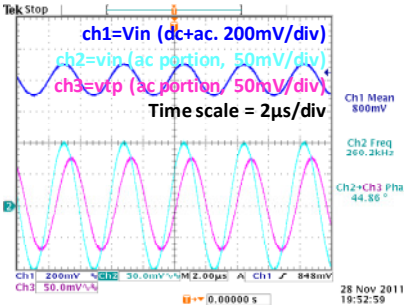


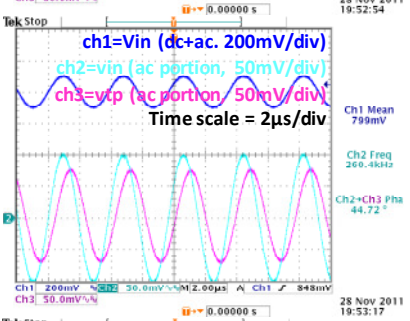


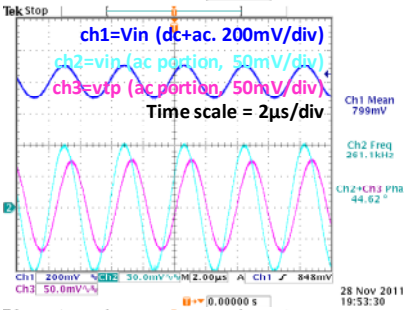


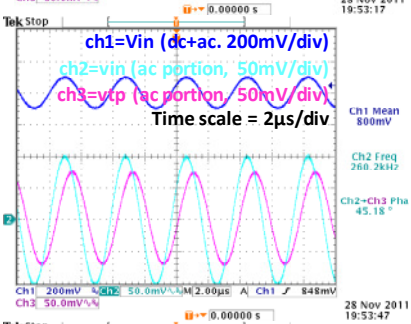

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 800mV
Ch2 Freq 261.7kHz
Ch2+Ch3 Pha 44.79 °
28 Nov 2011 19:52:48

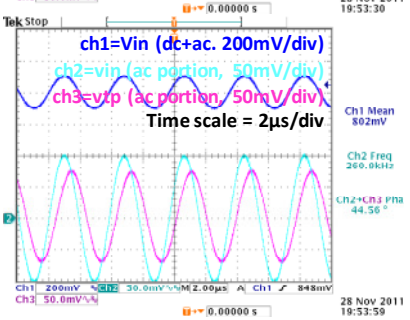

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 799mV
Ch2 Freq 259.7kHz
Ch2+Ch3 Pha 44.77 °
28 Nov 2011 19:52:54

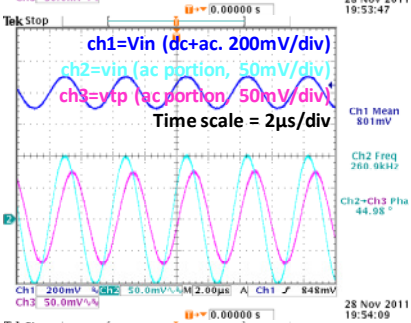

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 800mV
Ch2 Freq 260.2kHz
Ch2+Ch3 Pha 44.86 °
28 Nov 2011 19:52:59

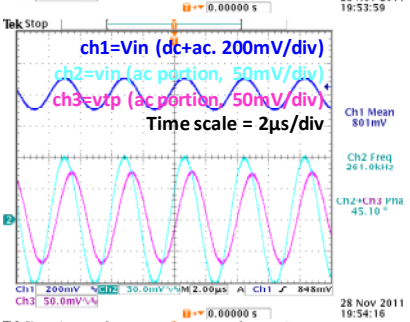

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 799mV
Ch2 Freq 260.4kHz
Ch2+Ch3 Pha 44.72 °
28 Nov 2011 19:53:17

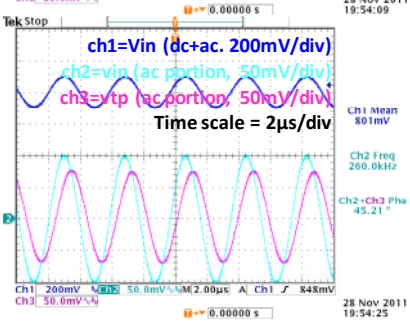

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 799mV
Ch2 Freq 261.1kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 19:53:30

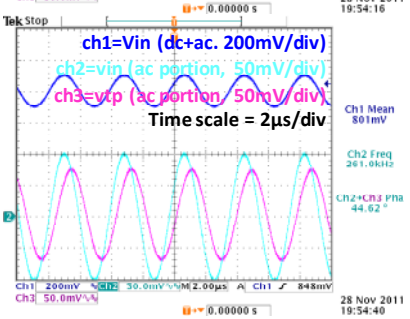

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 800mV
Ch2 Freq 260.2kHz
Ch2+Ch3 Pha 45.18 °
28 Nov 2011 19:53:47

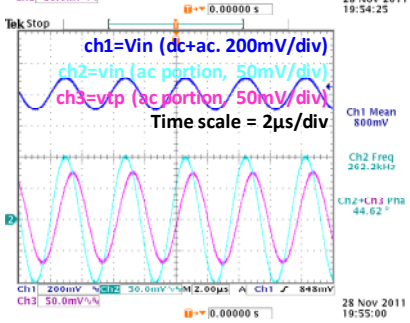

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 802mV
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 44.56 °
28 Nov 2011 19:53:59


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 801mV
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 44.98 °
28 Nov 2011 19:54:09


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 801mV
Ch2 Freq 261.0kHz
Ch2+Ch3 Pha 45.10 °
28 Nov 2011 19:54:16


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 801mV
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 45.21 °
28 Nov 2011 19:54:25

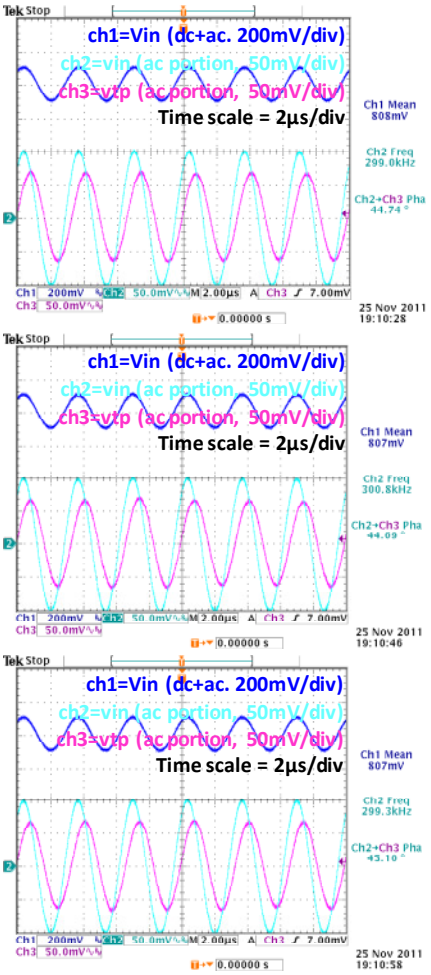

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 801mV
Ch2 Freq 261.0kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 19:54:40

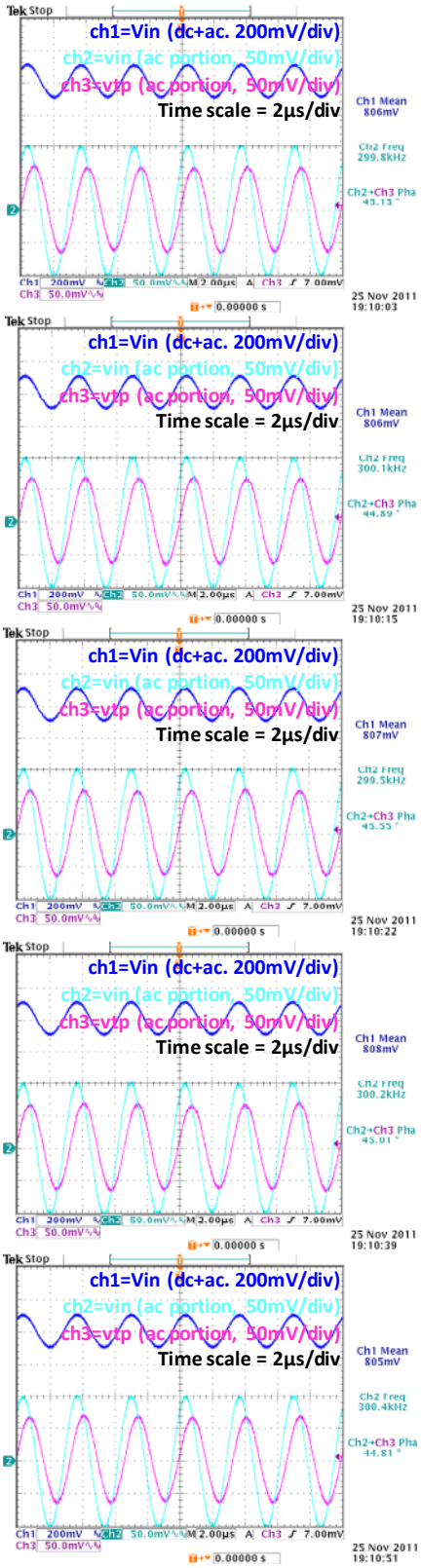

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 800mV
Ch2 Freq 262.2kHz
Ch2+Ch3 Pha 44.62 °
28 Nov 2011 19:55:00

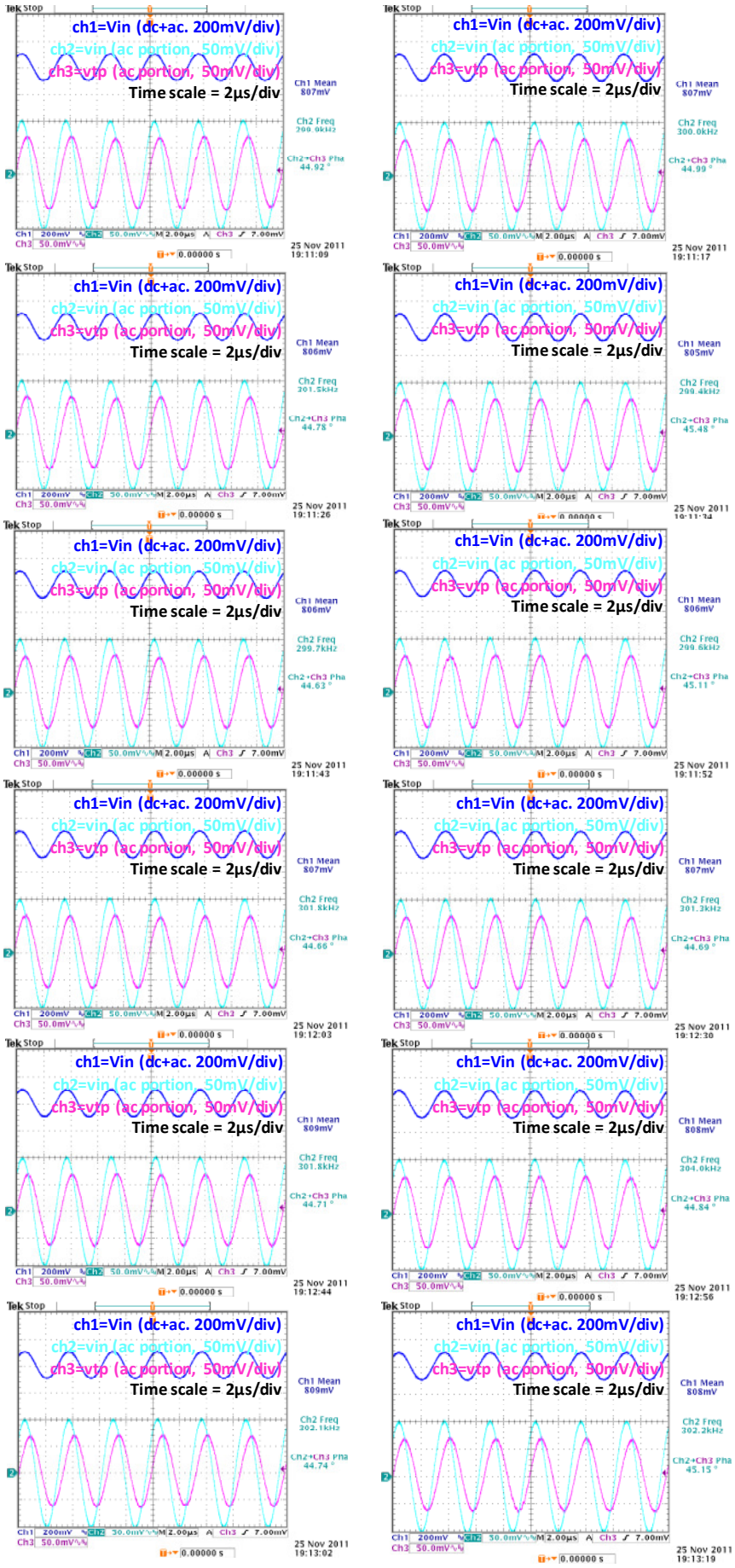
Measurements at PADONLY point with VBIAS=0.8V

RIN= 4.697E+04

Sample No.	*phase*	*f*	*c*
1	45.15	2.998E+05	1.14E-11
2	44.89	3.001E+05	1.12E-11
3	45.55	2.995E+05	1.15E-11
4	44.74	2.990E+05	1.12E-11
5	45.01	3.002E+05	1.13E-11
6	44.69	3.008E+05	1.11E-11
7	44.81	3.004E+05	1.12E-11
8	45.10	2.993E+05	1.14E-11
9	44.92	2.999E+05	1.13E-11
10	44.99	3.000E+05	1.13E-11
11	44.78	3.015E+05	1.12E-11
12	45.48	2.994E+05	1.15E-11
13	44.63	2.997E+05	1.12E-11
14	45.11	2.996E+05	1.14E-11
15	44.66	3.018E+05	1.11E-11
16	44.69	3.013E+05	1.11E-11
17	44.71	3.018E+05	1.11E-11
18	44.84	3.040E+05	1.11E-11
19	44.74	3.021E+05	1.11E-11
20	45.15	3.022E+05	1.13E-11
Average	44.93	3.006E+05	**1.125E-11**
STD	0.26	1.282E+03	**1.300E-13**



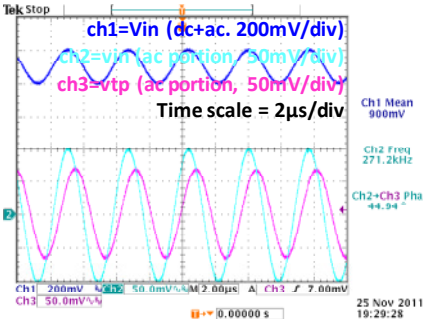


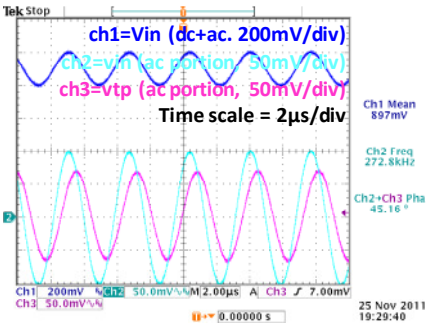

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 807mV
Ch2 Freq 300.0kHz
Ch2+Ch3 Pha 44.99 °
25 Nov 2011 19:11:17
Ch1 Mean 806mV
Ch2 Freq 301.5kHz
Ch2+Ch3 Pha 44.78 °
25 Nov 2011 19:11:26
Ch1 Mean 805mV
Ch2 Freq 299.4kHz
Ch2+Ch3 Pha 45.48 °
Ch1 Mean 806mV
Ch2 Freq 299.7kHz
Ch2+Ch3 Pha 44.63 °
25 Nov 2011 19:11:43
Ch1 Mean 806mV
Ch2 Freq 299.6kHz
Ch2+Ch3 Pha 45.11 °
25 Nov 2011 19:11:52
Ch1 Mean 807mV
Ch2 Freq 301.8kHz
Ch2+Ch3 Pha 44.66 °
25 Nov 2011 19:12:03
Ch1 Mean 807mV
Ch2 Freq 301.3kHz
Ch2+Ch3 Pha 44.69 °
25 Nov 2011 19:12:30
Ch1 Mean 809mV
Ch2 Freq 301.8kHz
Ch2+Ch3 Pha 44.71 °
25 Nov 2011 19:12:44
Ch1 Mean 808mV
Ch2 Freq 304.0kHz
Ch2+Ch3 Pha 44.84 °
25 Nov 2011 19:12:56
Ch1 Mean 809mV
Ch2 Freq 302.1kHz
Ch2+Ch3 Pha 44.74 °
25 Nov 2011 19:13:02
Ch1 Mean 808mV
Ch2 Freq 302.2kHz
Ch2+Ch3 Pha 45.15 °
25 Nov 2011 19:13:19

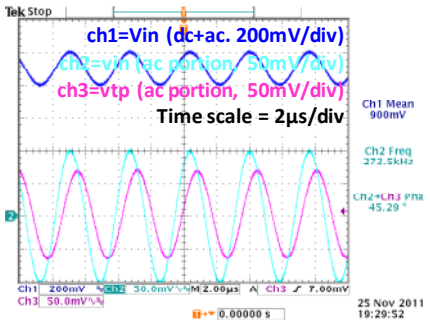
Measurements at NoQFG point with VBIAS=0.9V

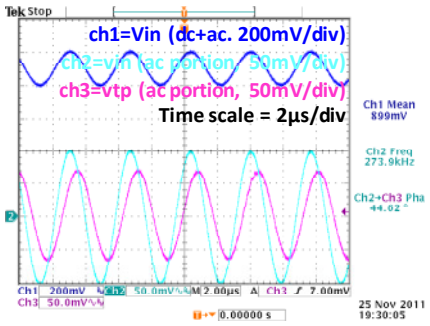
RIN= 4.697E+04

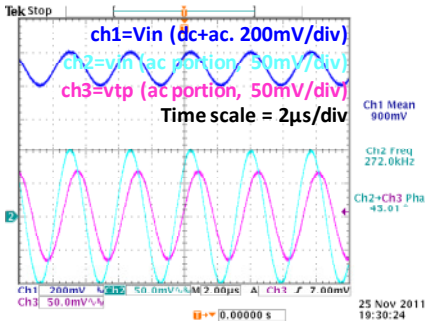
Sample No.	*phase*	*f*	*c*
1	44.94	2.712E+05	1.25E-11
2	45.16	2.728E+05	1.25E-11
3	45.29	2.735E+05	1.25E-11
4	44.96	2.730E+05	1.24E-11
5	44.62	2.739E+05	1.22E-11
6	44.61	2.717E+05	1.23E-11
7	45.01	2.720E+05	1.25E-11
8	45.12	2.724E+05	1.25E-11
9	45.00	2.729E+05	1.24E-11
10	45.21	2.736E+05	1.25E-11
11	44.58	2.740E+05	1.22E-11
12	45.08	2.730E+05	1.24E-11
13	44.78	2.736E+05	1.23E-11
14	44.67	2.743E+05	1.22E-11
15	44.93	2.756E+05	1.23E-11
16	45.17	2.737E+05	1.25E-11
17	45.18	2.733E+05	1.25E-11
18	44.65	2.744E+05	1.22E-11
19	45.17	2.738E+05	1.24E-11
20	45.10	2.728E+05	1.25E-11
Average	44.96	2.733E+05	**1.238E-11**
STD	0.23	1.007E+03	**1.158E-13**

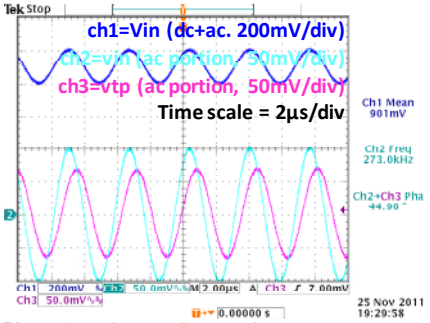


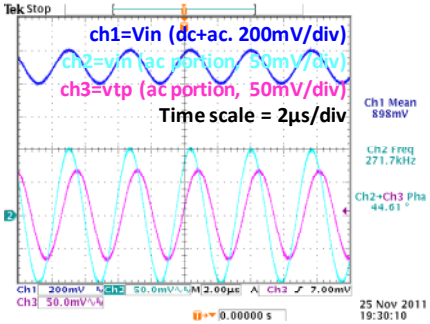


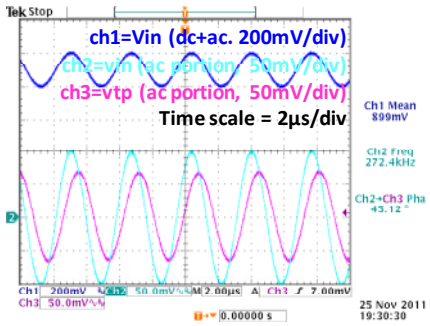


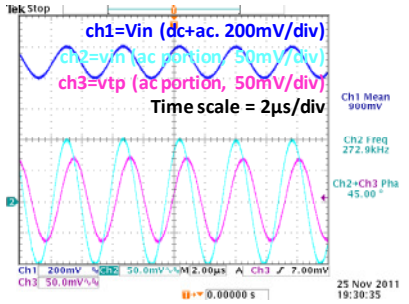


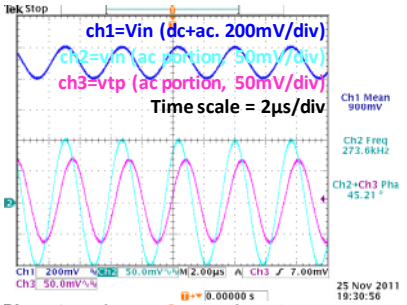


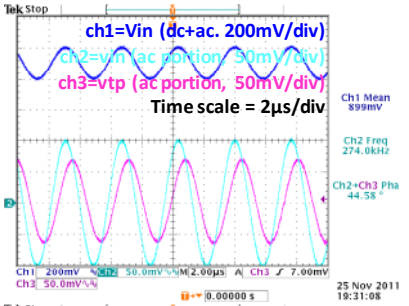


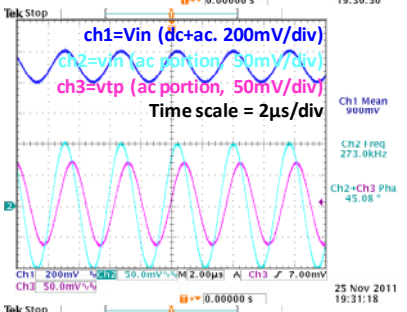


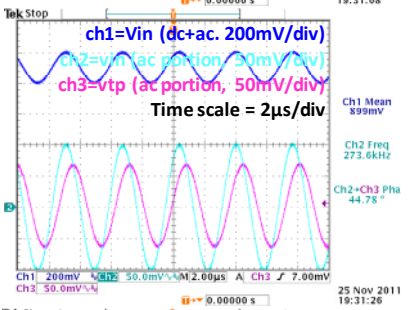


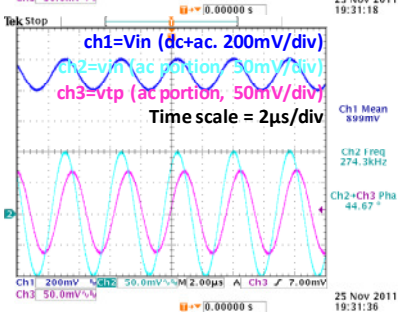

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2 Freq
272.9kHz
Ch2+Ch3 Pha
45.00 °
25 Nov 2011
19:30:35

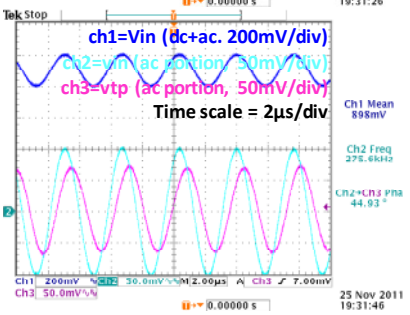

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2 Freq
273.6kHz
Ch2+Ch3 Pha
45.21 °
25 Nov 2011
19:30:56

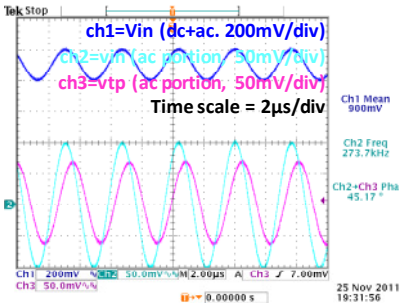

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
899mV
Ch2 Freq
274.0kHz
Ch2+Ch3 Pha
44.58 °
25 Nov 2011
19:31:08

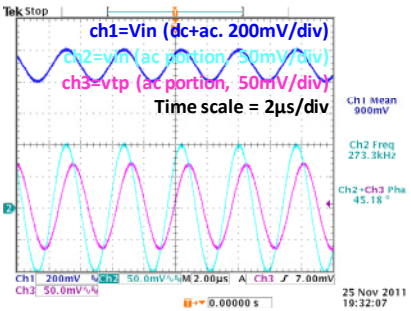

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2 Freq
273.0kHz
Ch2+Ch3 Pha
45.08 °
25 Nov 2011
19:31:18

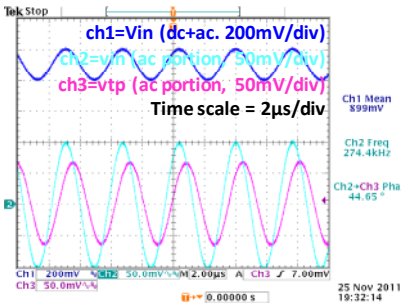

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
899mV
Ch2 Freq
273.6kHz
Ch2+Ch3 Pha
44.78 °
25 Nov 2011
19:31:26

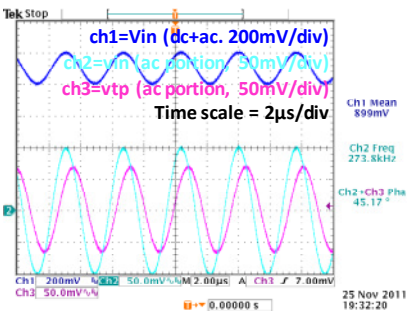

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
899mV
Ch2 Freq
274.3kHz
Ch2+Ch3 Pha
44.67 °
25 Nov 2011
19:31:36

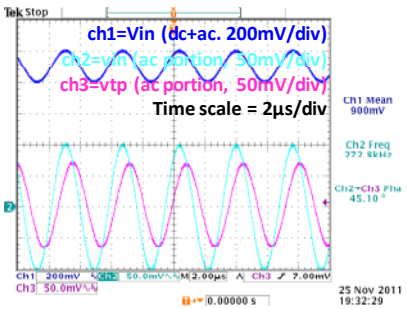

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
898mV
Ch2 Freq
275.6kHz
Ch2+Ch3 Pha
44.93 °
25 Nov 2011
19:31:46


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2 Freq
273.7kHz
Ch2+Ch3 Pha
45.17 °
25 Nov 2011
19:31:56


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2 Freq
273.3kHz
Ch2+Ch3 Pha
45.18 °
25 Nov 2011
19:32:07


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
899mV
Ch2 Freq
274.4kHz
Ch2+Ch3 Pha
44.65 °
25 Nov 2011
19:32:14

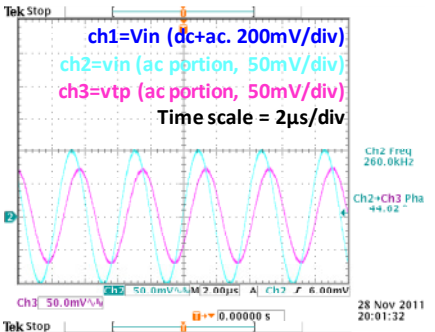

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
899mV
Ch2 Freq
273.8kHz
Ch2+Ch3 Pha
45.17 °
25 Nov 2011
19:32:20

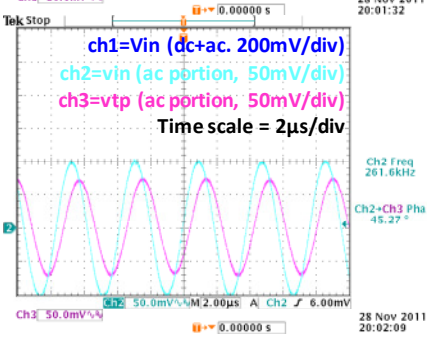

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean
900mV
Ch2+Ch3 Pha
45.10 °
25 Nov 2011
19:32:29

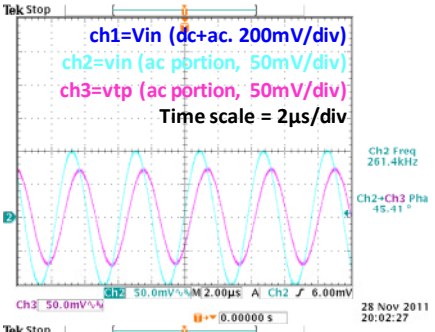
Measurements at QFG point with VBIAS=0.9V

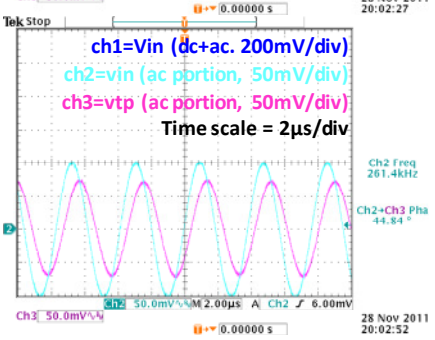
RIN= 4.697E+04

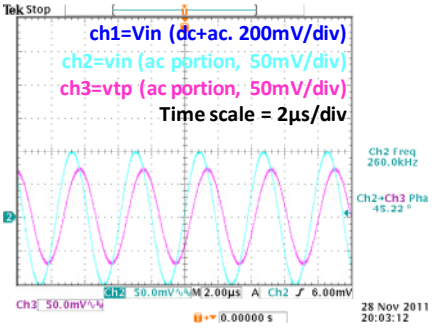
Sample No.	*phase*	*f*	*c*
1	44.62	2.600E+05	1.29E-11
2	45.27	2.616E+05	1.31E-11
3	45.41	2.614E+05	1.31E-11
4	44.70	2.606E+05	1.29E-11
5	44.84	2.614E+05	1.29E-11
6	44.53	2.601E+05	1.28E-11
7	45.22	2.600E+05	1.31E-11
8	45.10	2.608E+05	1.30E-11
9	44.74	2.607E+05	1.29E-11
10	45.20	2.606E+05	1.31E-11
11	44.88	2.612E+05	1.29E-11
12	45.08	2.610E+05	1.30E-11
13	44.86	2.609E+05	1.29E-11
14	44.58	2.609E+05	1.28E-11
15	44.53	2.603E+05	1.28E-11
16	44.55	2.615E+05	1.28E-11
17	45.07	2.608E+05	1.30E-11
18	44.82	2.617E+05	1.29E-11
19	45.16	2.602E+05	1.31E-11
20	44.82	2.606E+05	1.29E-11
Average	44.90	2.608E+05	**1.295E-11**
STD	0.27	5.324E+02	**1.216E-13**

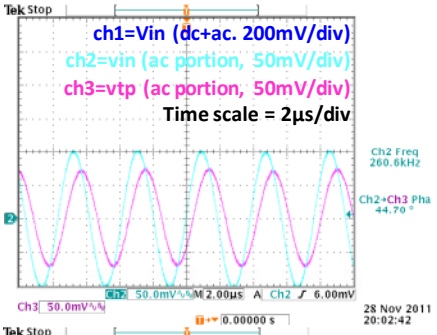


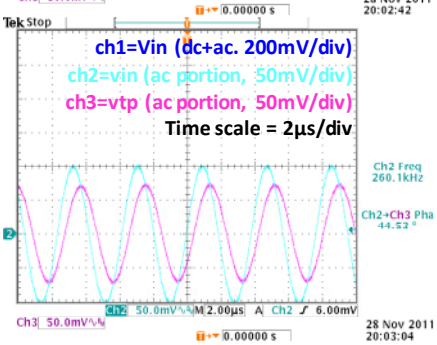


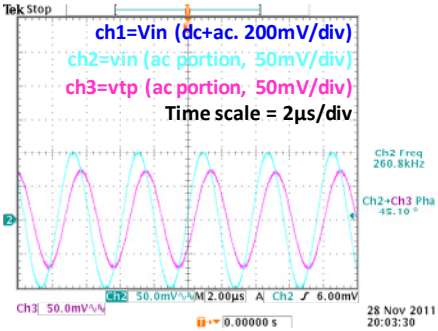


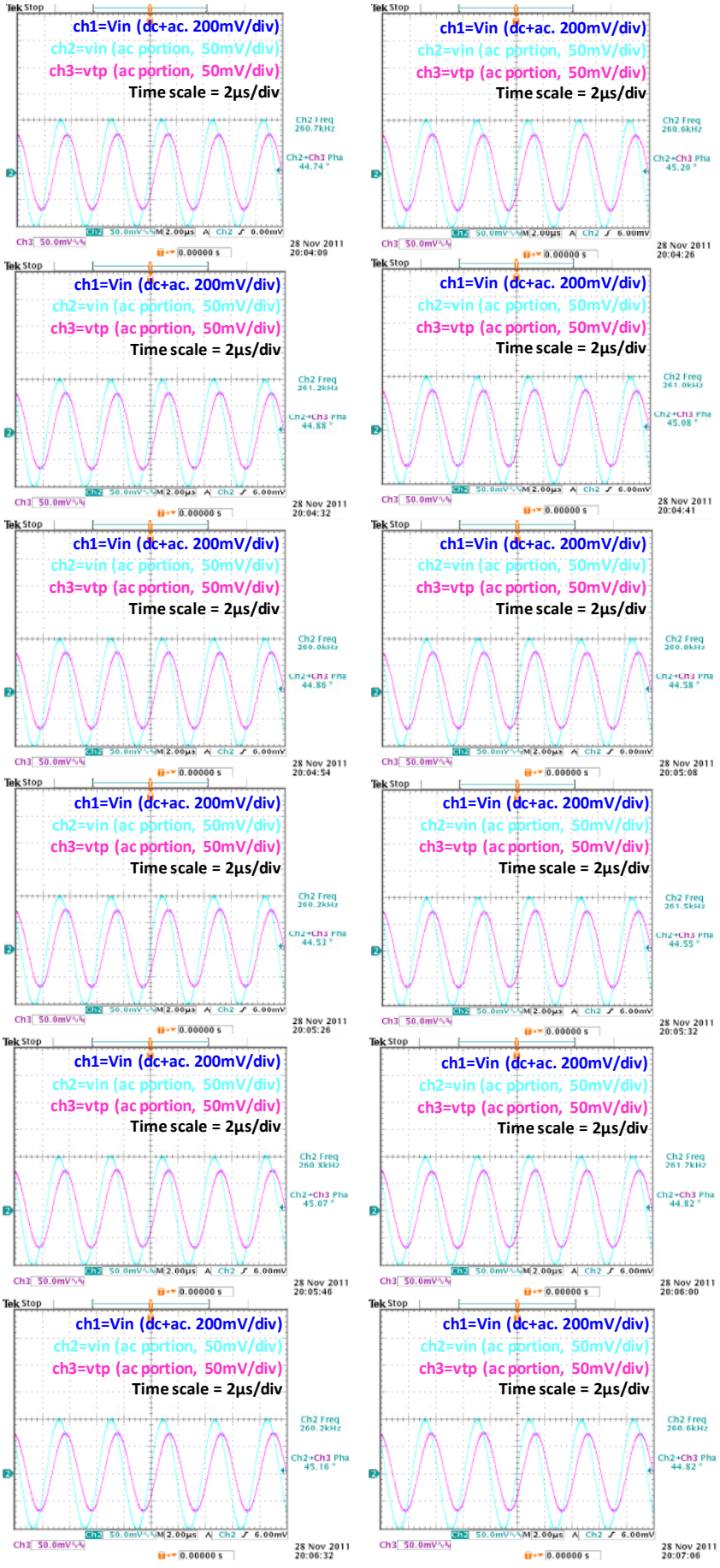








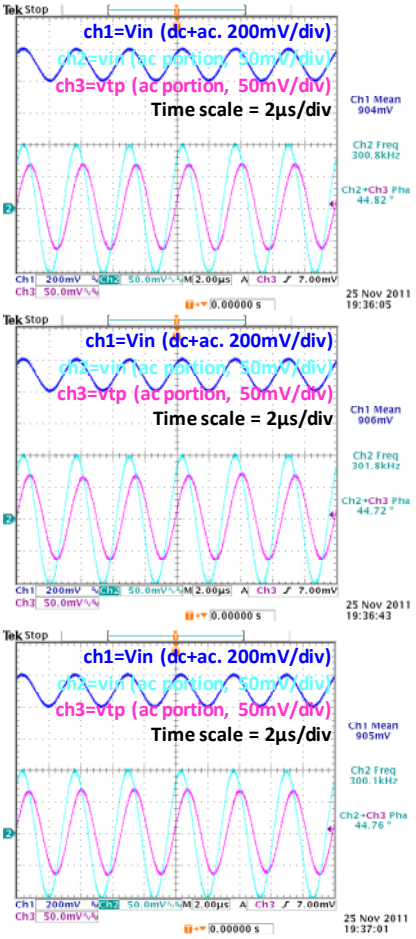


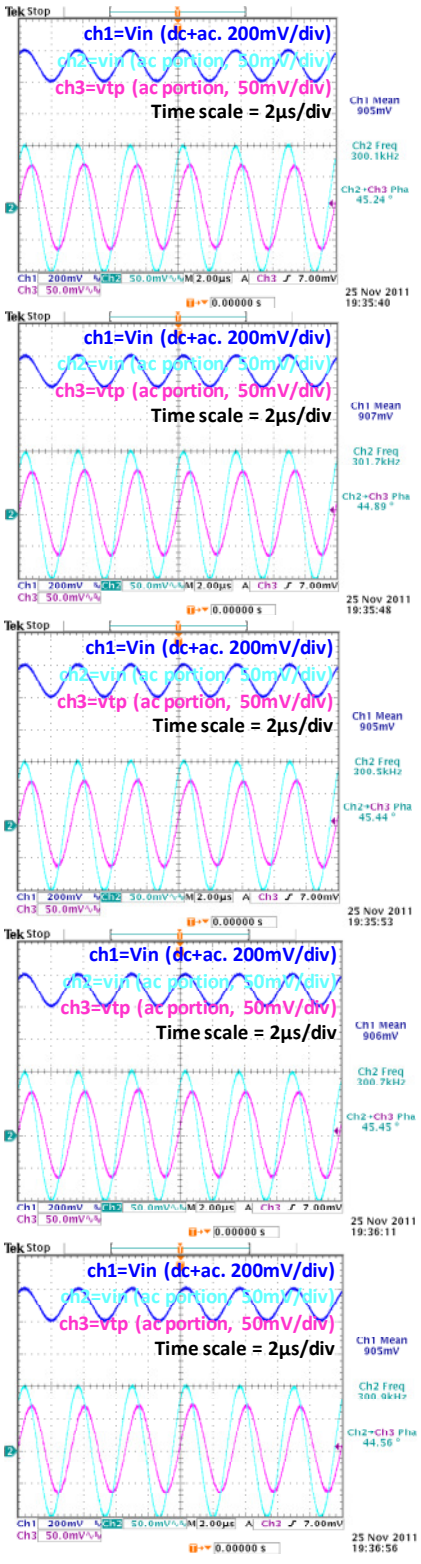

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch2 Freq 260.7kHz
Ch2+Ch3 Pha 44.74 °
28 Nov 2011 20:04:09
Ch2 Freq 260.6kHz
Ch2+Ch3 Pha 45.20 °
28 Nov 2011 20:04:26
Ch2 Freq 261.2kHz
Ch2+Ch3 Pha 44.88 °
28 Nov 2011 20:04:32
Ch2 Freq 261.0kHz
Ch2+Ch3 Pha 45.08 °
28 Nov 2011 20:04:41
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 44.86 °
28 Nov 2011 20:04:54
Ch2 Freq 260.0kHz
Ch2+Ch3 Pha 44.58 °
28 Nov 2011 20:05:08
Ch2 Freq 260.2kHz
Ch2+Ch3 Pha 44.53 °
28 Nov 2011 20:05:26
Ch2 Freq 261.5kHz
Ch2+Ch3 Pha 44.55 °
28 Nov 2011 20:05:32
Ch2 Freq 260.5kHz
Ch2+Ch3 Pha 45.07 °
28 Nov 2011 20:05:46
Ch2 Freq 261.7kHz
Ch2+Ch3 Pha 44.82 °
28 Nov 2011 20:06:00
Ch2 Freq 260.2kHz
Ch2+Ch3 Pha 45.16 °
28 Nov 2011 20:06:32
Ch2 Freq 260.6kHz
Ch2+Ch3 Pha 44.82 °
28 Nov 2011 20:07:06

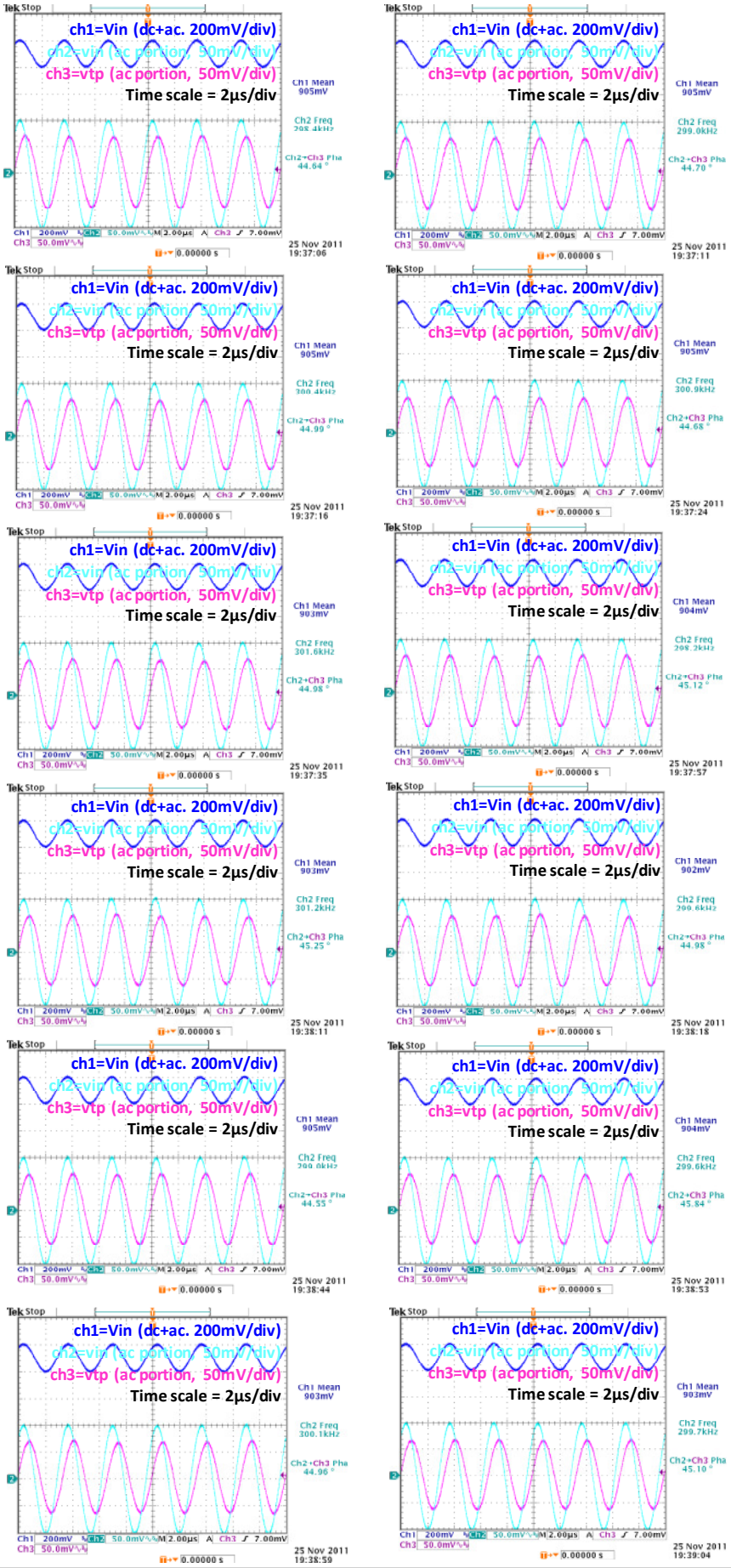
Measurements at PADONLY point with VBIAS=0.9V

RIN= 4.697E+04

Sample No.	*phase*	*f*	*c*
1	45.24	3.001E+05	1.14E-11
2	44.89	3.017E+05	1.12E-11
3	45.44	3.005E+05	1.15E-11
4	44.82	3.008E+05	1.12E-11
5	45.45	3.007E+05	1.14E-11
6	44.72	3.018E+05	1.11E-11
7	44.56	3.009E+05	1.11E-11
8	44.76	3.001E+05	1.12E-11
9	44.64	2.984E+05	1.12E-11
10	44.70	2.990E+05	1.12E-11
11	44.99	3.004E+05	1.13E-11
12	44.68	3.009E+05	1.11E-11
13	44.98	3.016E+05	1.12E-11
14	45.12	2.982E+05	1.14E-11
15	45.25	3.012E+05	1.13E-11
16	44.98	2.996E+05	1.13E-11
17	44.55	2.990E+05	1.12E-11
18	45.84	2.996E+05	1.16E-11
19	44.96	3.001E+05	1.13E-11
20	45.10	2.997E+05	1.13E-11
Average	44.98	3.002E+05	**1.128E-11**
STD	0.34	1.041E+03	**1.380E-13**



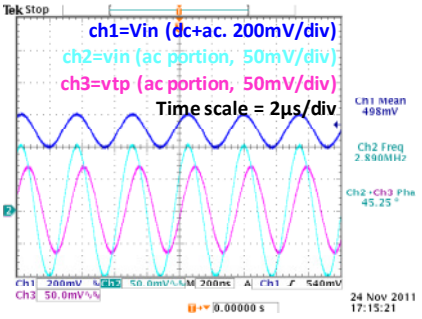


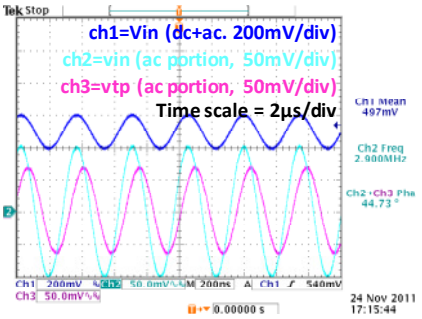

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 905mV
Ch2 Freq 298.4kHz
Ch2→Ch3 Pha 44.64 °
25 Nov 2011 19:37:06
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 905mV
Ch2 Freq 299.0kHz
Ch2→Ch3 Pha 44.70 °
25 Nov 2011 19:37:11
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 905mV
Ch2 Freq 300.4kHz
Ch2→Ch3 Pha 44.99 °
25 Nov 2011 19:37:16
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 905mV
Ch2 Freq 300.9kHz
Ch2→Ch3 Pha 44.68 °
25 Nov 2011 19:37:24
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 903mV
Ch2 Freq 301.6kHz
Ch2→Ch3 Pha 44.98 °
25 Nov 2011 19:37:35
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 904mV
Ch2 Freq 299.2kHz
Ch2→Ch3 Pha 45.12 °
25 Nov 2011 19:37:57
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 903mV
Ch2 Freq 301.2kHz
Ch2→Ch3 Pha 45.25 °
25 Nov 2011 19:38:11
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 902mV
Ch2 Freq 299.6kHz
Ch2→Ch3 Pha 44.98 °
25 Nov 2011 19:38:18
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 905mV
Ch2 Freq 300.0kHz
Ch2→Ch3 Pha 44.55 °
25 Nov 2011 19:38:44
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 904mV
Ch2 Freq 299.6kHz
Ch2→Ch3 Pha 45.84 °
25 Nov 2011 19:38:53
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 903mV
Ch2 Freq 300.1kHz
Ch2→Ch3 Pha 44.96 °
25 Nov 2011 19:38:59
Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 903mV
Ch2 Freq 299.7kHz
Ch2→Ch3 Pha 45.10 °
25 Nov 2011 19:39:04

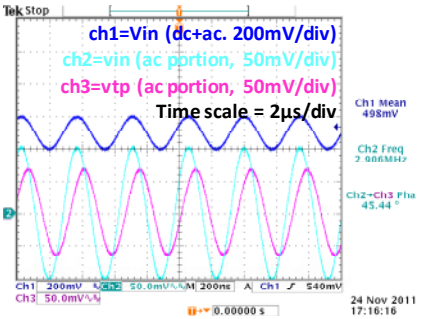
testsignal noQFG with 200mV 4k7 @0.5V

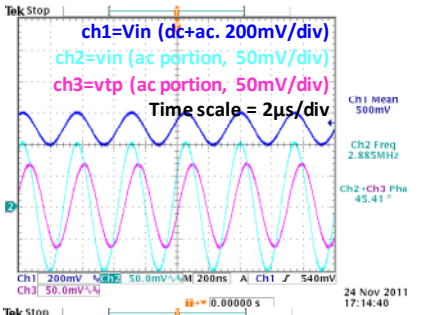
RIN= 4.692E+03

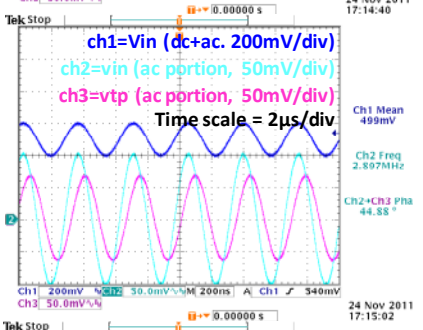
Sample No.	*phase*	*f*	*c*
1	45.41	2.885E+06	1.19E-11
2	44.88	2.897E+06	1.17E-11
3	45.35	2.901E+06	1.18E-11
4	45.25	2.890E+06	1.18E-11
5	45.21	2.897E+06	1.18E-11
6	44.73	2.900E+06	1.16E-11
7	44.60	2.905E+06	1.15E-11
8	45.44	2.906E+06	1.19E-11
9	44.68	2.900E+06	1.16E-11
10	45.37	2.971E+06	1.16E-11
11	45.35	2.903E+06	1.18E-11
12	45.43	2.897E+06	1.19E-11
13	45.11	2.896E+06	1.18E-11
14	45.07	2.892E+06	1.18E-11
15	45.18	2.894E+06	1.18E-11
16	44.64	2.904E+06	1.15E-11
17	45.56	2.901E+06	1.19E-11
18	44.82	2.896E+06	1.16E-11
19	44.50	2.909E+06	1.15E-11
20	44.64	2.900E+06	1.16E-11
Average	45.06	2.902E+06	**1.171E-11**
STD	0.34	1.716E+04	**1.506E-13**

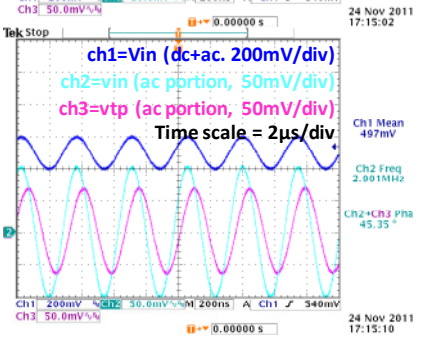


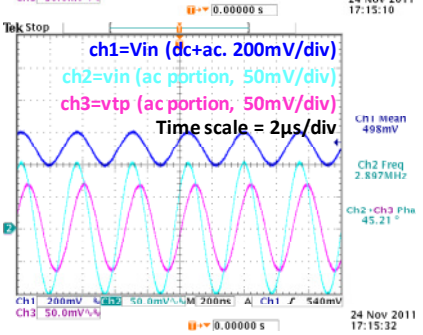


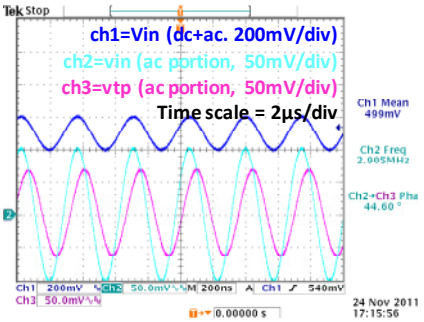


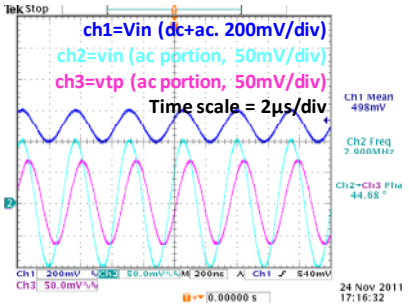


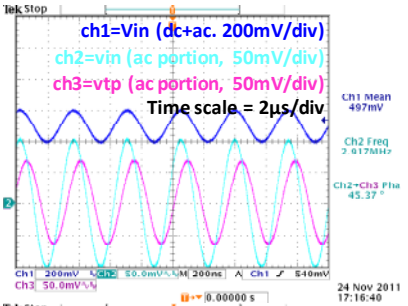


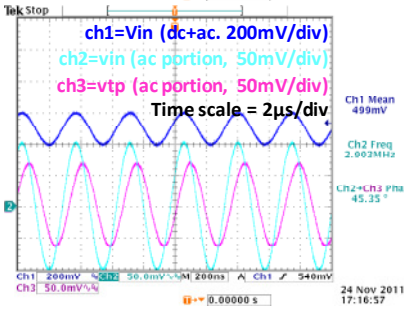


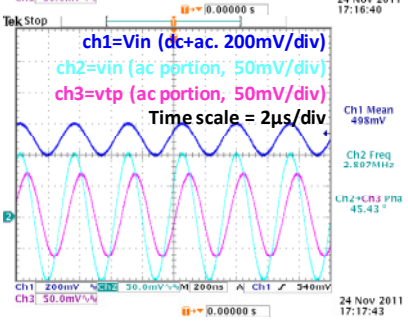


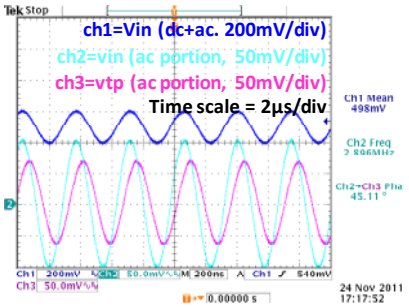


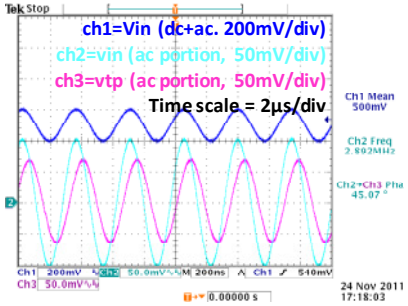

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 2.900MHz
Ch2+Ch3 Pha 44.68°
24 Nov 2011 17:16:32

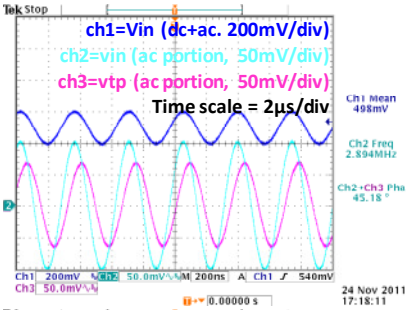

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 497mV
Ch2 Freq 2.917MHz
Ch2+Ch3 Pha 45.37°
24 Nov 2011 17:16:40

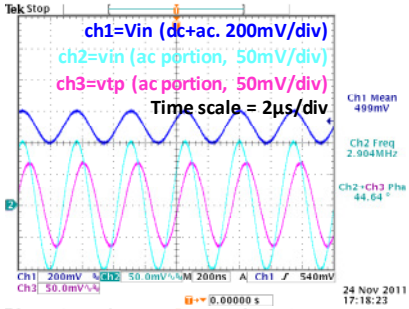

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 2.902MHz
Ch2+Ch3 Pha 45.35°
24 Nov 2011 17:16:57

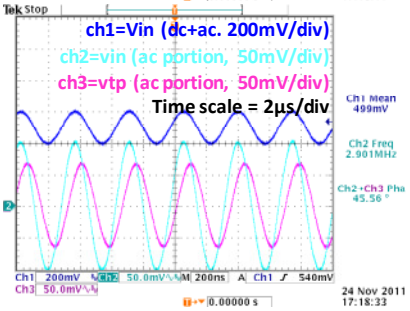

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 2.807MHz
Ch2+Ch3 Pha 45.43°
24 Nov 2011 17:17:43

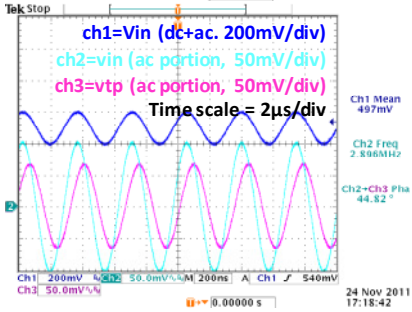

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 2.806MHz
Ch2+Ch3 Pha 45.11°
24 Nov 2011 17:17:52

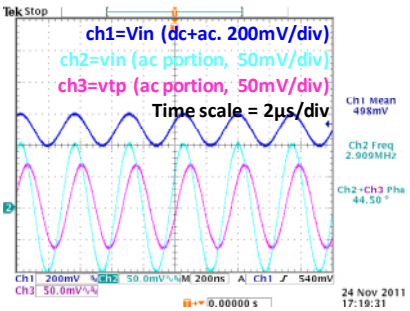

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 2.803MHz
Ch2+Ch3 Pha 45.07°
24 Nov 2011 17:18:03

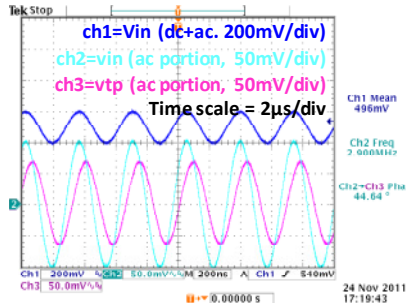

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 2.894MHz
Ch2+Ch3 Pha 45.18°
24 Nov 2011 17:18:11


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 2.904MHz
Ch2+Ch3 Pha 44.64°
24 Nov 2011 17:18:23


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 2.901MHz
Ch2+Ch3 Pha 45.56°
24 Nov 2011 17:18:33


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 497mV
Ch2 Freq 2.896MHz
Ch2+Ch3 Pha 44.82°
24 Nov 2011 17:18:42

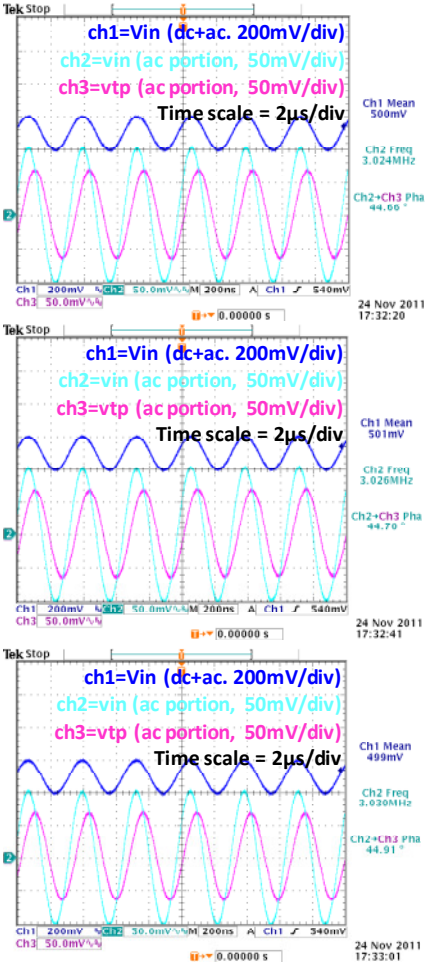

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 498mV
Ch2 Freq 2.909MHz
Ch2+Ch3 Pha 44.50°
24 Nov 2011 17:19:31

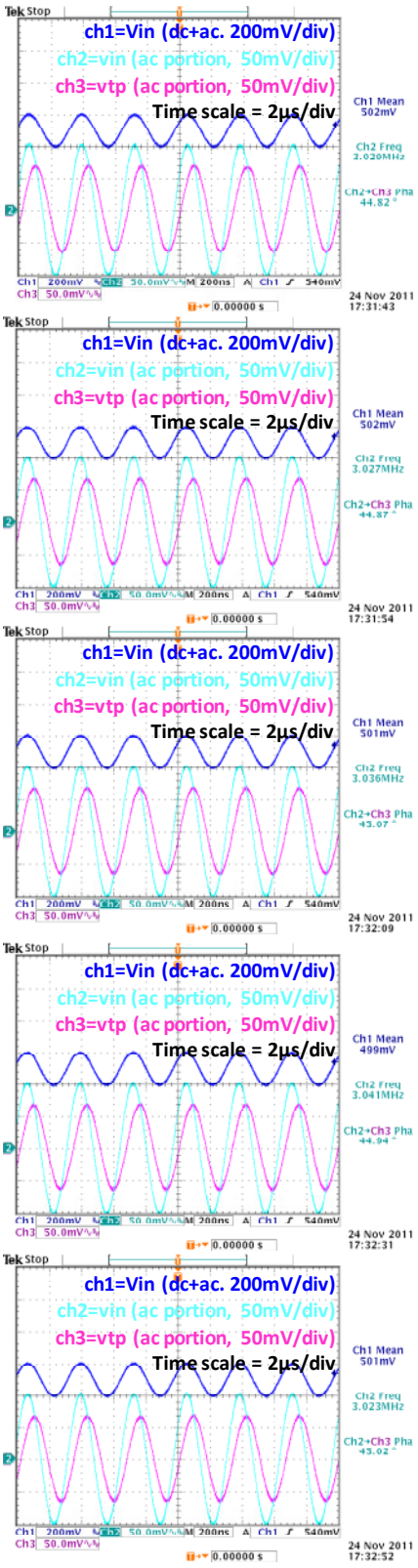

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 496mV
Ch2 Freq 2.908MHz
Ch2+Ch3 Pha 44.64°
24 Nov 2011 17:19:43

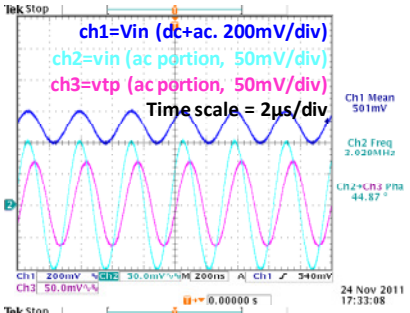
testsignal PADONLY with 200mV 4k7 @0.5V

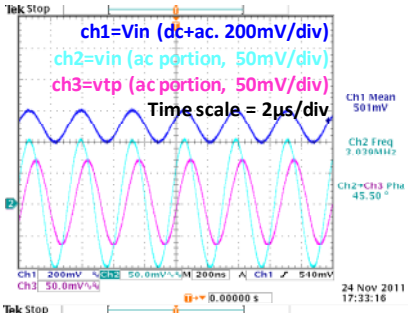
RIN= 4.692E+03

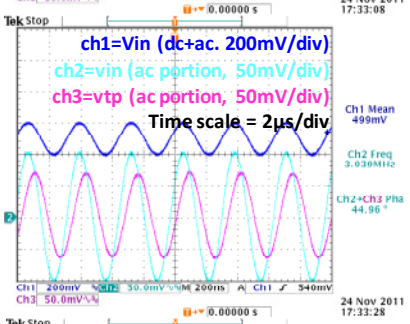
Sample No.	*phase*	*f*	*c*
1	44.82	3.029E+06	1.11E-11
2	44.87	3.027E+06	1.12E-11
3	45.07	3.036E+06	1.12E-11
4	44.66	3.024E+06	1.11E-11
5	44.94	3.041E+06	1.11E-11
6	44.70	3.026E+06	1.11E-11
7	45.02	3.023E+06	1.12E-11
8	44.91	3.030E+06	1.12E-11
9	44.87	3.029E+06	1.11E-11
10	45.50	3.039E+06	1.14E-11
11	44.96	3.039E+06	1.11E-11
12	45.47	3.027E+06	1.14E-11
13	45.32	3.029E+06	1.13E-11
14	45.24	3.032E+06	1.13E-11
15	44.52	3.028E+06	1.10E-11
16	44.65	3.043E+06	1.10E-11
17	45.00	3.041E+06	1.12E-11
18	45.31	3.019E+06	1.14E-11
19	45.10	3.024E+06	1.13E-11
20	45.24	3.022E+06	1.13E-11
Average	45.01	3.030E+06	**1.120E-11**
STD	0.27	7.096E+03	**1.128E-13**

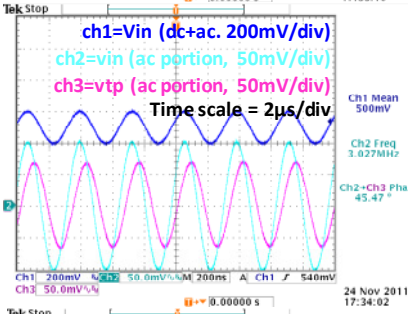


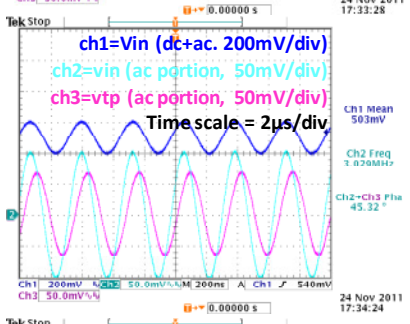


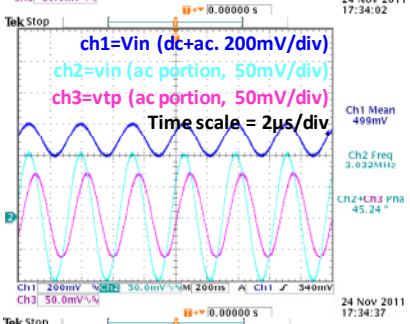

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.020MHz
Ch2+Ch3 Pha 44.87°
24 Nov 2011 17:33:08

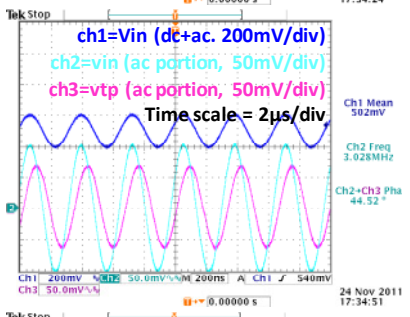

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.030MHz
Ch2+Ch3 Pha 45.50°
24 Nov 2011 17:33:16

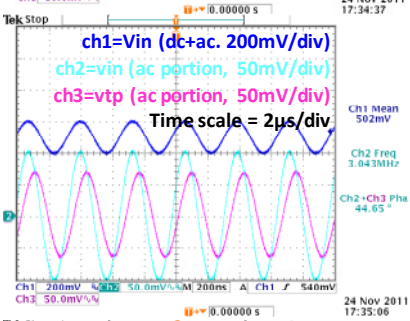

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 3.030MHz
Ch2+Ch3 Pha 44.96°
24 Nov 2011 17:33:28

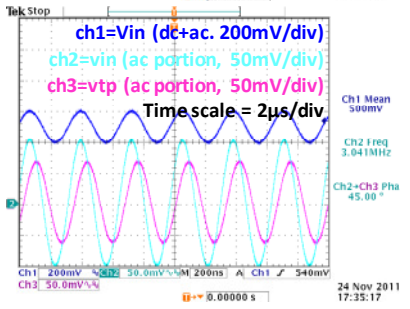

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.027MHz
Ch2+Ch3 Pha 45.47°
24 Nov 2011 17:34:02

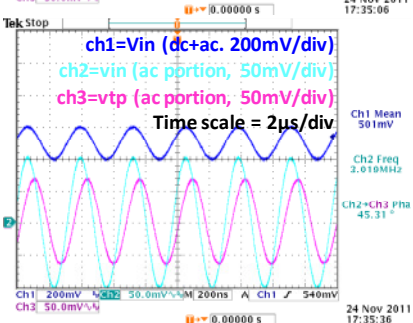

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 503mV
Ch2 Freq 3.030MHz
Ch2+Ch3 Pha 45.32°
24 Nov 2011 17:34:24

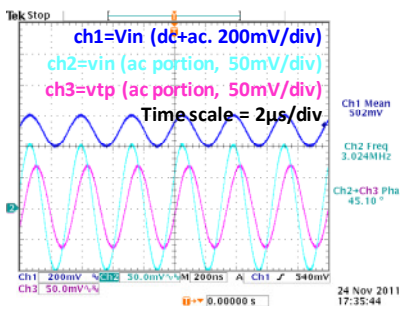

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 499mV
Ch2 Freq 3.032MHz
Ch2+Ch3 Pha 45.24°
24 Nov 2011 17:34:37

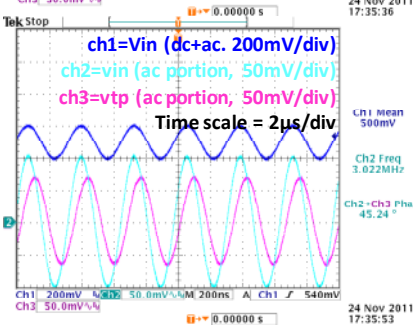

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.028MHz
Ch2+Ch3 Pha 44.52°
24 Nov 2011 17:34:51


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.043MHz
Ch2+Ch3 Pha 44.65°
24 Nov 2011 17:35:06


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.041MHz
Ch2+Ch3 Pha 45.00°
24 Nov 2011 17:35:17


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.019MHz
Ch2+Ch3 Pha 45.31°
24 Nov 2011 17:35:36

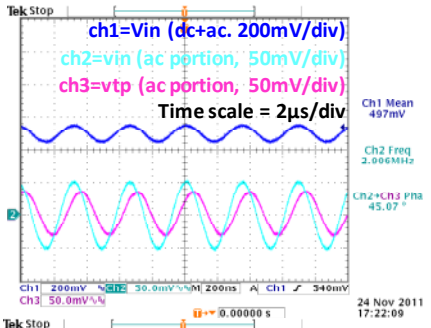

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.024MHz
Ch2+Ch3 Pha 45.10°
24 Nov 2011 17:35:44

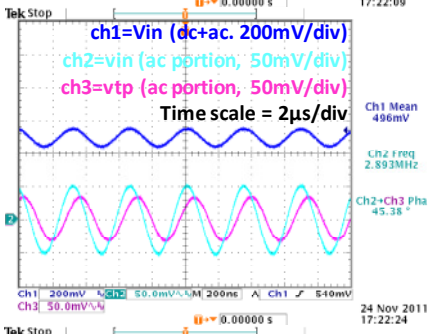

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.022MHz
Ch2+Ch3 Pha 45.24°
24 Nov 2011 17:35:53

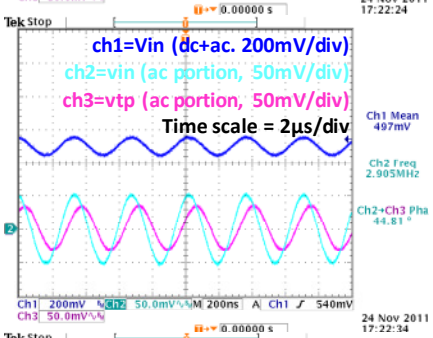
testsignal noQFG with 100mV 4k7 @0.5V

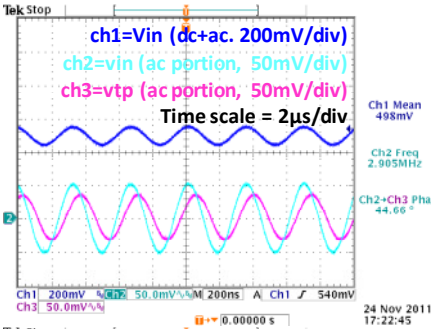
RIN= 4.692E+03

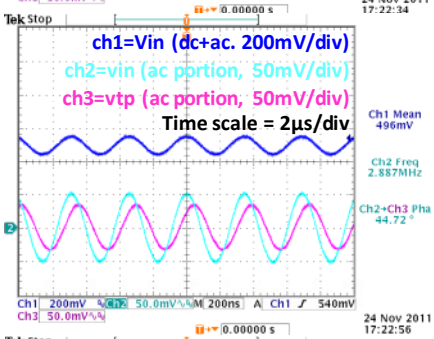
Sample No.	*phase*	*f*	*c*
1	45.07	2.906E+06	1.17E-11
2	45.38	2.893E+06	1.19E-11
3	44.81	2.905E+06	1.16E-11
4	44.66	2.905E+06	1.15E-11
5	44.72	2.887E+06	1.16E-11
6	45.31	2.906E+06	1.18E-11
7	44.69	2.877E+06	1.17E-11
8	45.00	2.867E+06	1.18E-11
9	45.35	2.889E+06	1.19E-11
10	45.50	2.895E+06	1.19E-11
11	45.30	2.904E+06	1.18E-11
12	44.50	2.879E+06	1.16E-11
13	45.39	2.885E+06	1.19E-11
14	45.50	2.875E+06	1.20E-11
15	45.23	2.919E+06	1.17E-11
16	45.49	2.972E+06	1.16E-11
17	45.09	2.879E+06	1.18E-11
18	45.28	2.937E+06	1.17E-11
19	45.22	2.940E+06	1.16E-11
20	45.07	2.886E+06	1.18E-11
Average	45.13	2.900E+06	**1.175E-11**
STD	0.31	2.571E+04	**1.340E-13**

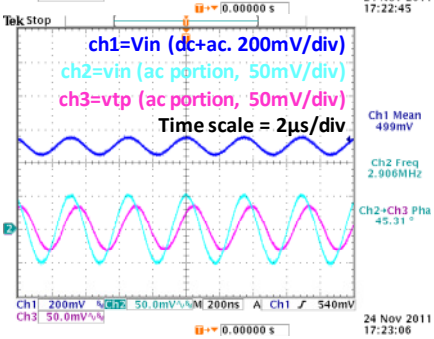


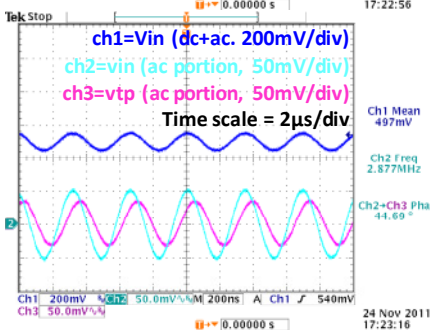


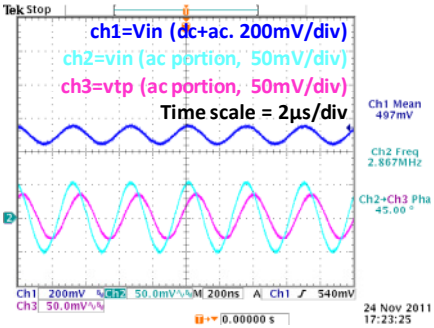


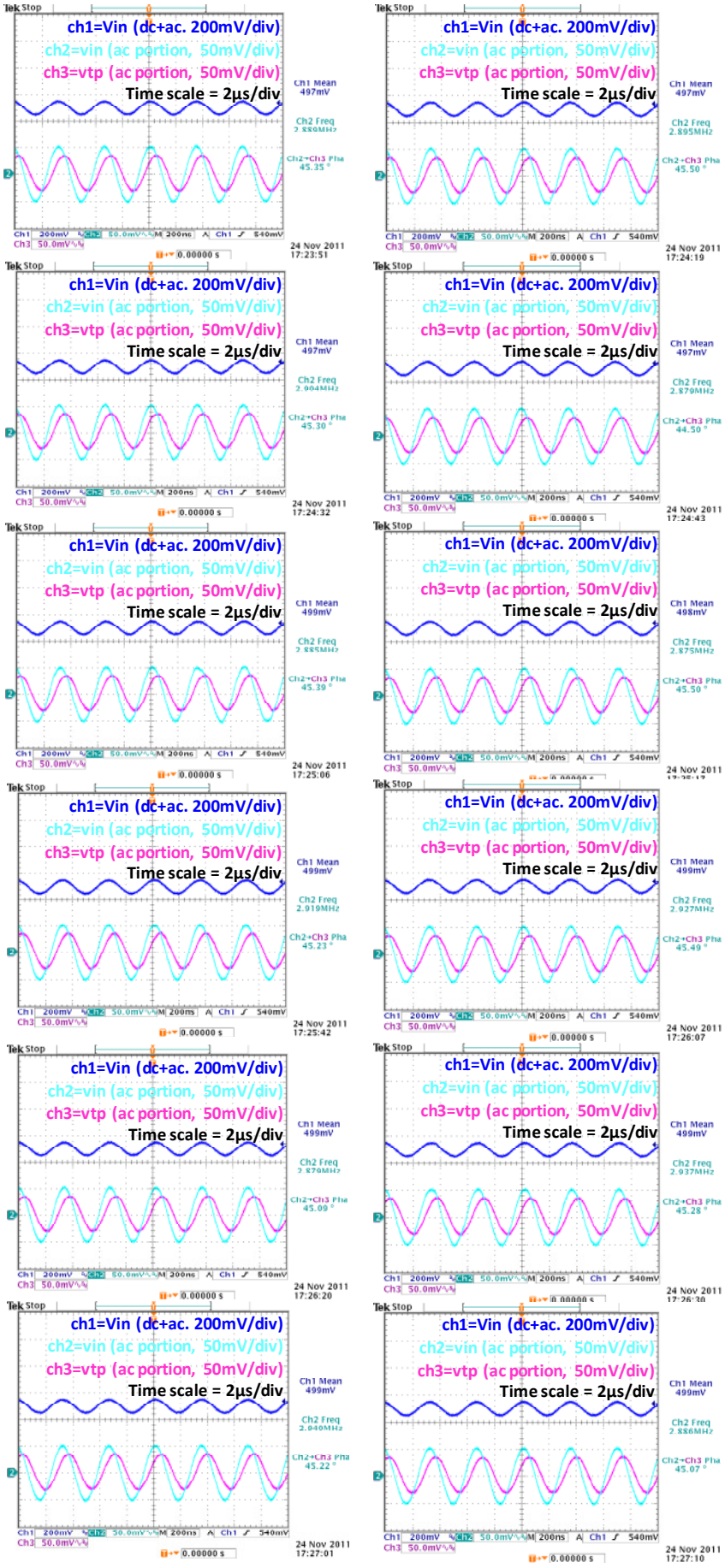








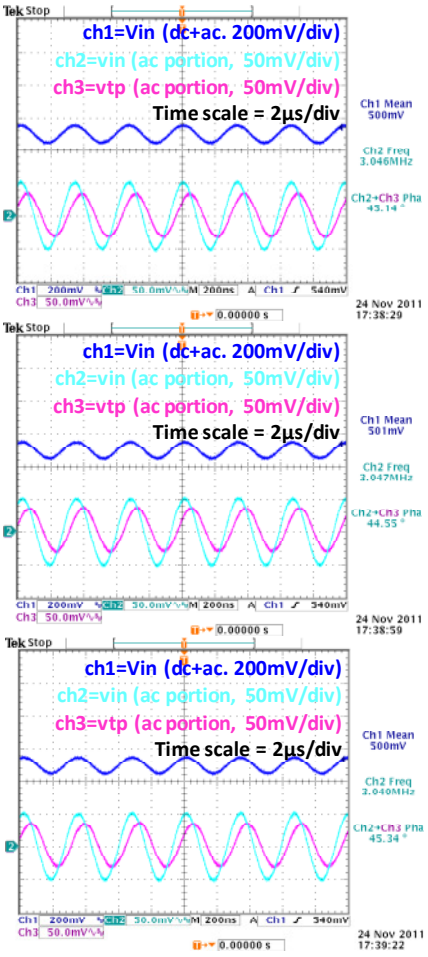


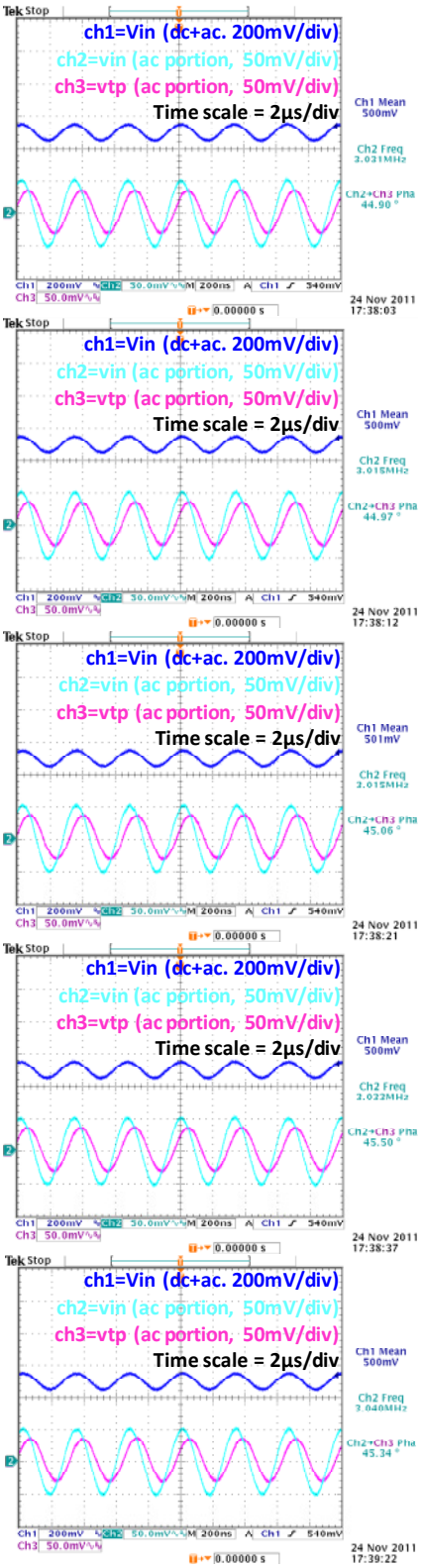

ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div

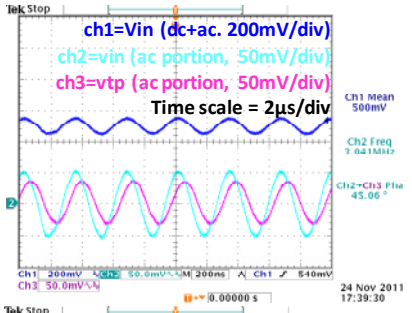
testsignal PADONLY with 100mV 4k7 @0.5V

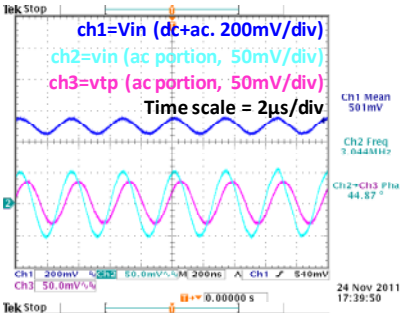
RIN= 4.692E+03

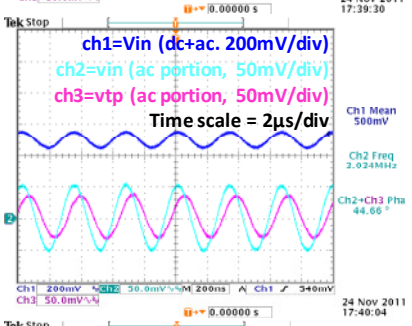
Sample No.	*phase*	*f*	*c*
1	44.90	3.031E+06	1.12E-11
2	44.97	3.015E+06	1.12E-11
3	45.06	3.015E+06	1.13E-11
4	45.14	3.046E+06	1.12E-11
5	45.50	3.033E+06	1.14E-11
6	45.55	3.047E+06	1.13E-11
7	45.06	3.046E+06	1.12E-11
8	45.34	3.040E+06	1.13E-11
9	45.06	3.041E+06	1.12E-11
10	44.87	3.044E+06	1.11E-11
11	44.66	3.034E+06	1.10E-11
12	44.62	3.035E+06	1.10E-11
13	45.53	3.052E+06	1.13E-11
14	44.56	3.035E+06	1.10E-11
15	44.59	3.036E+06	1.10E-11
16	44.51	3.029E+06	1.10E-11
17	44.46	3.021E+06	1.10E-11
18	45.45	3.036E+06	1.13E-11
19	44.55	3.038E+06	1.10E-11
20	45.02	3.021E+06	1.12E-11
Average	44.97	3.035E+06	**1.117E-11**
STD	0.37	1.045E+04	**1.337E-13**

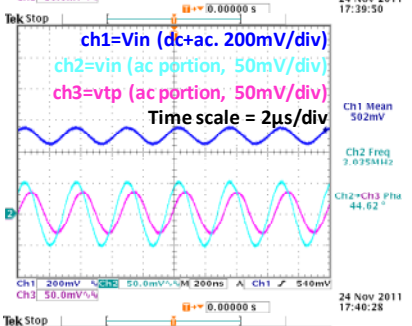


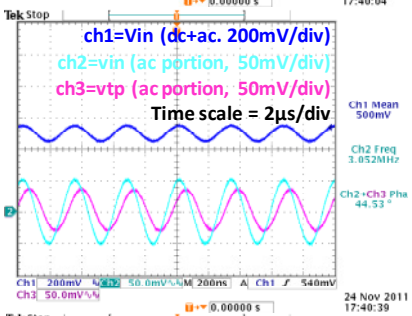


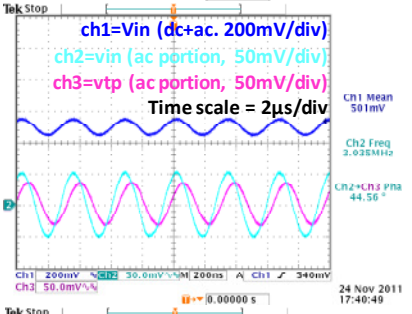

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.041MHz
Ch2+Ch3 Pha 45.06 °
24 Nov 2011 17:39:30

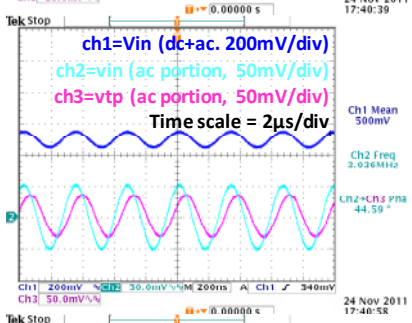

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.044MHz
Ch2+Ch3 Pha 44.87 °
24 Nov 2011 17:39:50

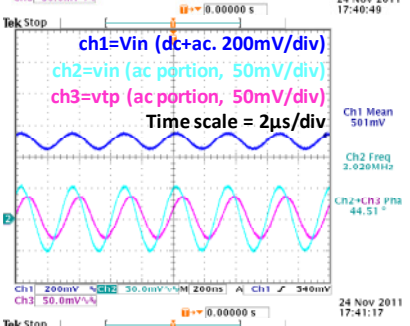

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.034MHz
Ch2+Ch3 Pha 44.66 °
24 Nov 2011 17:40:04

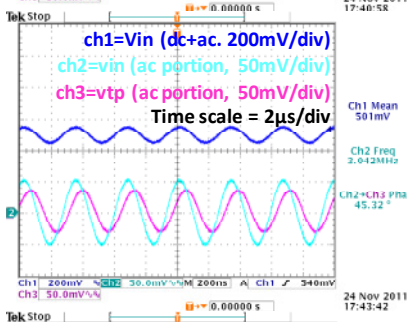

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.035MHz
Ch2+Ch3 Pha 44.62 °
24 Nov 2011 17:40:28

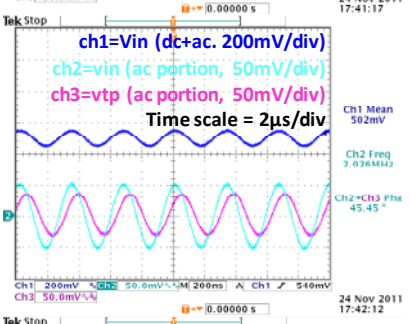

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.052MHz
Ch2+Ch3 Pha 44.53 °
24 Nov 2011 17:40:39

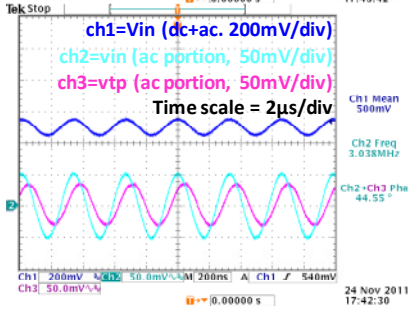

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.038MHz
Ch2+Ch3 Pha 44.56 °
24 Nov 2011 17:40:49

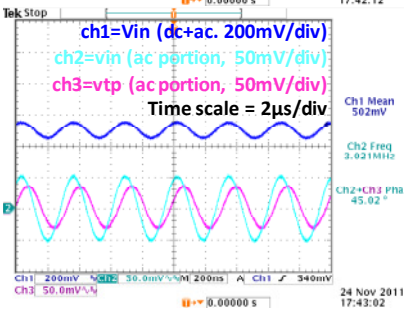

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.036MHz
Ch2+Ch3 Pha 44.59 °
24 Nov 2011 17:40:58


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.020MHz
Ch2+Ch3 Pha 44.51 °
24 Nov 2011 17:41:17


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 501mV
Ch2 Freq 3.042MHz
Ch2+Ch3 Pha 45.32 °
24 Nov 2011 17:43:42


Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.036MHz
Ch2+Ch3 Pha 45.45 °
24 Nov 2011 17:42:12

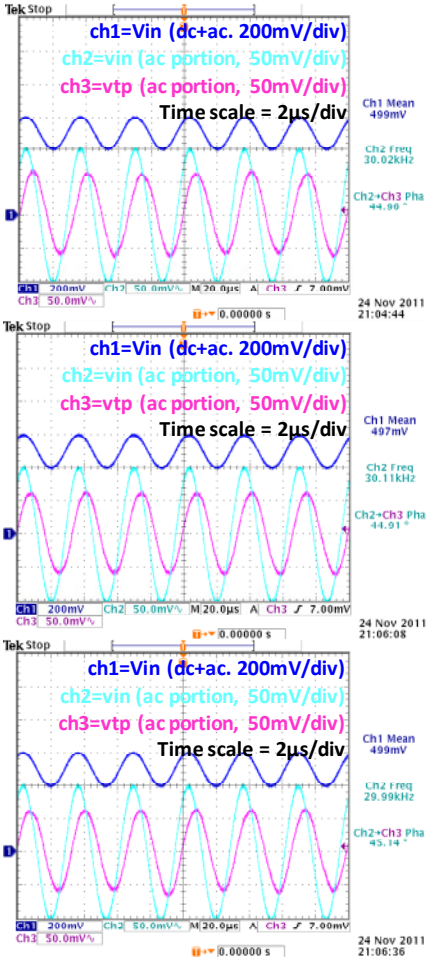

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 500mV
Ch2 Freq 3.038MHz
Ch2+Ch3 Pha 44.55 °
24 Nov 2011 17:42:30

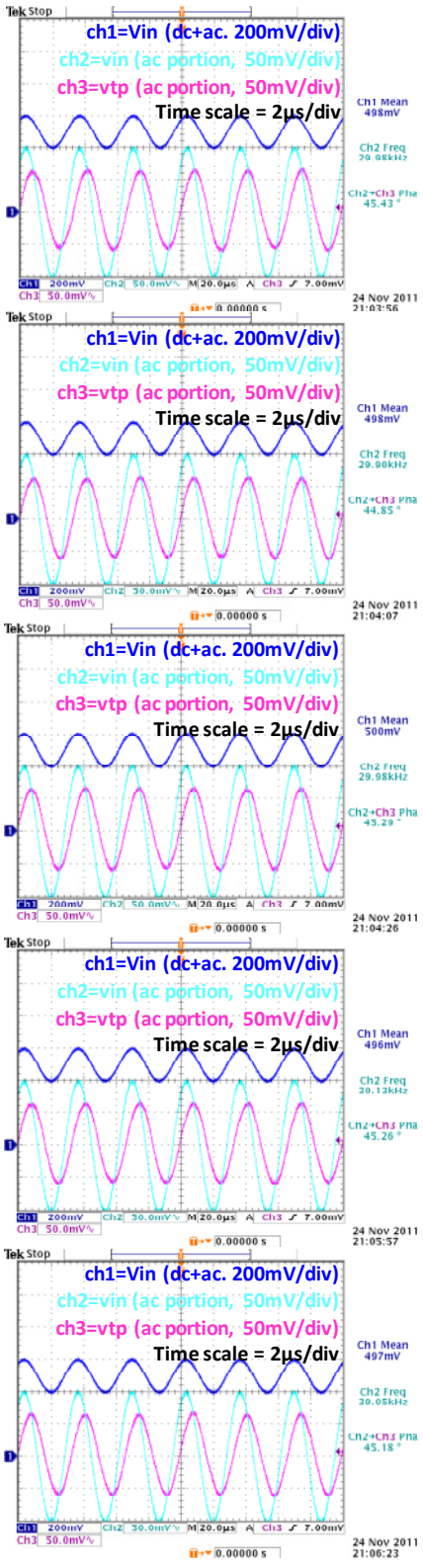

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 502mV
Ch2 Freq 3.021MHz
Ch2+Ch3 Pha 45.02 °
24 Nov 2011 17:43:02

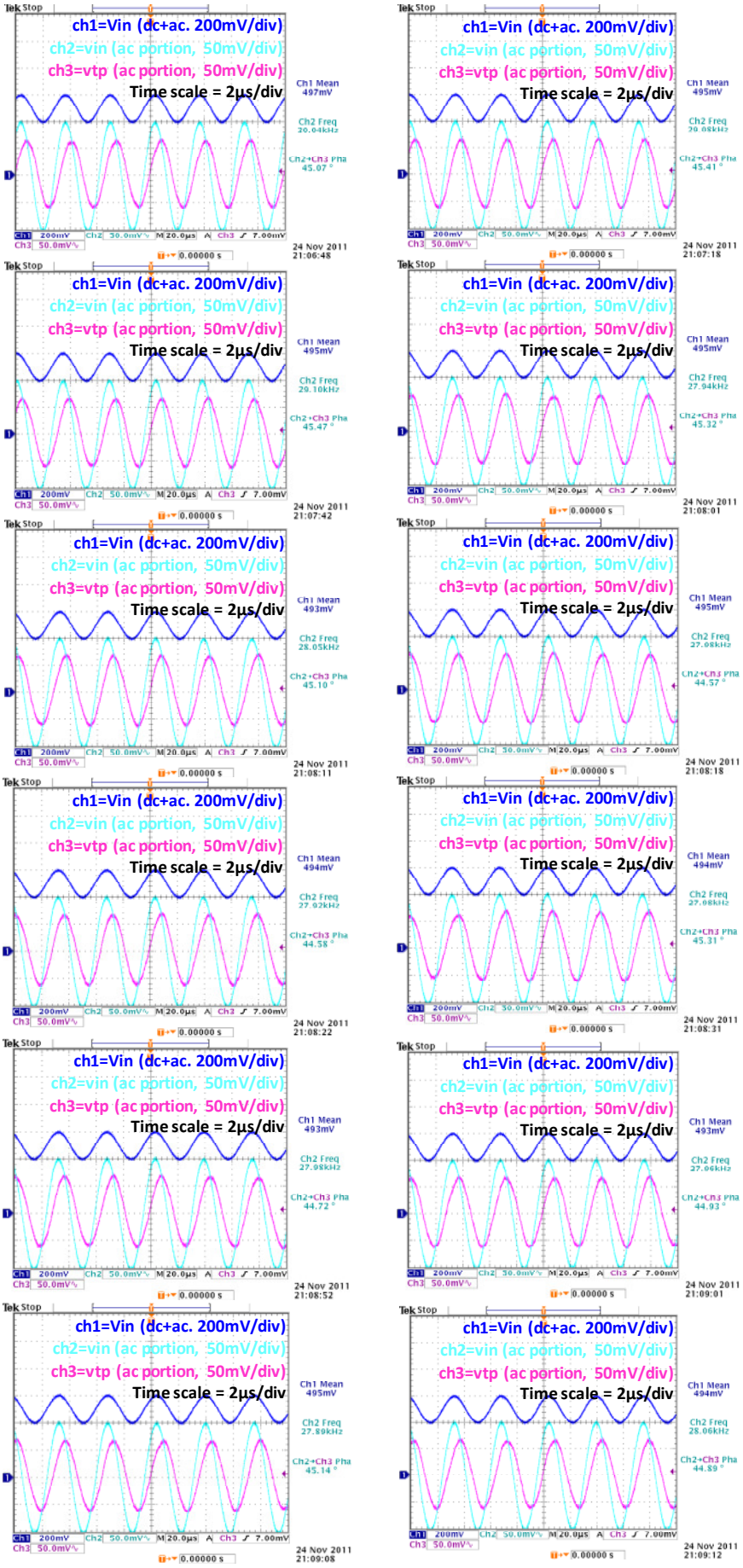
testsignal noQFG5 with 200mVpp 470k @0.5VDC

RIN= 4.715E+05

Sample No.	*phase*	*f*	*c*
1	45.43	2.998E+04	1.14E-11
2	44.85	2.990E+04	1.12E-11
3	45.29	2.998E+04	1.14E-11
4	44.96	3.002E+04	1.12E-11
5	45.26	3.013E+04	1.13E-11
6	44.91	3.011E+04	1.12E-11
7	45.18	3.005E+04	1.13E-11
8	45.14	2.999E+04	1.13E-11
9	45.07	3.004E+04	1.13E-11
10	45.41	2.908E+04	1.18E-11
11	45.47	2.910E+04	1.18E-11
12	45.32	2.794E+04	1.22E-11
13	45.10	2.805E+04	1.21E-11
14	44.57	2.798E+04	1.19E-11
15	44.58	2.792E+04	1.19E-11
16	45.31	2.798E+04	1.22E-11
17	44.72	2.798E+04	1.19E-11
18	44.93	2.796E+04	1.20E-11
19	45.14	2.789E+04	1.22E-11
20	44.89	2.806E+04	1.20E-11
Average	45.08	2.901E+04	**1.168E-11**
STD	0.27	9.992E+02	**3.815E-13**



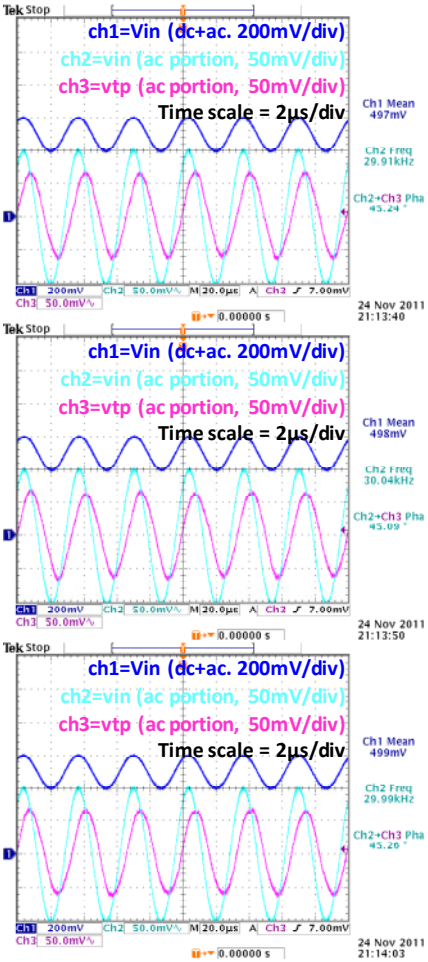


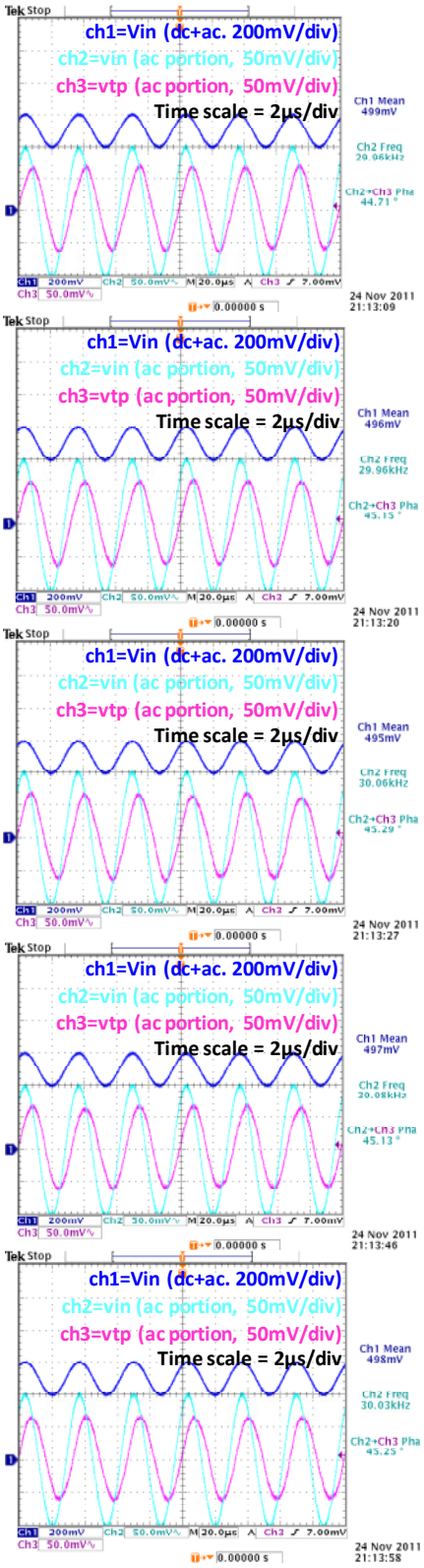

Tek Stop
ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div
Ch1 Mean 497mV
Ch2 Freq 30.04kHz
Ch2+Ch3 Pha 45.07 °
24 Nov 2011 21:06:48
Ch1 Mean 495mV
Ch2 Freq 30.08kHz
Ch2+Ch3 Pha 45.41 °
24 Nov 2011 21:07:18
Ch1 Mean 495mV
Ch2 Freq 29.10kHz
Ch2+Ch3 Pha 45.47 °
24 Nov 2011 21:07:42
Ch1 Mean 495mV
Ch2 Freq 27.94kHz
Ch2+Ch3 Pha 45.32 °
24 Nov 2011 21:08:01
Ch1 Mean 493mV
Ch2 Freq 28.05kHz
Ch2+Ch3 Pha 45.10 °
24 Nov 2011 21:08:11
Ch1 Mean 495mV
Ch2 Freq 27.08kHz
Ch2+Ch3 Pha 44.57 °
24 Nov 2011 21:08:18
Ch1 Mean 494mV
Ch2 Freq 27.92kHz
Ch2+Ch3 Pha 44.58 °
24 Nov 2011 21:08:22
Ch1 Mean 494mV
Ch2 Freq 27.08kHz
Ch2+Ch3 Pha 45.31 °
24 Nov 2011 21:08:31
Ch1 Mean 493mV
Ch2 Freq 27.98kHz
Ch2+Ch3 Pha 44.72 °
24 Nov 2011 21:08:52
Ch1 Mean 493mV
Ch2 Freq 27.06kHz
Ch2+Ch3 Pha 44.93 °
24 Nov 2011 21:09:01
Ch1 Mean 495mV
Ch2 Freq 27.89kHz
Ch2+Ch3 Pha 45.14 °
24 Nov 2011 21:09:08
Ch1 Mean 494mV
Ch2 Freq 28.06kHz
Ch2+Ch3 Pha 44.89 °
24 Nov 2011 21:09:12

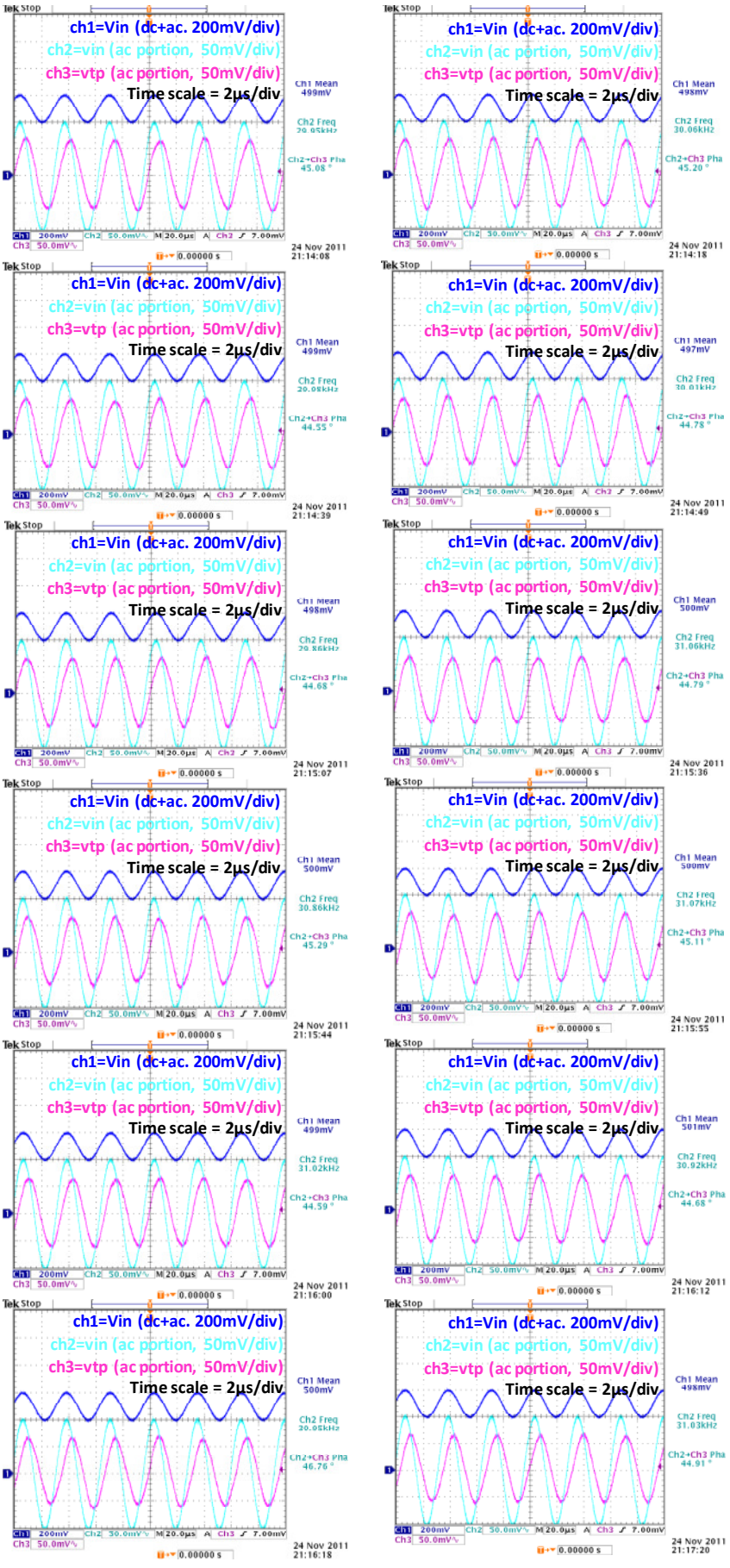
testsignal PADONLY with 200mVpp 470k @0.5VDC

RIN= 4.715E+05

Sample No.	*phase*	*f*	*c*
1	44.71	2.996E+04	1.12E-11
2	45.15	2.996E+04	1.13E-11
3	45.29	3.006E+04	1.13E-11
4	45.24	2.991E+04	1.14E-11
5	45.13	3.008E+04	1.13E-11
6	45.09	3.004E+04	1.13E-11
7	45.25	3.003E+04	1.13E-11
8	45.26	2.999E+04	1.14E-11
9	45.08	2.995E+04	1.13E-11
10	45.20	3.006E+04	1.13E-11
11	44.55	2.998E+04	1.11E-11
12	44.78	3.001E+04	1.12E-11
13	44.68	2.986E+04	1.12E-11
14	44.79	3.106E+04	1.08E-11
15	45.29	3.086E+04	1.10E-11
16	45.11	3.107E+04	1.09E-11
17	44.59	3.102E+04	1.07E-11
18	44.68	3.092E+04	1.08E-11
19	46.76	3.095E+04	1.16E-11
20	44.91	3.103E+04	1.08E-11
Average	45.08	3.034E+04	**1.116E-11**
STD	0.47	4.918E+02	**2.385E-13**






ch1=Vin (dc+ac. 200mV/div)
ch2=vin (ac portion, 50mV/div)
ch3=vtp (ac portion, 50mV/div)
Time scale = 2µs/div

References

References for Chapter 1

[ALL02] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford University Press, 2nd ed., 2002

[BLA98] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V opamps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[ITR10] International Technology Roadmap for Semiconductors (ITRS 2010), http://www.itrs.net/

[GRA01] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., Johnson Wiley and Sons, New York 2001

[LOP09] A. J. López-Martin, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient Class AB CMOS Buffer", *IEE J. Electronic Letters*, 2009, 45, (2), pp. 89–90

[MOR65] G. E. Moore, "Cramming More Components onto Integrated Circuits, Reprinted from Electronics, Volume 38, Number 8, April 19, 1965, pp.114 ff", *IEEE Solid-State Circuits Newsletter*, 2006, 20, (3), pp.33-35

References for Chapter 2

[ALL02] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford University Press, 2nd ed., 2002

[BLA96] B. J. Blalock and P.E. Allen, "A One-Volt, 120μW, 1-MHz OTA for Standard CMOS technology", *IEEE Proc. International Symposium on Circuits and Systems*, 1996, pp. 305 – 307

[BLA98] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V opamps using standard digital CMOS technology," *IEEE Tans.*

Circuits and Systems – II: Analog and Digital Signal Processing, pp. 769-780, vol. 45, no. 7, July 1998

[MOS11] The MOSIS service, http://www.mosis.net/

[SAN06] W. Sansen, Analog Design Essentials, Springer, 2006.

[SED11] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th ed., Oxford University Press, 2011

[YTT03] T. Ytterdal, Y. Cheng, T. A. Fjeldly, "Device modeling for analog and RF CMOS circuit design", Wiley, 2003

Reference for Chapter 3

[ALL02] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford University Press, 2nd ed., 2002

[BAH00] F. Bahmani, S. M. Fakhraie, and A. Khakifirooz, "A rail-to-rail, constant-gm, 1-volt CMOS opamp," *IEEE Proc. International Symposium on Circuits and Systems*, 2000, pp. 669 – 672

[BAK08] R. J. Baker, "CMOS Circuit Design, Layout and Simulation", revised 2nd ed., Wiley Interscience, 2008

[BIA99] M. Bialko, A. Guzinski, P. E. Allen, B. J. Blalock, and G. A. Rincon-Mora, "Comments on "Designing 1-V opamps using standard digital CMOS technology" and Reply", *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 1448, vol. 46, no. 11, November 1999

[BLA98] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V opamps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[BLA00] B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-driving as a low-voltage analog design technique for CMOS technology," *IEEE Southwest Symp. on Mixed-Signal Design*, *2000*, pp. 113-118, February 2000

[CAR03] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. of Solid-State Circuits*, vol. 38, no. 8, August 2003

[CAR05] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. on Circuits and Design I*, vol. 52, no. 7, pp. 1276 – 1291, July 2005

[DIE91] F. Dielacher, J. Hauptmann, J. Reisinger, R. Steiner, and H. Zojer, "A Software Programmable CMOS Telephone Circuit", *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp.1015-1026, July 1991

[GRA01] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., Johnson Wiley and Sons, New York 2001

[GUZ87] A. Guzinski, M. Bialko, and J. C. Matheau, "Body Driven Differential Amplifier for Application in Continuous Time Active-C Filter", *IEEE Proc. European Conference in Circuit Theory and Design*, 1987, pp. 315 – 320

[HAG06] Y. Haga, R. C. S. Morling, and I. Kale, "A New Bulk-Driven Input Stage Design for sub 1-volt CMOS Op-Amps", *IEEE Proc. International Symposium in Circuits and Systems*, 2006, pp. 1547 – 1550

[HAG09] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp. 2717 – 2720

[HAG10] Y. Haga and I. Kale, "Bulk-Driven Flipped Differential Pair", *IEEE Proc. PhD Research in Microelectronics and Electronics*, 2010

[HOG92] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-*gm* rail-to-rail input stage," *IEEE Proc. International Symposium in Circuits and Systems,* 1992, vol. 6, pp. 2876-2879

[JOH97] D. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, 1997

[LOP09] A. J. López-Martin, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient Class AB CMOS Buffer", *IEE J. Electronic Letters*, 2009, 45, (2), pp. 89 – 90

[RAZ01] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-

Hill, 2001

[SAN06] W. Sansen, "Analog Design Essentials", Springer, 2006.

[SED11] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th ed., Oxford University Press, 2011

[SON08] T. Song, J. Hu, X. Li, E. Sánchez-Sinencio, and S. Yan, "A Robust and Scalable Constant-gm Rail-to-Rail CMOS Input Stage with Dynamic Feedback for VLSI Cell Libraries", *IEEE Trans. Circuits and Systems – I: Regular Papers*, vol. 55, No. 3, April 2008

[WU94] W.-C. Wu, W. J. Helms, J. A. Kuhn, and B. E. Byrkett, "A digital process compatible high-drive CMOS op amp with tail-to-rail input and output ranges," *IEEE J. on Solid-State Circuits*, vol. 29, no. 1, pp. 63 – 66, January 1994

[YAN00] S. Yan and E. Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial", *IEICE Trans. Analog Integrated Circuits and Systems*, vol. E00–A, no.2, pp. 179 – 196, February 2000

References for Chapter 4

[ALL02] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford University Press, 2nd ed., 2002

[BAK08] R. J. Baker, "CMOS Circuit Design, Layout and Simulation", revised 2nd ed., Wiley Interscience, 2008

[BAN88] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully Differential Operational Amplifiers with Accurate Output Balancing", *IEEE J. Solid-State Circuits,* vol.23, issue 6, pp. 1410 – 1414, December 1988

[BLA96] B. J. Blalock and P.E. Allen, "A One-Volt, 120μW, 1-MHz OTA for Standard CMOS technology", *IEEE Proc. International Symposium in Circuits and Systems*, 1996, pp. 305 – 307

[BLA98] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V opamps using standard digital CMOS technology," *IEEE Trans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[BLA00] B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-driving as a low-voltage analog design technique for CMOS technology," *IEEE Proc. Southwest Symp. on Mixed-Signal Design*, 2000, pp. 113-

118, February 2000

[CAR03] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. of Solid-State Circuits*, vol. 38, no. 8, August 2003

[CAR05] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. on Circuits and Design I*, vol 52, no. 7, pp. 1276 – 1291, July 2005

[FAN05] Z. Fan and P. K. Chan, "Analysis and Design of Low-Distortion CMOS Source Followers", *IEEE Tran. on Circuits and Systems—I: Regular Papers*, vol. 52, no. 8, August 2005

[GRA01] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., Johnson Wiley and Sons, New York 2001

[HAG08] Y. Haga and I. Kale, "Achieving Rail-to-Rail Input Operation using Level-Shift Multiplexing Technique for All CMOS Op-Amps", *IEEE Proc. Midwest Symposium in Circuits and Systems*, August 2008, pp. 698 – 701

[HAG09A] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp. 2717 – 2720

[HAG09B] Y. Haga and I. Kale, "Class-AB Rail-to-Rail CMOS Buffer with Bulk-Driven Super Source Followers", *IEEE European Conference on Circuit Theory and Design*, 2009, pp. 695 – 698

[HOG92] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-*gm* rail-to-rail input stage," *IEEE Proc. International Symposium in Circuits and Systems*, 1992, vol. 6, pp. 2876 – 2879

[JOH97] D. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, 1997

[LOP09] A. J. López-Martin, J. Ramírez-Angulo, R. G. Carvajal, and L. Acosta, "Power-efficient Class AB CMOS Buffer", *IEE J. Electronic*

Letters, 2009, 45, (2), pp. 89 – 90

[MAN08] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE trans on Circuits and Design I*, pp. 1392 – 1401, Vol 55, No. 5, June 2008

[PAD06] I. Padilla, J. Ramirez-Angulo, R. G. Carvajal, A. J. Lopez-Martin, A. Carlosena, "Compact implementation of linear weighted CMOS transconductance adder based on the flipped voltage follower," *IEEE proc. International Symposium in Circuits and Systems,* 2006, pp. 4281 – 4284, May 2006

[PAD07] I. Padilla-Cantoya, J. E. Molinar-Solis, G. O. Ducoudary, "Class AB Low-Voltage CMOS Voltage Follower," *IEEE Proc. Midwest Symposium in Circuits and Systems*, 2007, pp. 887 – 890, August 2007

[RAJ02] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques", *IEEE Circuits and Systems Magazine*, 2002, issue 1, vol.2, pp. 24 – 42

[RAM94] J. Ramírez-Angulo, "Low voltage current mirrors for built-in current sensors", *IEEE proc. International Symposium in Circuits and Systems*, 1994, pp. 529 – 532

[RAM04] J. Ramírez-Angulo, A. J. López-Martin, R. G. Carvajal, and F. M. Chavero, "Very Low-Voltage Analog Signal Processing Based on Quasi-Floating Gate Transistors", *IEEE J. Solid-State Circuits*, 2004, 39, (3), pp. 434 – 442

[RAM06] J. Ramirez-Angulo, S. Gupta, R. G. Carvajal, A. J. Lopez-Martin, "New Improved CMOS Class AB Buffers Based on Differential Flipped Voltage Followers," *IEEE proc. International Symposium in Circuits and Systems*, 2006, pp. 3914 – 3917

[RAZ01] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001

[SAN06] W. Sansen, "Analog Design Essentials", Springer, 2006.

[SED11] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th ed., Oxford University Press, 2011

[SHE09] P. Sheng-Wen, C. Chiung-Cheng, Y. Chung-Huang, and Yu-Sheng Lai, "A Novel OTA with Dual Bulk-driven Input Stage", *IEEE Proc. International Symposium in Circuits and Systems*, 2009, pp. 2721 –

2723

[TSI76] Y. P. Tsividis and P. R. Gray, "An Integrated NMOS Operational Amplifier with Internal Compensation", *IEEE J. Solid-State Circuits*, Vol. SC-11, No. 6, pp. 748 – 753, December 1976

References for Chapter 5

[ALL02] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," Oxford University Press, 2nd ed., 2002

[BAK08] R. J. Baker, "CMOS Circuit Design, Layout and Simulation", revised 2nd ed., Wiley Interscience, 2008

[BLA95] B. J. Blalock and P. E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology", *IEEE Proc. International Symposium on Circuits and Systems*,1995, pp.1972 – 1975

[BLA96] B. J. Blalock and P.E. Allen, "A One-Volt, 120μW, 1-MHz OTA for Standard CMOS technology", *IEEE Proc. International Symposium on Circuits and Systems*, 1996, pp. 305 – 307

[BUL90] "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain", *IEEE J. Solid-State Circuits*, 1990, Vol.25, Issue 6, pp. 1379 – 1384

[DON02] Z. Dong and P. E. Allen, "Low-Voltage, Supply Independent CMOS Bias Circuit," *The 2002 45th Midwest Symp. on Circuits and Systems*, 2002, Vol. 3, pp. 568 – 570

[GRA01] P. R. Gray, P. J. Hurst, H. Lewis, and R. G. Mayer, "Analysis and Design of Analog Integrated Circuits", 4th ed., Johnson Wiley and Sons, New York 2001

[HOG92] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS Low-Voltage Operational Amplifiers with Constant-*gm* Rail-to-Rail Input Stage," *IEEE Proc. International Symposium on Circuits and Systems*, 1992, pp. 2876 – 2879

[HOS79] B. J. Hosticka, "Improvement of the Gain of MOS Amplifiers", *IEEE J. Solid-State Circuits*, 1979, Vol.14, Issue 6, pp. 1111 – 1114

[JOH97] D. Johns and K. Martin, "Analog Integrated Circuit Design", Wiley, 1997

[RAJ02] S. S. Rajput and S. S. Jamuar, "Low Voltage Analog Circuit Design

Techniques", *IEEE Circuits and Systems Magazine*, 2002, issue 1, vol.2, pp. 24 – 42

[RAZ01] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001

[ROS03] J. Rosenfeld, M. Kozak, and E.G. Friedman, " A 0.8 Volt High Performance OTA Using Bulk-Driven MOSFETs for Low Power Mixed-Signal SOCs", *SOC Conference, 2003 Proceedings, IEEE International [Systems-on-Chip]*, pp. 245 – 246, 17-20 September 2003

[ROS04] J. Rosenfeld, M. Kozak, and E.G. Friedman, " A Bulk-driven CMOS OTA with 68dB gain", *IEEE Proc. International Conference on Electronics, Circuits and Systems*, 2004, pp. 5 – 8

[SAC90] E. Säckinger and W. Guggenbühl, W "A high-swing, high-impedance MOS cascode circuit", *IEEE J. Solid-State Circuits*, 1979, Vol.25, Issue 1, pp. 289 – 298

[SAN06] W. Sansen*, "Analog Design Essentials"*, Springer, 2006.

[SED11] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th ed., Oxford University Press, 2011

[TER02] S. Terry, B. J. Blalock, L. Yong, B. Dufrene, and M. Mojarradi, "Complementary body driving - a low voltage analog circuit technique for SOI", *IEEE Proc. International SOC Conference*, 2002, pp. 80 – 82

[WU94] W.-C. Wu, W. J. Helms, J. A. Kuhn, and B. E. Byrkett, "A digital process compatible high-drive CMOS op amp with tail-to-rail input and output ranges," *IEEE J. on Solid-State Circuits*, vol. 29, no. 1, pp. 63-66, January 1994

[ZAB07] S. A. Zabihian and R. Lotfi, "Ultra-low-voltage, low-power, high-speed operational amplifiers using body-driven gain boosting technique", *IEEE Proc. International Symposium on Circuits and Systems*, 2007, pp. 705 – 708

References for Chapter 6

[ALL02] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford

University Press, 2nd ed., 2002

[BAK11] http://cmosedu.com/

[ELE11] http://www.staticfreesoft.com/

[ENZ95] C.C. Enz, F. Krummenacher, and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", *J. Analog Integrated Circuits and Signal Processing*, 1995, 8, pp. 83 – 114, Kluwer Academic Publishers

[EUR10] Annual Report 2010, http://www.europractice-ic.com/

[HE08] R. He and L. Zhang, "Evaluation of Modern MOSFET models for Bulk-Driven Applications", *IEEE Proc. Midwest Symposium in Circuits and Systems*, 2008, pp.105 – 108

[NAT90] S. Natarajan, and B.K. Herman, "Measurement of Small Capacitances using Phase Measurement", *IEEE Proc. Twenty-Second Southeastern Symposium on System Theory*, 1990, pp.46 – 50

[RAM04] J. Ramírez-Angulo, A. J. López-Martin, R. G. Carvajal, and F. M. Chavero, "Very Low-Voltage Analog Signal Processing Based on Quasi-Floating Gate Transistors", *IEEE J. Solid-State Circuits*, 2004, 39, (3), pp. 434–442

[SAN98] W. Sansen, M. Steyaert, V. Peluso, and E. Peeters, "Toward Sub 1V Analog Integrated Circuits in Submicron Standard CMOS Technologies", *IEEE International Solid-State Circuits Conference*, 1998, pp. 186 – 187

[SAN06] W. Sansen, *"Analog Design Essentials"*, Springer, 2006

[SED11] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th ed., Oxford University Press, 2011

[TEK_1] Tektronix, “Instructions P6139A 10X Passive Probe 063-0870-05”

[TEK_2] Tektronix, “User Manual TDS3000 Series Digital Phosphor Oscilloscopes 071-0274-01”

[TEK_3] Tektronix, “ABCs of Probes Primer”, http://www.tek.com

[TER03] S. C. Terry, J. M. Rochelle, D. M. Binkley, B. J. Blalock, D. P. Foty, and M. Bucher, “Comparison of a BSIM3V3 and EKV MOSFET Model for 0.5µm CMOS Process and Implications for Analog Circuit Design”, *IEEE Trans. Nuclear Science*, pp. 915 – 920, vol. 50, no. 4, 2003

[WAN09] S. Wang, R. He, and L. Zhang, “MOSFET Model Assessment for Submicron and Nanometer Bulk-Driven Applications”, *IEEE Proc. Canadian Conference on Electrical and Computer Engineering*, 2009, pp. 1091 – 1094

[WAN10] S. Wang, “Nanometer Bulk-Driven Applications MOSFET Model Analysis”, *IEEE Proc. International Conference on Computer Design and Automation*, 2010, pp. V4-197 – V4-200

References for Chapter 7

[BLA95] B. J. Blalock and P. E. Allen, “A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology”, *IEEE Proc. International Symposium on Circuits and Systems*,1995, pp.1972 – 1975

[CAR05] J. M. Carrillo, R. Pérez-Aloe, J. M. Valverde, and J. F. Duque-Carrillo, “1-V Rail-to-Rail Bulk-Driven CMOS OTA With Enhanced Gain and Gain-Bandwidth Product”, *IEEE Proc. European Conference on Circuits Theory and Design*, 2005, pp. I/261 – I/264

[HSI10] L. Chun-Hsing Li and K. Chien-Nan, “Design Optimization of a 1.4 GHz Low Power Bulk-Driven mixer”, *IEEE Proc. Asia-Pacific Microwave Conference*, 2010, pp. 1035 – 1038

[KHA06] A. Khateb, D. Biolek, and K. Novacek, "On the Design of Low-Voltage Low-power Bulk-driven CMOS Current Conveyors", *IEEE Proc. International Spring Seminar on Electronics Technology*, 2006, pp. 318 – 216

[KHA11A] F. Khateb and N. Khatib, "New bulk-driven class AB CCII", *IEEE Proc. International Conference on Radioelektronika*, 2011, pp. 1 – 4

[LAK11] N. Lakkamraju and A. K. Mal, "A low voltage high output impedance bulk driven regulated cascode current mirror", *IEEE Proc. International Conference on Electronics Computer Technology*, 2011, Vol.3, pp. 79-83

[LUN09] L. Yu-Lung, Y. Wei-Bin, C. Ting-Sheng, and C. Kuo-Hsing, "Designing an Ultralow-Voltage Phase-Locked Loop Using a Bulk-Driven Technique", *IEEE Tran. on Circuits and Systems II: Express Briefs*, vol.56, issue 5, 2009

[MON09] P. Monsurr, S. Pennisi, G. Scotti, and Alessandro Trifiletti, "0.9-V CMOS cascode amplifier with body-driven gain boosting", International Journal of Circuit Theory and Applications, 2009, 37, pp. 193 – 202, Wiley Online Library

[RAI10A] G. Raikos and S. Vlassis, "0.8V bulk-driven variable gain amplifier", *IEEE Proc. International Conference on Electronics, Circuits, and Systems*, 2010, pp. 347 – 350

[RAI10B] G. Raikos and S. Vlassis, "Low-voltage CMOS voltage squarer" *IEEE Proc. International Conference on Electronics, Circuits, and Systems*, 2010, pp. 159 – 162

[RAI10C] G. Raikos and S. Vlassis, "0.8 V Bulk-Driven Operational Amplifier", *Analog Integrated Circuits and Signal Processing*, 2010, 63, pp. 425 – 432, Springer

[SCH08] O. Schmitz, S. K Hampel, C. Orlob, M. Tiebout, and I. Rolfes, "Low-Voltage Bulk-Driven Mixers in 45nm CMOS for Ultra-Wideband TX and RX", *IEEE Proc. Norchip Conference*, 2008, pp. 119 – 122

[VOR08] D. Van Vorst, and S. Mirabbasi, "Low-Power 1V 5.8 GHz Bulk-Driven Mixer with On-Chip Balun in 0.18μm CMOS", *IEEE Proc. Radio Frequency Integrated Circuits Symposium*, 2008, pp. 197 – 200

[ZAB07] S. A. Zabihian, and R. Lotfi, "Ultra-Low-Voltage, Low-Power, High-Speed Operational Amplifiers Using Body-Driven Gain-Boosting

Technique", *IEEE Proc. International Symposium on Circuits and Systems*, 2007, pp. 705 – 708

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