A subsampling delta-sigma modulator for global navigation satellite systems

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A SUBSAMPLING DELTA-SIGMA MODULATOR FOR GLOBAL NAVIGATION SATELLITE SYSTEMS

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A Thesis Submitted in Partial Fulfilment of Requirements of the University of Westminster for the Degree of Doctor of Philosophy

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I hereby certify that the research work presented in this thesis is, to the best of my knowledge and belief, original except as referenced in the thesis. I hereby declare that I have not submitted this material, either completely or in part, for a degree at this or any other institution.

Science is the true mentor for civilization, for life, for success in the world.

M. Kemal Ataturk

Anneme

To my mother

Abstract

Next-generation Global Navigation Satellite Systems (GNSS) receivers should be capable of processing multi-frequency signals in order to provide better positioning accuracy and signal availability to end-user. Nevertheless, the realization of such receivers with conventional receiver architectures leads to power-hungry devices and hinders monolithic integration of the receiver. Multi–frequency receivers can be realized with lower power and cost by performing sub-Nyquist sampling (subsampling) at Radio Frequency (RF). In practice, the use of subsampling receivers has been limited due to their poor noise performance. This is particularly a concern in applications of Code Division Multiple Access (CDMA) such as GNSS since subsampling may saturate the Analog-to-Digital Converter (ADC) as the thermal noise floor is above the signals of interest. Continuous-Time (CT) Delta-Sigma ($\Delta\Sigma$) modulation is an attractive candidate for subsampling Analog-to-Digital (A/D) conversion as it provides noise-shaping and inherent Anti-Alias (AA) filtering. However, the attenuation of the RF alias in the feedback path of the modulator and the reduction of the effective Quality (Q-factor) of the loop filter prevent conventional CT-$\Delta\Sigma$ modulators to be utilized in subsampling receivers. This thesis proposes a novel CT-$\Delta\Sigma$ modulator at both the system and the circuit level that is capable of compensating for the effects of subsampling. These are achieved by modifying the feedback path of the conventional modulator architecture to accommodate for the RF alias and by enhancing the Q-factor of the loop filter. The proposed CT-$\Delta\Sigma$ has significant improvements over previously published subsampling modulators as it provides jitter and alias suppression and excess loop delay compensation to improve the dynamic range, thus enabling the modulator to be utilized in subsampling receivers when a relatively low sampling rate is desired. Based on the novel CT-$\Delta\Sigma$ modulator, this thesis also proposes a subsampling receiver architecture for multi-constellation GNSS applications. Simulations results indicate that the proposed receiver architecture can successfully acquire and track the civilian radionavigation signals with a high performance.

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Abbreviations

AA	Anti-Alias
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
bps	bits per second
c	Speed of Light
C/N_0	Carrier to Noise Density
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
$\Delta\Sigma$	Delta-Sigma
D/A	Digital-to-Analog
DAC	Digital-to-Analog Converter
DLL	Delayed Lock Loop
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete Time
ELD	Excess Loop Delay
FET	Field Effect Transistor
FIR	Finite Impulse Response
GaAs	Gallium Arsenide
GIOVE	Galileo In Orbit Validation Element

GLONASS	GLObalnaya Navigatsionnaya Sputnikovaya Sistema
GNSS	Global Navigation Satellite Systems
GPS	Global Positioning System
Hz	Hertz
IC	Integrated Circuit
IIT	Impulse-Invariant Transform
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
NF	Noise Figure
NMOS	N-channel MOS
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
P1dB	Output Power at 1-dB Compression Point
PDF	Probability Distribution Function
PDK	Process Design Kit
PLL	Phased Locked Loop
PMOS	P-channel MOS
PSD	Power Spectral Density

RF	Radio Frequency
RHP	Right Half Plane
S/H	Sample-and-Hold
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
STF	Signal Transfer Function
THD	Total Harmonic Distortion

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Chapter 1

Introduction

1.1 Motivation

The modernization plans for the United States (US) Navstar Global Positioning System (GPS) and the Russian GLObal'naya NAvigatsionnaya Sputnikovaya Sistema (GLONASS) as well as the upcoming satellite navigation systems, Galileo and Compass, catalyzes the research activity for the design and implementation of multi-constellation GNSS receivers [Ako03], [Jin05], [Psi05], [Det08], [Noo08]. The new radionavigation signals will provide better positioning accuracy and robustness against the effects of multipath and interference. The availability of multi-frequency radionavigation signals will enhance signal reception and provide ionosphere estimation capabilities that would enable to eliminate one of the biggest error sources in radionavigation [Ako03].

The integration of wireless communication standards such as Global System for Mobile communications (GSM), Universal Mobile Telecommunications System (UMTS), and IEEE 802.11 Wireless Local Area Network (WLAN), with GPS onto a single radio receiver to provide Location-Based Services (LBS) have become a practical reality in the last decade. The market research company iSuppli forecasts that more than 80% of the mobile phones will provide LBS by 2012 [url01]. According to the GNSS market monitoring report published by the European GNSS Agency (GSA), it is estimated that the GNSS market size will be €244 billion in 2020 [url02]. The biggest share for the GNSS market is the personal navigation, i.e. automotive and mobile applications. Therefore, the two foremost prerequisites for a GNSS receiver for consumer market applications are low-power dissipation and low-cost.

Next generation GNSS-enabled radio receivers should be able to tune into the radionavigation band of interest to comply with the modulation standard as and when desired to benefit from the advantages of multi-constellation GNSS. This could be achieved by means of the Software Defined Radio (SDR) approach [Mit95], [Jon05] where the receiver is capable of tuning into any frequency band and receiving any modulation across a large frequency spectrum by means of programmable hardware, which is controlled by software. Nevertheless, realization of such receivers with conventional receiver architectures puts stringent requirements on either the RF front-end or the ADC. Multi-constellation capability in a GNSS receiver can be achieved with lower power and cost by performing subsampling at RF [Vau91]. This enables to shift of the Intermediate Frequency (IF) processing stage into the digital domain thereby eliminating the need for analog mixers, Image Rejection Filters (IRF), and RF frequency synthesisers paving the way for low-power and low-cost on-chip solutions. The RF front-end of such a receiver is the simplest architecture among the receiver front–end's which would be feasible to implement with today's Integrated Circuit (IC) technologies.

Despite the advantages, the use of subsampling receivers has been limited due to the Signal-to-Noise Ratio (SNR) degradation of the sampled signal as a result of noise aliasing. This reduces the Dynamic Range (DR) of

the ADC and may cause saturation in a GNSS receiver since the thermal noise floor is approximately 30dB above the radionavigation signals at the input of the ADC.

Traditionally, ΔΣ modulators have been utilized for narrowband A/D conversion; however, employing CT-ΔΣ ADCs could actually be a feasible option for subsampling A/D conversion. The wideband noise introduced during sampling can be shaped away with a CT-ΔΣ modulator as the sampling is performed inside the feedback loop of the modulator. Additionally, CT-ΔΣ modulators provide inherent AA filtering on the input signal path at no additional cost, which is essential in subsampling [Can85], [Vau91]. Despite these benefits, conventional CT-ΔΣ modulators are not suitable for subsampling A/D conversion due to two undesirable phenomena [Gou94], [Yua05]:

- The attenuation of the RF alias of the feedback signal in the sampled signal spectrum
- The reduction in the effective Q-factor of the loop filter of the modulator

The next section highlights the original contributions by the author to compensate for these issues, which forms the basis of the thesis.

1.2 Original Contributions

The main contributions resulting from this research can be summarized as below:

- This work proposes a novel subsampling CT-ΔΣ modulator by altering the feedback loop of the conventional modulator and by proposing a circuit architecture for the novel modulator to compensate for the issues associated with subsampling. System and transistor-level design for the novel CT-ΔΣ modulator is presented in Chapter 5. Based on [Xin05], a low-complexity Q and centre frequency tuning circuit for the modulator's loop filter is also proposed in this chapter.

- This work proposes a novel subsampling receiver architecture for multi-constellation GNSS applications, which aims to move the ADC as close to antenna as possible in an effort to minimize the number of analog components in the receiver. The novel subsampling CT-ΔΣ modulator is the core component of this receiver architecture. The simulation results for the subsampling GNSS receiver are presented in Chapter 6.

- A parametrizable MATLAB/SIMULINK GNSS toolbox was developed and used to evaluate the performance of the proposed receiver architecture. The toolbox comprises a complete transmission model for GPS L1/L2C/L5 and Galileo E1/E5/E6 signals as well as the fixed-point implementation of the Digital Signal Processor (DSP).

1.3 Author's Publications

- Ucar, A.; Cetin, E.; Kale, I.; "A Subsampling Continuous-Time Delta-Sigma Modulator for RF Subsampling Receivers", IEEE Transactions on Circuits and Systems II: Express Briefs, Accepted for Publication
- Ucar, A.; Cetin, E.; Kale, I.; "A Subsampling Receiver for Global Navigation Satellite Systems", Submitted to GPS Solutions: The Journal of Global Navigation Satellite Systems
- Ucar, A.; Cetin, E.; Kale, I.; "The Effect of Clock Jitter on the on the Performance of Continuous-Time Delta-Sigma ADC for GNSS Signals", Proceedings of the European Navigation Conference on Global Navigation Satellite Systems (ENC-GNSS) 2009, 3-6 May 2009, Naples, Italy
- Ucar, A.; Cetin, E.; Kale, I.; "On the Implications of Analog-to-Digital Conversion on Variable-Rate Bandpass Sampling GNSS Receivers", Proceedings of the Forty-second Asilomar Conference on Signals Systems and Computers, Pacific Grove, CA, USA, 26-29 Oct 2008

- Kazazoglu, R.; Ucar, A.; Cetin, E.; Kale, I.; "Weak Signal & Multipath Analysis Using GNSScope: A Toolbox for End-to-End Modelling, Simulation and Analysis of GNSS", Proceedings of the Navigation Conference & Exhibition (NAV08/ILA37): Navigation and Location, London, UK, 28 - 30 Oct 2008
- Ucar, A.; Cetin, E.; Kale, I.; "A Low Complexity DSP Driven Analog Impairment Mitigation Scheme for Low-IF GNSS Receivers", Proceedings of the IEEE/ION Position, Location and Navigation Symposium 2008, Monterey, CA, USA, 5-8 May 2008

1.4 Author's Abstracts and Invited Talks

- Ucar, A.; Cetin, E.; Kale, I.; "A Bandpass Sampling Receiver for Multi-Constellation GNSS", School of Electronics and Computer Science Research Conference, University of Westminster, London, UK, 3-6 Jul 2010 (Best Presentation Award)
- Ucar, A.; Cetin, E.; Kale, I.; "A Bandpass Sampling Receiver for GNSS Applications", New Navigators Seminar 2010, Imperial College, London, UK, 16 Jun 2010
- Ucar, A.; Kazazoglu, R.; Cetin, E.; Kale, I.; "GNSScope: Overview of a Toolbox for End-to-End Modelling, Simulation and Analysis of GNSS", New Navigators Seminar 2008, Imperial College, London, UK, 18 Jun 2008

1.5 Thesis Organization

Chapter 2 provides detailed information on GPS and Galileo signal structure. Spectral characteristics of the spreading code sequences and the modulation schemes for each radionavigation band are given in this chapter. Moreover, this chapter briefly explains how the new signals will provide better position accuracy and robustness against multipath and interference.

Chapter 3 discusses the design considerations of a multi-constellation GNSS receiver. An overview of a typical GNSS receiver from the antenna to the tracking loops is provided. This is followed by a discussion on conventional RF front-end topologies and subsampling receivers. This chapter is concluded with an analysis on the issues associated with the subsampling receiver.

Chapter 4 is intended to provide the reader an overview of ΔΣ modulators with an emphasis on theory and practical implementations of high-speed CT-ΔΣ modulators.

Chapter 5 introduces the novel subsampling CT-ΔΣ modulator. A system-level design methodology for the novel modulator presented. This is followed by the transistor-level design of the modulator using TSMC 90nm RF Process Design Kit (PDK). Furthermore, a low-complexity Q and centre frequency tuning circuit for modulator's Q-enhanced LC filters is proposed. Chapter 5 also provides a detailed performance evaluation of novel modulator.

Chapter 6 introduces the novel subsampling receiver architecture for multi-constellation GNSS applications. A design procedure for the receiver is presented followed by the MATLAB/SIMULINK – CADENCE co-simulation of the receiver chain to demonstrate the successful acquisition and tracking of the civilian radionavigation signals.

Chapter 7 presents a summary of the thesis, conclusions drawn from this research, and comments on the future research directions.

Chapter 2

GNSS Signal Characteristics

There has been an increasing demand for satellite navigation products and services within the wireless mass-market in the last decade. At the time of writing, GPS and GLONASS are the two fully operational satellite navigation systems offering global coverage with at least 24 satellites in orbit. Galileo, which currently being built by the European Space Agency (ESA), is scheduled to provide global coverage in 2014 [url03]. The People's Republic of China has been expanding its regional Beidou-1 satellite navigation system into Beidou-2 (also known as Compass) with the aim of offering global coverage with 35 satellites by 2020 [url04].

GPS, GLONASS, and Galileo incorporate both open and restricted access radionavigation signals. The frequency allocation for GPS and Galileo is depicted in Figure 2-1 [Nav06], [Esa09]. The frequency bands that fall in the Aeronautical Radio Navigation System (ARNS) band are more robust to interference since no other users of this band is permitted to interfere with the signals [Mis06]. As can be observed in Figure 2-1, there is a spectral overlap between L1-E1 and L5-E5a. This significantly simplifies receiver design at the expense of introducing inter-system interference, which degrades the Carrier-to-Noise density (C/N_0)[†]. In 2004, the US and the European Union (EU) reached an agreement to minimize the inter-system interference between GPS and Galileo signals by introducing the split-spectrum Binary Offset Carrier (BOC) modulation [url05]. The studies have shown that the C/N_0 degradation of GPS L1 signal due to BOC modulated Galileo E1 signal never exceeds 0.2dB [Pra03]. The C/N_0 degradation of GPS L5 signal code due to Galileo E5a is between 0.2 to 0.4 dB; and the C/N_0 degradation of Galileo E5a due to GPS L5 is between 0.5 to 0.8dB. The slightly higher figures can be explained by the use of similar modulation schemes in E5a and L5.

2.1 Spreading Code Sequences

GPS and Galileo utilize a spread-spectrum technique called Code Division Multiple Access (CDMA). Spread-spectrum is so called since the bandwidth of the transmitted signal is considerably wider than the information bandwidth in order to provide secure communications and robustness against interference and jamming [Pet95]. Each satellite transmitting a particular radionavigation signal share a common carrier frequency but consists of a unique spreading code, which enables the receiver to distinguish one satellite from the other. Spreading code sequences utilized in GPS and Galileo belong to a family of sequences referred to as Gold codes [Gol67]. A Gold code sequence is the sum of two binary Maximum-Length Sequences (MLS). MLS are generated using maximal Linear Feedback Shift Registers (LFSR) with proper feedback and it

[†] C/N_0 [dB/Hz] is the Signal-to-Noise Ratio (SNR) referenced to 1Hz

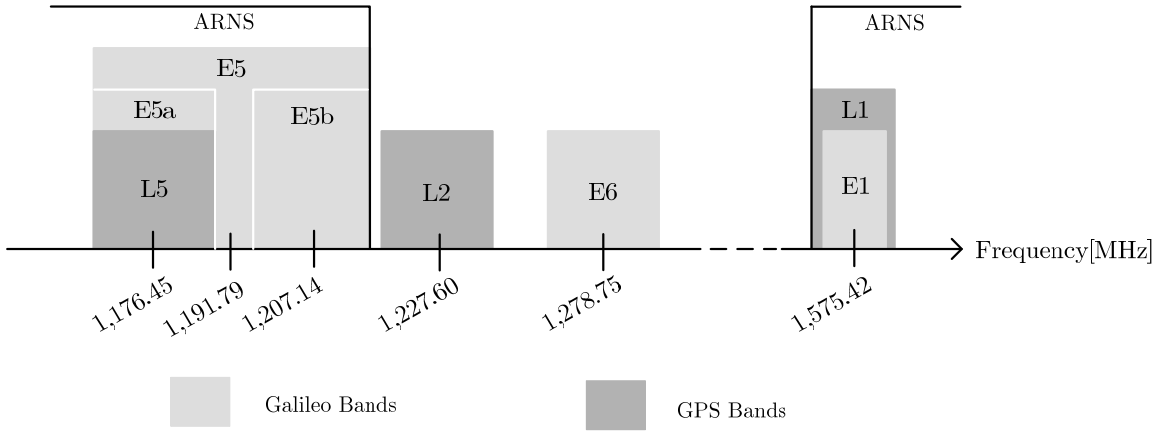


Figure 2-1 Frequency allocation of the GPS and Galileo signals

is so called since an L-tap maximal LFSR can generate a non-repeating sequence of length $N=2^L-1$. As MLS are periodic and consist of deterministic sequence of pulses, they are also referred to as PseudoRandom Noise (PRN) sequences. If PRN sequences were of infinite length, they would result in orthogonal code sequences with zero cross-correlation and zero auto-correlation except for the zero lag.

A pseudo-random binary sequence of rectangular pulses with amplitude ±1 and pulse duration T has the autocorrelation function [Hay01]:

$$R_{xx}(\tau)=\begin{cases}\left(1-\dfrac{|\tau|}{T}\right), & |\tau|<T\\ 0, \text{ otherwise}\end{cases} \tag{2.1}$$

As can be observed in Figure 2-2, there is no correlation outside the correlation interval $\{-T,T\}$. According to the Wiener–Khinchin theorem, the Power Spectral Density (PSD) of a random stationary process can be determined by taking the Fourier transform of its autocorrelation function [Lee98a]:

$$S_x(f)\triangleq\int_{-T}^{T}R_{xx}(\tau)e^{-j2\pi f\tau}d\tau \tag{2.2}$$

The PSD of the random binary process can be derived from its autocorrelation function as:

$$S_x(f) = \int_{-T}^{T} \left(1 - \frac{|\tau|}{T}\right) e^{-j2\pi f\tau} d\tau = T\,\mathrm{sinc}^2\left(fT\right) \tag{2.3}$$

where

$$\mathrm{sinc}\left(x\right) \triangleq \frac{\sin\left(\pi x\right)}{\pi x} \tag{2.4}$$

The power spectrum of the random process has a sinc-squared envelope and a null-to-null bandwidth of $2/T$ as plotted in Figure 2-3. For a MLS code sequence of length N, the correlation value outside the correlation interval is $-1/N$, as illustrated in Figure 2-4. The autocorrelation function of a MLS code sequence can be formulated as [Hol90]:

$$R_{\mathrm{MLS}}\left(\tau\right) = \frac{-1}{N} + \frac{N+1}{N} R_{xx}\left(\tau\right) \otimes \sum_{m=-\infty}^{\infty} \delta\left(\tau + mNT\right),\ m = \pm 1, \pm 2, \ldots \tag{2.5}$$

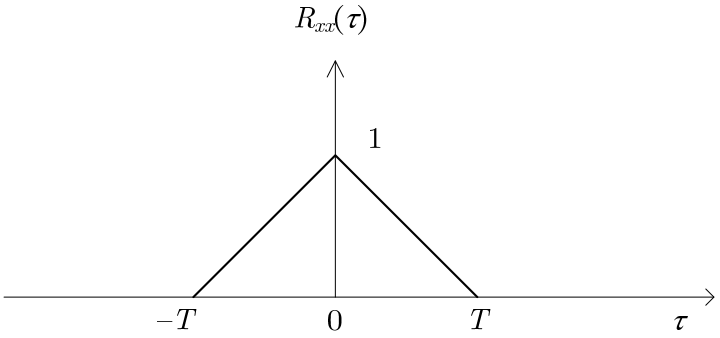


Figure 2-2 Autocorrelation function of a random binary sequence of rectangular pulses with amplitude ±1 and pulse duration T

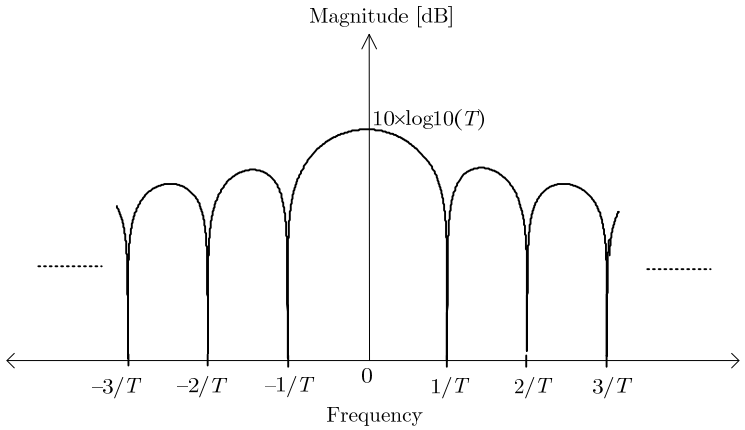


Figure 2-3 Power spectrum of the random binary process

The PSD of the MLS can be derived by taking the Fourier transform of Equation (2.5):

$$S_{\mathrm{MLS}}(f) = \frac{1}{N^2}\delta(f) + \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} (N+1)\,\mathrm{sinc}^2\left(\frac{m\pi}{N}\right)\delta\left(2\pi f + \frac{m2\pi}{NT}\right) \tag{2.6}$$

The envelope of the discrete spectrum of the MLS, as illustrated in Figure 2-5, is the same as the continuous spectra of the random binary process except for the DC component, which has the value, $1/N^2$. As the length of the MLS goes to infinity, the spacing between the bins, $1/NT$, approaches to zero [Kap06]. MLS have better auto-correlation properties than Gold code sequences; however, they are not preferred for CDMA since only a small number of MLS exist for a given sequence length and they have inferior cross-correlation properties compared to Gold codes [Bue06].

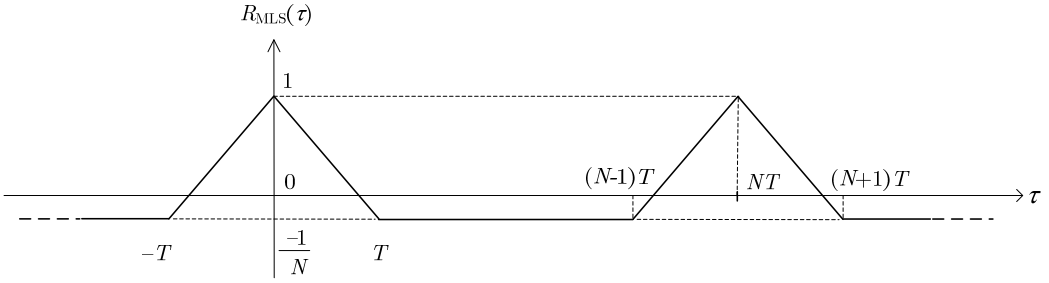


Figure 2-4 Autocorrelation function of a MLS code sequence

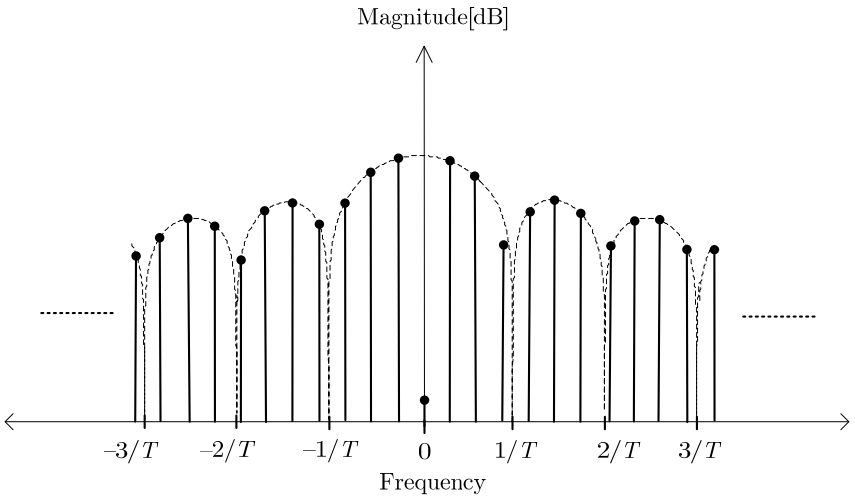
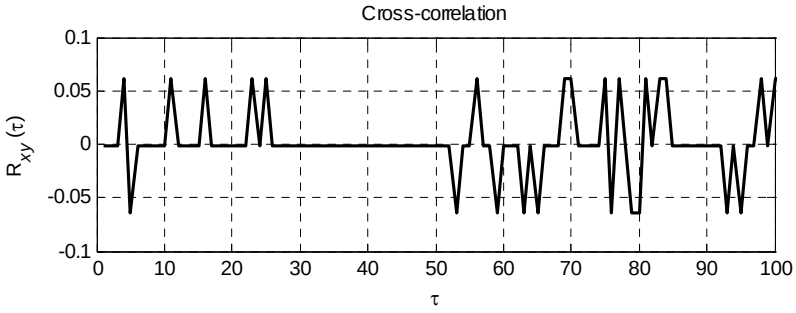


Figure 2-5 Power spectrum of a MLS code sequence (Bin spacing not to scale)

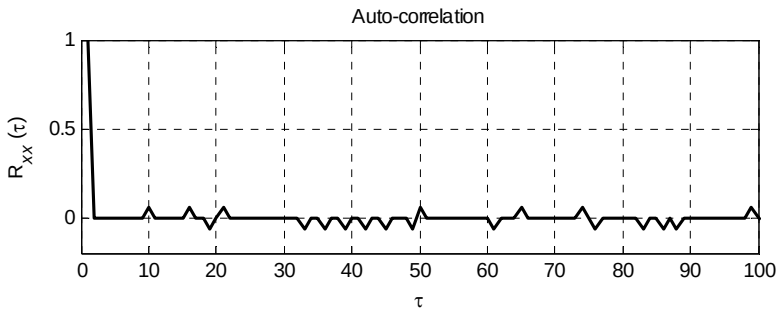
While a Gold code sequence has a four-valued autocorrelation function,

$$R_{\text{Gold}}(\tau) \in \left\{1, -\frac{1}{N}, -\frac{1}{N}\left(1+2^{\frac{n+2}{2}}\right), \frac{1}{N}\left(2^{\frac{n+2}{2}}-1\right)\right\}, n \text{ even}$$
$$R_{\text{Gold}}(\tau) \in \left\{1, -\frac{1}{N}, -\frac{1}{N}\left(1+2^{\frac{n+1}{2}}\right), \frac{1}{N}\left(2^{\frac{n+1}{2}}-1\right)\right\}, n \text{ odd} \quad (2.7)$$

a larger number of Gold code sequences for a given length are available with the desired cross-correlation properties. Cross-correlation function of two Gold code sequences takes the same values as that of the auto-correlation function, except for the peak value of one. Cross- and auto-correlation plots for two Gold codes of length 1023 are shown in Figure 2-6. Small fluctuations in the auto-correlation function of a Gold code sequence result in the deviation of discrete spectra of a Gold code sequence from the sinc-squared envelope, as illustrated in Figure 2-7 [Spi78]. The magnitude of each frequency bin depends on the particular Gold code sequence.



(a)



(b)

Figure 2-6 (a) Cross-correlation plot of two Gold code sequences (b) Auto-correlation plot of a Gold code sequence of length N=1023
(Only the first 100 values are shown)

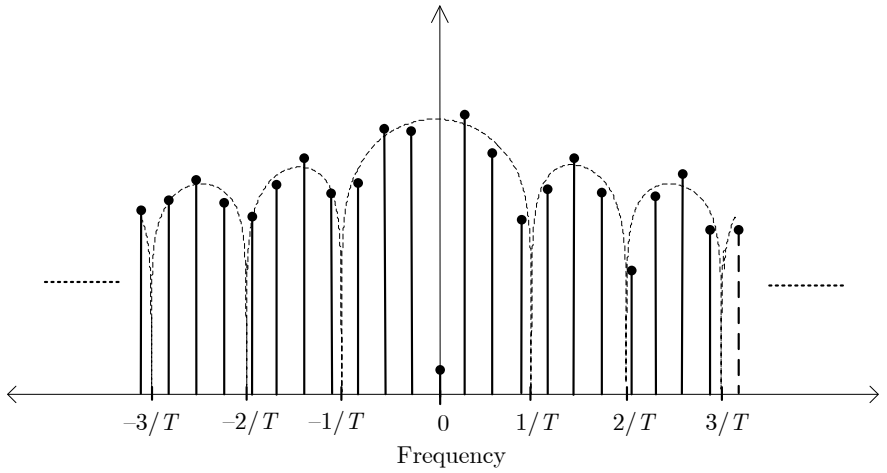


Figure 2-7 Power spectrum of a Gold code sequence (Bin spacing not to scale)

2.2 Modulation Schemes

GPS and Galileo signals are transmitted on five frequencies referred to as L1 (E1), L2, L5, E5, and E6. Sinusoidal RF carriers are generated at each satellite with an on-board caesium (Cs) and/or rubidium (Rb) atomic clock oscillating at 10.23MHz[†]. Respective frequencies are given as:

$$\begin{aligned} f_{\mathrm{L1}(E1)} &= 10.23 \times 154.0 = 1{,}575.420\,\mathrm{MHz} \\ f_{\mathrm{L2}} &= 10.23 \times 120.0 = 1{,}227.600\,\mathrm{MHz} \\ f_{\mathrm{L5}} &= 10.23 \times 115.0 = 1{,}176.450\,\mathrm{MHz} \\ f_{\mathrm{E5}} &= 10.23 \times 116.5 = 1{,}191.795\,\mathrm{MHz} \\ f_{\mathrm{E6}} &= 10.23 \times 125.0 = 1{,}278.750\,\mathrm{MHz} \end{aligned} \tag{2.8}$$

2.2.1 Phase Shift Keying

A PSK modulated signal consists of two components, namely:

- Sinusoidal RF carrier
- Binary-coded data

[†] Local Oscillators (LOs) are set to 10.22999999543MHz prior to launch of a satellite to compensate for the relativistic effects.

Direct Sequence Spread Spectrum (DSSS) signalling scheme adds a third component, the spreading code sequence, which is modulo-2 added with the data sequence. In GNSS, the binary-coded data is the navigation message, which contains clock corrections and orbital parameters of the satellites in order to enable the receiver to determine the location of a satellite at the instant of signal transmission. The modulo-2 addition of the navigation data with the spreading code is converted from unipolar to bipolar, i.e. {0,1}→{1,–1}, before modulating the sum onto the carrier. GPS/Galileo signals, which utilize PSK modulation, are either Binary PSK (BPSK) or Quadrature PSK (QPSK) modulated. The notation BPSK(b)/QPSK(b) is the shorthand for a BPSK/QPSK modulation with a spreading code rate of b×1.023Mc/s (Mega chips per second). A "chip" is one pulse in the spreading code and it is so called to emphasize that it does not hold any information [Bor07].

The phase of a BPSK modulated signal can take two distinct values, which are separated by π radians. A BPSK modulated radionavigation signal can be written as:

$$x_{\mathrm{BPSK}}(t) = \sqrt{2P} \cdot x(t) \cdot \cos\left(2\pi f_0 t + \phi\right) \tag{2.9}$$

where P is the transmitted signal power, $x(t)$ is the bipolar representation of the modulo-2 addition of the spreading code with the navigation data, f_0 is the carrier frequency, and ϕ is the carrier phase.

QPSK modulation is the summation of two BPSK modulated signals; therefore, the phase of a QPSK modulated signal can take four distinct values, which are separated by π/2 radians. A QPSK modulated radionavigation signal can be written as:

$$x_{\mathrm{QPSK}}(t) = \sqrt{2P_I} \cdot x_I(t) \cos\left(2\pi f_0 t + \phi_I\right) + \sqrt{2P_Q} \cdot x_Q(t) \cdot \sin\left(2\pi f_0 t + \phi_Q\right) \tag{2.10}$$

where P_I and P_Q are the powers, ϕ_I and ϕ_Q are the carrier phases of the In-phase (I) and Quadrate (Q) branches, respectively. QPSK modulation is utilized in GPS/Galileo to transmit different spreading codes, i.e. civilian and military, on the same carrier frequency. The phase of the BPSK/QPSK modulated radionavigation signal changes when there is a transition in the

spreading code or the navigation data sequence. The spectrum of the BPSK/QPSK signal is that of $x(t)$ translated to $\pm f_0$.

2.2.2 Binary Offset Carrier

BOC describes a class of spread spectrum modulations introduced for the next generation satellite navigation systems. The notation BOC(a,b) is the shorthand for a BOC modulation generated with a×1.023MHz subcarrier frequency and with b×1.023Mcps chipping rate. Sine and cosine phased BOC modulated signals can be written as [Bet99]:

$$\begin{aligned} x_{\mathrm{BOC}_s}(t) &= x_{\mathrm{PRN}}^{(k)}(t) \cdot \operatorname{sgn}\Big(\sin(2\pi f_{\mathrm{SC}} t)\Big) \\ x_{\mathrm{BOC}_c}(t) &= x_{\mathrm{PRN}}^{(k)}(t) \cdot \operatorname{sgn}\Big(\cos(2\pi f_{\mathrm{SC}} t)\Big) \end{aligned} \tag{2.11}$$

where $x_{\mathrm{PRN}}^{(k)}(t)$ is the bipolar representation of the spreading code sequence, f_{SC} is the subcarrier frequency, and sgn is the signum function,

$$\operatorname{sgn}\Big(x\Big) \triangleq \begin{cases} 1, & x \geq 0 \\ -1, & x < 0 \end{cases} \tag{2.12}$$

and f_{SC} is the subcarrier frequency. The subscripts s and c indicate sine and cosine phasing of the subcarrier, respectively. The modulation of the spreading code sequence onto the Square Wave (SW) subcarrier is sometimes referred to as BOC-PRN. The number of SW pulses per chip is called the BOC modulation order, which is a positive integer defined as:

$$k_{\mathrm{BOC}} \triangleq \frac{2a}{b} \tag{2.13}$$

Assuming the spreading code sequence is a binary random process with amplitude ±1 and the modulated signal has infinite bandwidth, the auto-correlation function of $\mathrm{BOC_S}$ and $\mathrm{BOC_C}$ have $2k_{\mathrm{BOC}}-1$ and $2k_{\mathrm{BOC}}+1$ peaks, respectively, that are separated by the SW pulse duration, $T_{\mathrm{SW}}=0.5\,T_{\mathrm{SC}}=(2f_{\mathrm{SC}})^{-1}$. The correlation value for the p^{th} peak can be written as [Bet02]:

$$R_{\mathrm{BOC}}(p)=\frac{\left(-1\right)^{p}\left(k_{\mathrm{BOC}}-\left|p\right|\right)}{k_{\mathrm{BOC}}} \tag{2.14}$$

The amplitude of the main peak (p=0) is equal to one when the signal has unlimited bandwidth and is less than one when the signal is band-limited. The auto-correlation function of $\mathrm{BOC}_s(a,a)$ is illustrated in Figure 2-8.

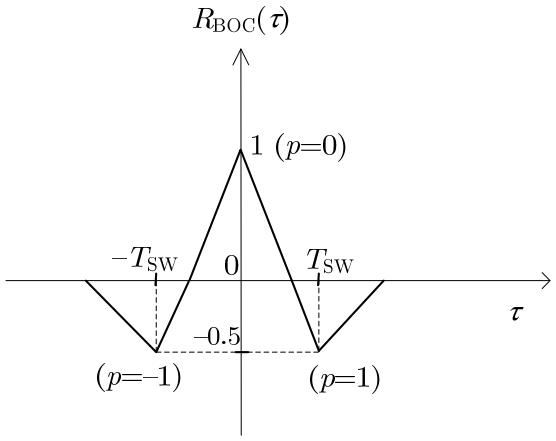


Figure 2-8 Autocorrelation function of BOC(a,a)

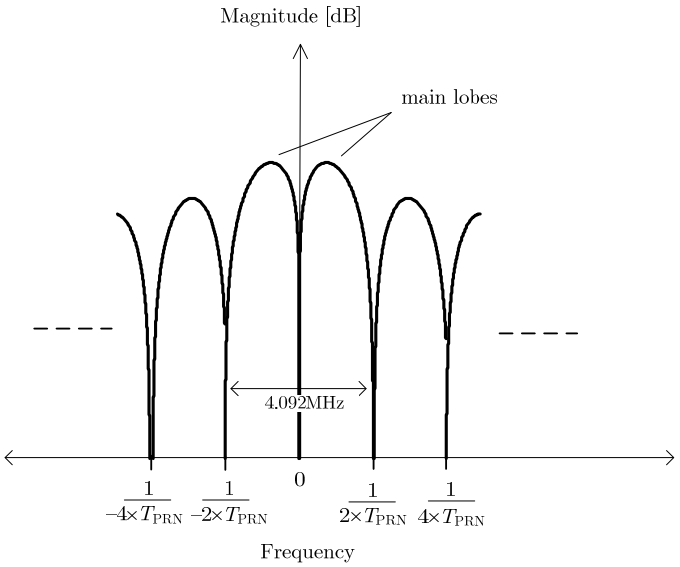
BOC modulation splits the sinc-shaped spectrum of the spreading code into two symmetrical spectral components (sidebands) with zero power on the carrier frequency. The PSD of a BOC-PRN signal is derived to be [Bet02], [Kap06]:

$$S_{\mathrm{BOC}_s}(f)=\begin{cases} T_{\mathrm{PRN}}\tan^{2}\left(\pi f\,T_{\mathrm{SC}}/2\right)\mathrm{sinc}^{2}\left(fT_{\mathrm{PRN}}\right),\text{even } k_{\mathrm{BOC}} \\ T_{\mathrm{PRN}}\tan^{2}\left(\pi f\,T_{\mathrm{SC}}/2\right)\dfrac{\cos^{2}\left(\pi fT_{\mathrm{PRN}}\right)}{\left(\pi fT_{\mathrm{PRN}}\right)^{2}},\ \text{odd } k_{\mathrm{BOC}} \end{cases} \tag{2.15}$$

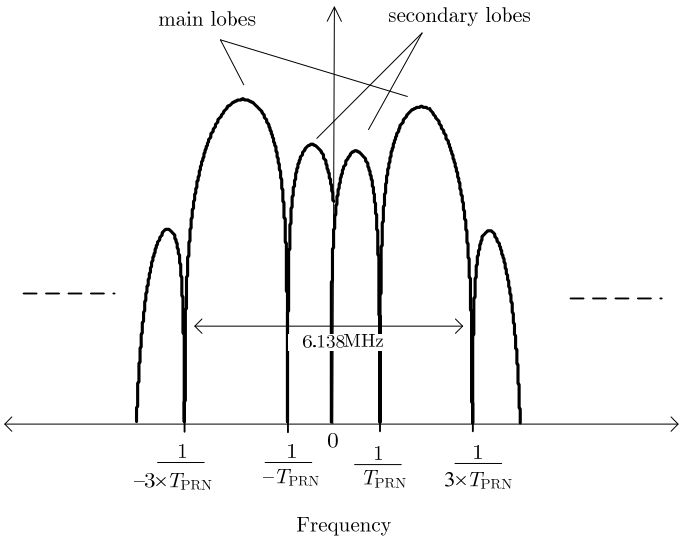
for sine-phased BOC modulation and

$$S_{\mathrm{BOC}_c}(f)=\begin{cases} 4T_{\mathrm{PRN}}\left(\dfrac{\sin^{2}\left(\pi f\,T_{\mathrm{SC}}/4\right)}{\cos\left(\pi f\,T_{\mathrm{SC}}/2\right)}\right)^{2}\mathrm{sinc}^{2}\left(fT_{\mathrm{PRN}}\right),\text{even } k_{\mathrm{BOC}} \\ 4T_{\mathrm{PRN}}\left(\dfrac{\sin^{2}\left(\pi f\,T_{\mathrm{SC}}/4\right)}{\cos\left(\pi f\,T_{\mathrm{SC}}/2\right)}\right)^{2}\dfrac{\cos^{2}\left(\pi fT_{\mathrm{PRN}}\right)}{\left(\pi fT_{\mathrm{PRN}}\right)^{2}},\text{odd } k_{\mathrm{BOC}} \end{cases} \tag{2.16}$$

for cosine-phased BOC modulation. The power spectrum of a BOC modulated signal has k_{BOC} lobes where the zero-crossings of the main lobes are spaced by twice the code rate and the zero-crossings of the secondary lobes are spaced by the code rate, as illustrated in Figure 2-9.



(a)



(b)

Figure 2-9 Power spectrum of (a) BOC$_S$(1,1) (b) BOC$_S$(2,1) modulated signal

Both sidebands of a BOC modulated signal contain all the information needed for ranging calculations and data demodulation. However, processing both sidebands coherently leads to better ranging performance [Bet02]. The main peak of the auto-correlation function of a BOC(a,b) modulated signal is

sharper than that of a PSK(b) modulated one, which results in better ranging accuracy and multipath handling. The side peaks of the auto-correlation function also enable the receiver to enhance the performance of signal tracking [Fin99].

2.3 GPS Signal Structure

Navstar GPS has been operational since 1995 with at least 24 satellites in orbit at all times, providing global coverage to civilian and military users [url06]. GPS modernization plans started in 1998 and have introduced two new civilian signals, L2C and L5, which will bring improvements to signal acquisition and tracking since they will provide longer and faster spreading code sequences, Forward Error Correction (FEC) [Wic95] on the navigation data, and data–free signal components. A modernized military signal, called the M-code, has also been introduced to provide better jamming resistance than the legacy Y-code, which is modulated onto L1 and L2 using BOC(10,5) scheme [Bar00]. GPS signal parameters are summarized in Table 2-1 [Nav04], [Nav06].

Table 2-1 GPS signal parameters

	L1			L2			L5
Service	Civilian	Military		Civilian	Military		Civilian
Code	C/A	P(Y)	M	CL/CM	P(Y)	M	I5/Q5
Modulation	BPSK	BPSK	BOC	BPSK	BPSK	BOC	QPSK
Chipping Rate [Mcps]	1.023	10.23	5.115	0.5115*	10.23	5.115	10.23
Subcarrier [MHz]	–	–	10.23	–	–	10.23	–
Data Rate [bps]	50	50	N/A	25	50	N/A	50
Bandwidth† [MHz]	2.046	20.46	30.69	2.046	20.46	30.69	20.46
Carrier [MHz]	1575.42			1227.60			1176.45

* Two 511.5Kcps code are multiplexed to give 1.023Mcps

† Null-to-null bandwidth for PSK modulation and the bandwidth between the outer nulls of the largest spectral lobes for BOC modulation [Kap06]

2.3.1 The L1 Signal

The set of Gold codes utilized for the civilian GPS L1 signal is called the Coarse Acquisition (C/A) code. The C/A code is so called since the acquisition of the code results in a coarse accuracy compared to that of the high-precision military code P(Y). Each C/A code is 1023 chips long and has a chipping rate of 1.023Mcps; therefore, it repeats itself every millisecond. The C/A code is generated by two maximal LFSR as depicted in Figure 2-10 [Nav06]. The positions of the feedback locations determine the output pattern of the sequence. The feedback of the top LSFR is from cells 3 and 10 and the corresponding polynomial is:

$$G_1 = 1 \oplus x_3 \oplus x_{10} \tag{2.17}$$

The feedback of the bottom LSFR is from cells 2, 3, 6, 8, 9, 10 and the corresponding polynomial is

$$G_2 = 1 \oplus x_2 \oplus x_3 \oplus x_6 \oplus x_8 \oplus x_9 \oplus x_{10} \tag{2.18}$$

where $\oplus$ donates modulo-2 addition (XOR). Initially, all cells are set to one. The output of the bottom maximal LSFR is generated from the two cells, S_1 and S_2. Position of S_1 and S_2 determine the output of G_2; and therefore, the C/A code.

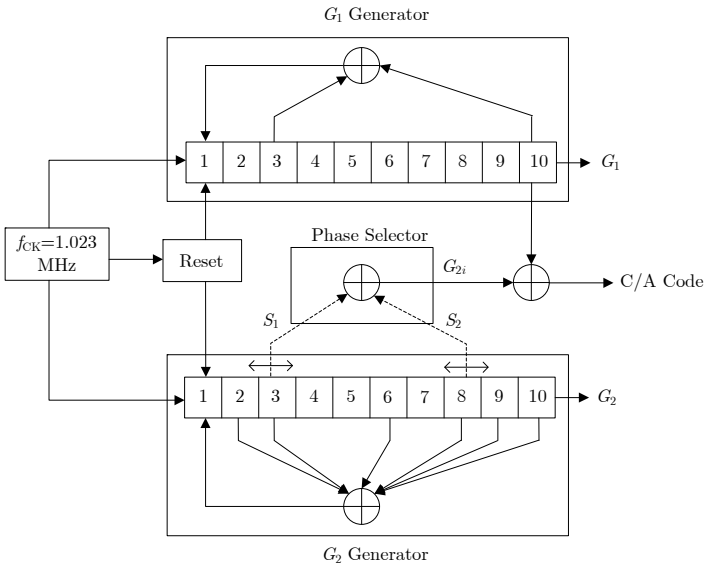


Figure 2-10 C/A code generator

With this configuration, shown in Figure 2-10, 37 different Gold code sequences can be generated. Among these, 32 of them are selected for the satellites and five other are reserved for other applications such as ground transmission [Tsu05]. The L1 signal generation scheme is illustrated in Figure 2-11[†] [Kap06]. The civilian and military signals are BPSK-modulated and superimposed on each other with a $\pi/2$ phase and 3dB amplitude difference. The L1 signal transmitted from satellite k can be written as:

$$x_{\mathrm{L1}}^{(k)}(t) = \underbrace{\sqrt{2P_I}\left[1-2\left(x_{\mathrm{C/A}}^{(k)}(t)\oplus x_{\mathrm{ND,L1}}^{(k)}(t)\right)\right]\cos\left(2\pi f_{\mathrm{L1}}t+\phi_I\right)}_{I(t)} + \underbrace{\sqrt{2P_Q}\left[1-2\left(x_{\mathrm{P(Y)}}^{(k)}(t)\oplus x_{\mathrm{ND,L1}}^{(k)}(t)\right)\right]\sin\left(2\pi f_{\mathrm{L1}}+\phi_Q\right)}_{Q(t)} \tag{2.19}$$

where $x_{\mathrm{C/A}}^{(k)}$ and $x_{\mathrm{P(Y)}}^{(k)}$ are the C/A and P(Y) code sequences assigned for satellite k, and $x_{\mathrm{ND,L1}}^{(k)}(t)$ is the navigation data sequence transmitted from satellite k. The civilian L1 signal has a null-to-null bandwidth of 2.046MHz and is located at the centre of the wider bandwidth P(Y) and M-code military signals, as shown in Figure 2-12.

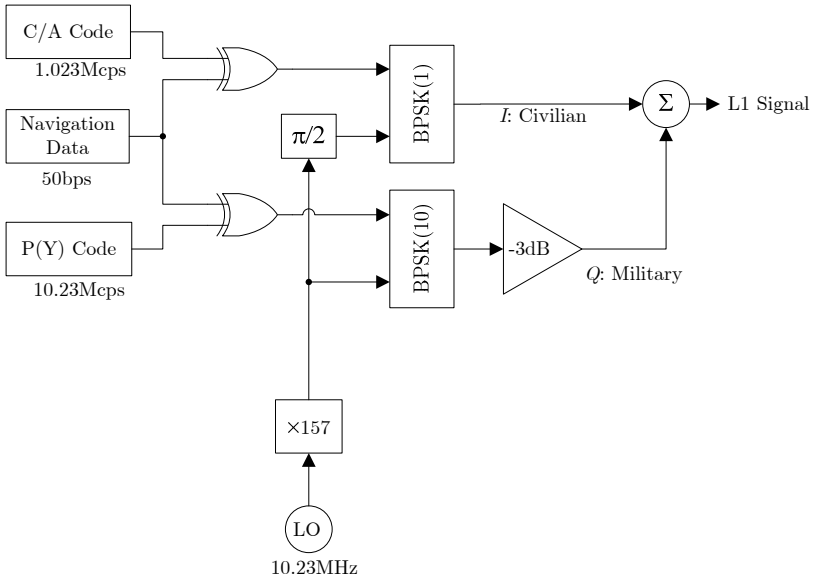


Figure 2-11 GPS L1 signal generation

[†] The new L1 military signal is not shown in Figure 2-11 and Equation (2.22) since, at the time of writing, very little has been published about it.

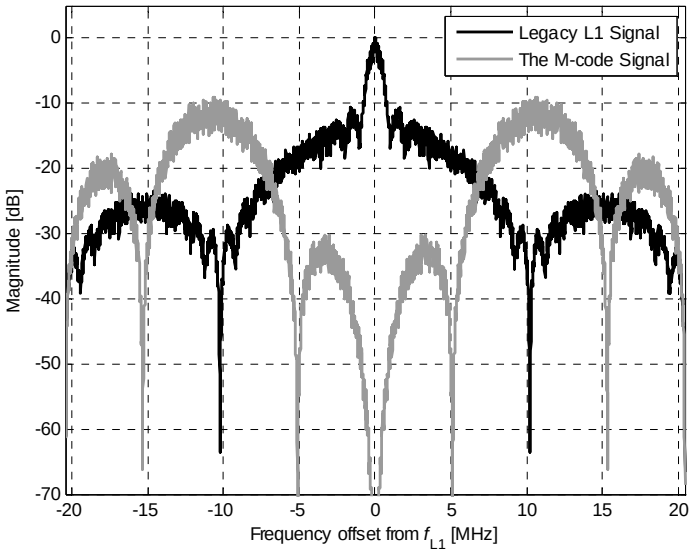


Figure 2-12 Power spectrum of the GPS L1 signal

2.3.2 The L2 Signal

The first satellite transmitting the L2C signal was launched in September 25, 2005. It is anticipated that global coverage with 24 L2C-enabled satellites will be available around 2012 [url07].

The L2C signal consists of two types of spreading code known as Civil Moderate (CM) and Civil Long (CL). The CM code has a period of 20ms and contains 10230 chips while the CL has a period of 1.5s and has 767250 chips. Code generation for CM and CL are described in the Navstar GPS interface specification, IS-GPS-200D [Nav04]. Each of the two codes has a chipping rate of 511.5Kcps. The CM code is modulo-2 added with a 25bps navigation data stream[†]. The CL code is not modulated with a navigation data, which improves the overall carrier tracking performance by 3dB since a pure Phase Locked Loop (PLL) discriminator can be utilized in the process instead of the Costas PLL [Fon01]. The navigation message, in this case, can be obtained by connecting the receiver to an assistance server. This procedure is known as Assisted GPS (A-GPS). The two codes are time-multiplexed together and the

[†] The convolutional code used in FEC has a code rate of ½; therefore, the 25bps navigation data input results in a 50Sps (Symbols per second) data stream.

combined sequence has a chipping rate of 1.023Mcps. The combined sequence, called Replacement Code (RC), modulates the L2 carrier at 1227.60MHz to generate the L2C signal, as illustrated in Figure 2-13‡.

The L2 signal transmitted from satellite k can be written as:

$$x_{\mathrm{L2C}}^{(k)}(t) = \underbrace{\sqrt{2P_I}\left[1-2\left(x_{\mathrm{RC}}^{(k)}(t) \oplus \mathrm{FEC}\left\{x_{\mathrm{ND,25bps}}^{(k)}(t)\right\}\right)\right]\cos\left(2\pi f_{\mathrm{L2}} t + \phi_I\right)}_{I(t)} + \underbrace{\sqrt{2P_Q}\left[1-2\left(x_{\mathrm{P(Y)}}^{(k)}(t) \oplus x_{\mathrm{ND,50bps}}^{(k)}(t)\right)\right]\sin\left(2\pi f_{\mathrm{L2}} + \phi_Q\right)}_{Q(t)} \quad (2.20)$$

where $x_{\mathrm{RC}}^{(k)}(t)$ is the RC sequence. The power spectrum of the L2 signal is similar to that of L1: The L2C signal with a null-to-null bandwidth of 2.046MHz is located at the centre of the military P(Y) and M-code signals.

The C/A code has a chipping rate of 1.023Mcps and a code length of 1023; as a result, the discrete spectrum of the C/A code has bins that are $1/(N\times T)$=1kHz apart. The power level of a bin in the discrete spectra of a C/A code sequence can be as high as –24dB relative to the total code power. When a narrowband interference signal is present, the correlator within the receiver spreads this interference creating a comb of frequency bins. The interference signal will only be attenuated by 24dB causing a leakage through the correlator, which can lead to degradation in navigation accuracy or complete loss of signal tracking [Spi95], [Kap06]. The L2C CM and CL codes are longer sequences with the overall chipping rate equal to that of the C/A code; therefore, have narrower frequency bin spacing, which minimizes the vulnerability of narrowband interference since the amount of power per frequency bin is diminished [Eng03]. Longer codes also provide better cross-correlation protection against self-interference [Die02].

‡ The new L2 military signal is not plotted in Figure 2-13 and in Equation (2.23) since, at the time of writing, very little has been published about it.

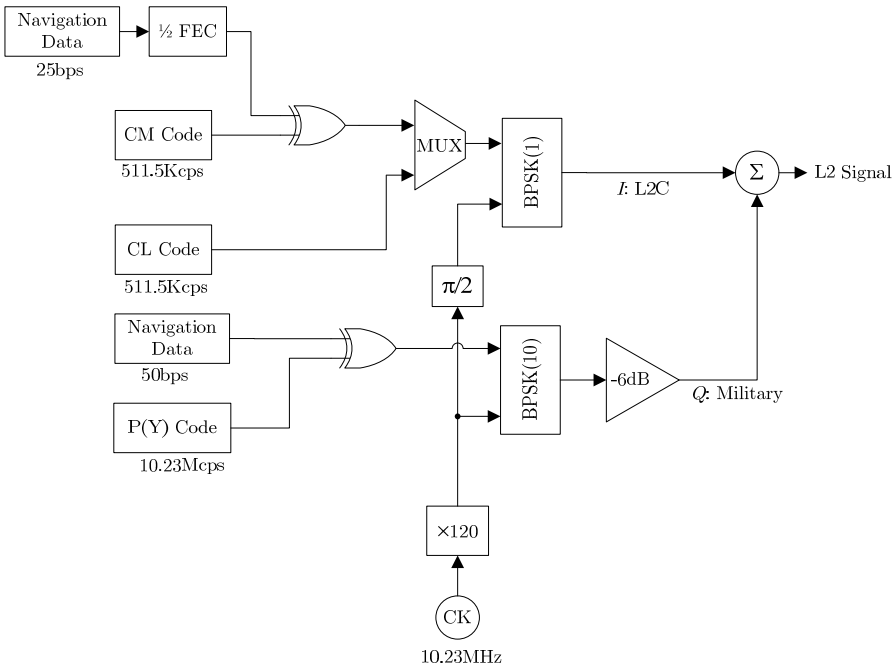
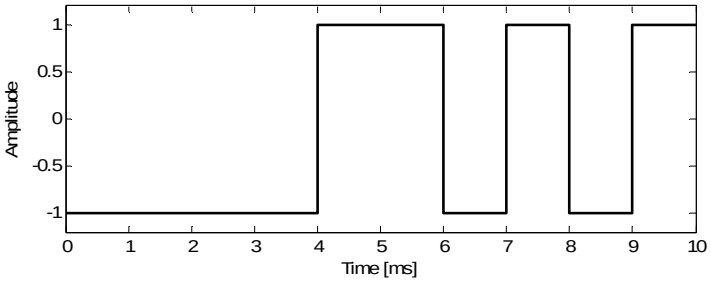


Figure 2-13 GPS L2 Signal Generation

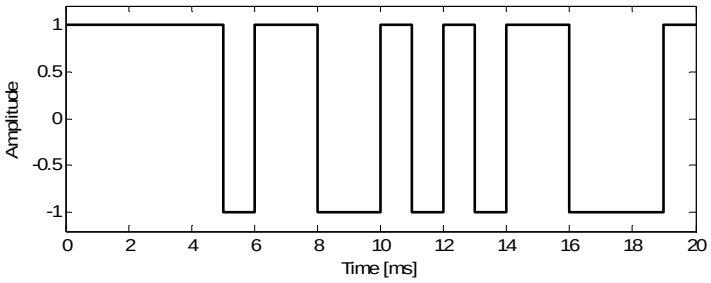
2.3.3 The L5 Signal

The L5 is intended to be a Safety-of-Life (SoL) signal for aircraft and maritime navigation. The first GPS satellite carrying a demonstration payload of the new L5 signal was launched in March 24, 2009 [url08]. The L5 signal consists of two spreading code sequences, the in-phase code (I5) and the quadrature Code (Q5), both with a chipping rate of 10.23Mcps and a code length of 10230. Code generation for I5 and Q5 are described in GPS interface specification, IS-GPS-705 [Nav06]. The two Neumann-Hoffman code sequences, plotted in Figure 2-14, are modulo-2 added with I5 and Q5 to extend the code length by a factor 10 and 20, respectively [Nav06]. The L5 signal transmitted from satellite k can be written as:

$$x_{\mathrm{L5}}^{(k)}(t) = \underbrace{\sqrt{2P_I}\left[1-2\left(x_{\mathrm{I5}}^{(k)}(t)\oplus x_{\mathrm{NH,10}}^{(k)}(t)\oplus \mathrm{FEC}\left\{x_{\mathrm{ND,50bps}}^{(k)}(t)\right\}\right)\right]\cos\left(2\pi f_{\mathrm{L5}}t+\phi_I\right)}_{I(t)} \\ \underbrace{+\sqrt{2P_Q}\left[1-2\left\{x_{\mathrm{Q5}}^{(k)}(t)\oplus x_{\mathrm{NH,20}}^{(k)}(t)\right\}\right]\sin\left(2\pi f_{\mathrm{L5}}+\phi_Q\right)}_{Q(t)} \tag{2.21}$$



(a)



(b)

Figure 2-14 (a) 10-chip Neumann-Hoffman code sequence $x_{\mathrm{NH},10}$(t) (b) 20-chipNeumann-Hoffman code sequence $x_{\mathrm{NH},20}$(t)

where $x_{\mathrm{I5}}^{(k)}(t)$, $x_{\mathrm{Q5}}^{(k)}(t)$, $x_{\mathrm{NH},10}^{(k)}(t)$, and $x_{\mathrm{NH},20}^{(k)}(t)$ are the I5, Q5, 10-chip NH and 20-chip NH code sequences, respectively. The L5 signal generation is illustrated in Figure 2-15 and the power spectrum is plotted in Figure 2-16. As the L2C signal, one of the codes in L5 is not modulo-2 added with the navigation data to improve the tracking performance.

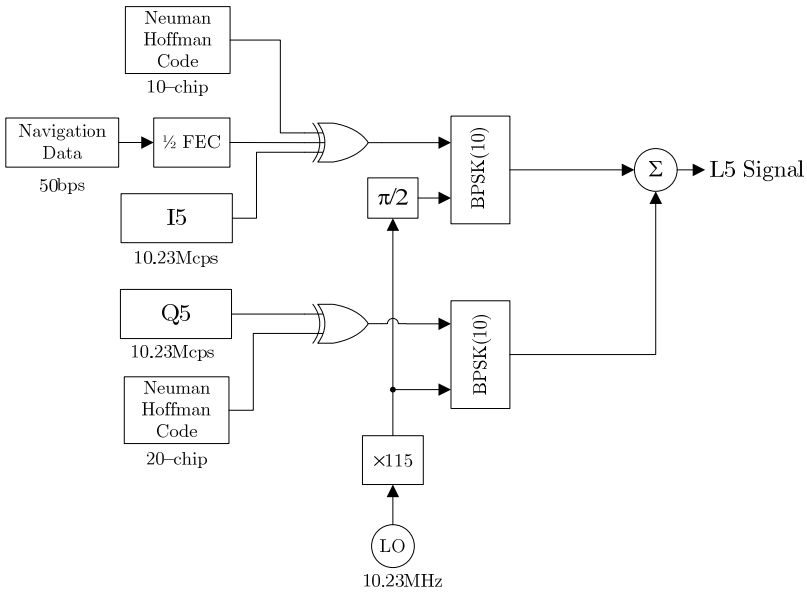


Figure 2-15 GPS L5 Signal Generation

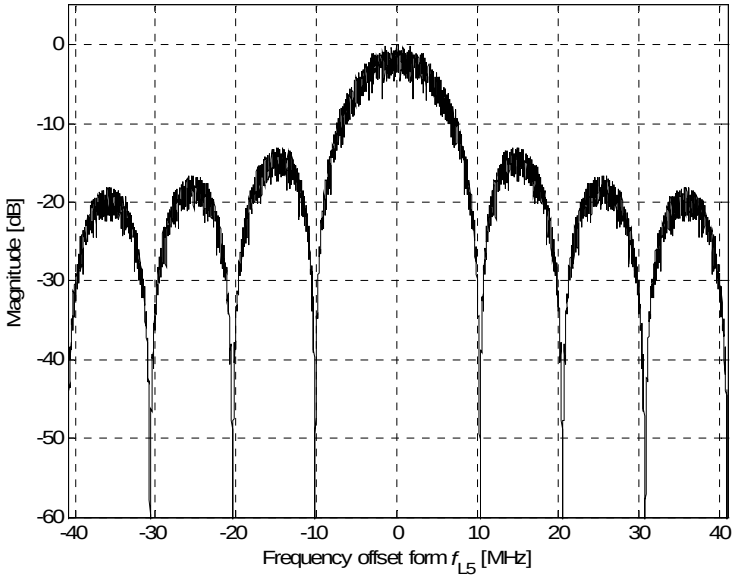


Figure 2-16 Power spectrum of the GPS L5 Signal

L5 spreading codes are faster and longer than the C/A code. The C/A code has a chipping rate of 1.023Mcps, which corresponds to a chip length of

$$\lambda = \frac{c}{f_{\mathrm{C/A}}} \simeq \frac{299{,}792{,}458\mathrm{m/s}}{1.023\mathrm{Mcps}} = 293.05\mathrm{m} \tag{2.22}$$

where λ is the wavelength, c is the speed of light, and $f_{\mathrm{C/A}}$ is the chipping rate of the C/A code. Assuming the time of arrival can be measured with accuracy of approximately 0.1% in a receiver, this corresponds to a range precision of 0.3m [Mis06]. Faster chipping rates lead to a sharper main peak in the auto-correlation function, which results in a better range precision. A sharp auto-correlation peak also helps to improve the multipath performance of the receiver, as illustrated in Figure 2-17.

2.4 Galileo Signal Structure

The fully developed Galileo will consist of 27 operational and three spare satellites and will provide multiple levels of service to the users [url09]. These are [Esa06], [Kap06]:

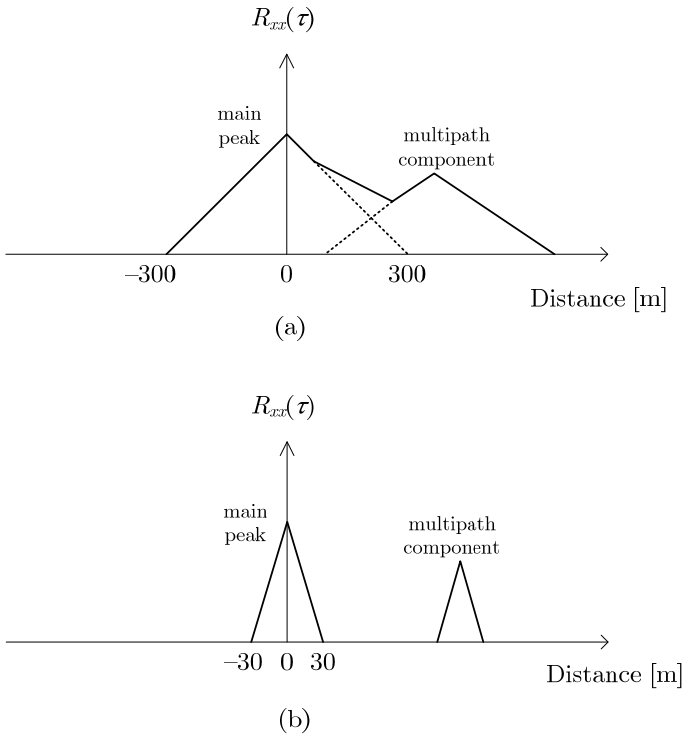


Figure 2-17 (a) The C/A code can resolve reflections that are delayed by 300m or more (b) The L5 codes can resolve reflections that are delayed by 30m or more [Eng03]

- An Open Service (OS) will provide position, velocity, and timing information that can be accessed free of charge. This service is particularly suitable with integration in mobile phones.
- An encrypted Commercial Service (CS) will allow value-added services such as weather alerts, accident warnings, traffic information, and map updates for higher accuracy applications.
- A SoL service will be used for safety-critical users involved in maritime, aviation, and railway modes of transportation.
- An encrypted Public Regulated Service (PRS) will only be offered to government-authorized users with a higher level of protection. The service will have increased robustness against interference and jamming.
- A Search and Rescue (SaR) service will allow relay of alarms from distress beacons to SaR organizations.

At the time of writing, Galileo has two satellites in orbit, Galileo In-Orbit Validation Element (GIOVE)-A and GIOVE-B, to test the novel features of Galileo signals. Galileo signal parameters are summarized in Table 2-2 [Esa09],

[Esa10]. Bandwidth in Table 2-2 is the null-to-null bandwidth for PSK-modulated signals and the bandwidth between the outer nulls of the largest spectral lobes for BOC-modulated signals [Kap06]. E5a and E5b can be thought as QPSK signals with 20.46MHz null-to-null bandwidth.

Table 2-2 Galileo signal parameters

	E1		E5		E6	
Service	OS	PRS	OS/CS	CS/SoL	CS	PRS
Modulation	BOC/CBOC	BOC	AltBOC		BPSK	BOC
Code Rate [Mcps]	1.023	2.5575	10.23		5.115	5.115
Subcarrier [MHz]	1.023	15.335	15.335		–	10.23
Data Rate [bps]	250	100	50	250	1000	100
Bandwidth [MHz]	16.368	40.92	92.07		10.23	30.69
Carrier [MHz]	1575.42		1176.45	1207.14	1278.75	

2.4.1 Spreading Codes

As explained in Section 2.1, longer codes provide better cross-correlation performance and robustness against interference; however, at the expense of longer signal acquisition times. The spreading codes for the Galileo E1-C, E5a/E5b, and E6-C are tiered codes, consisting of a shorter duration primary code modulo-2 added with a longer duration secondary code, as illustrated in Figure 2-18. Tiered codes enable a receiver to exclusively acquire and track primary codes when a strong signal is present and switch to tiered codes under poor signal conditions. Primary codes are truncated Gold codes that are generated on-board utilizing LFSRs, as depicted in Figure 2-19, while secondary codes are predefined. Lengths of the primary and secondary codes are given in Table 2-3.

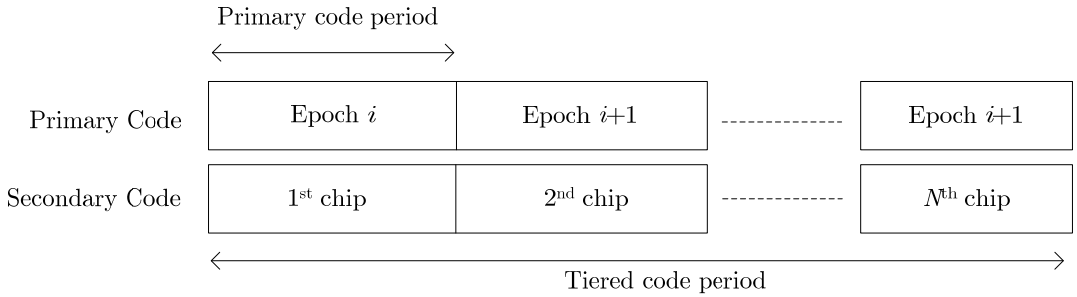


Figure 2-18 Galileo spreading code construction for E1 and E5 [Esa10]

The parameters (i.e. Base/Preset Register length and values) for generating the codes for OS signals can be accessed from the Galileo Open Service Signal in Space Interface Control Document (OS-SIS-ICD) [Esa07], [Esa10].

Table 2-3 Galileo spreading codes

	Tiered Code Period [ms]	Code Length [Chips]		Encryption
		Primary	Secondary	
E1-A	10	25575	–	✓
E1-B	4	4092	–	–
E1-C	200	8184	200	–
E5a-I	20	10230	20	–
E5a-Q	100	10230	100	–
E5b-I	4	10230	4	–
E5b-Q	100	10230	100	–
E6-A	10	51150	–	✓
E6-B	1	5115	–	✓
E6-C	100	10230	50	✓

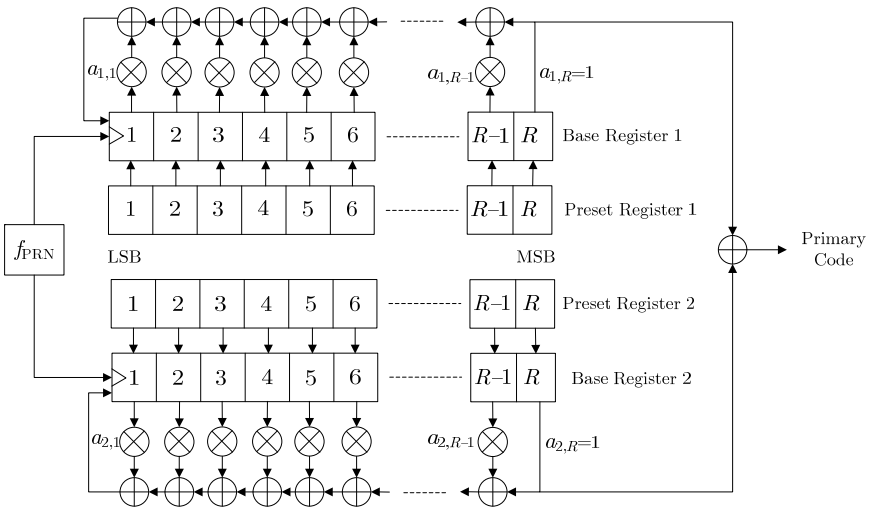


Figure 2-19 Primary code generation [Esa10]

2.4.2 The E1 Signal

In the E1 band, $BOC_s(1,1)$ was originally proposed as the modulation scheme for the OS signal, which is being transmitted from GIOVE-A. In 2007, the US and the EU announced their joint decision to implement an optimized modulation scheme, called the Multiplexed BOC (MBOC), for the Galileo E1

OS [url10]. The MBOC signal being transmitted from GIOVE-B is denoted as CBOC(6,1,1/11)[†], which defines a weighted composition of $\mathrm{BOC_S}(1,1)$ and $\mathrm{BOC_S}(6,1)$ with a PSD given by [Rod06]:

$$S_{\mathrm{CBOC(6,1,1/11)}}(f) = 10/11 \cdot S_{\mathrm{BOC}_s(1,1)}(f) + 1/11 \cdot S_{\mathrm{BOC}_s(6,1)}(f) \tag{2.23}$$

CBOC(6,1,1/11) modulated signal can be written in time domain as [Esa10]:

$$\begin{aligned} x_{\mathrm{E1,OS}}(t) = & \underbrace{\left[1-2\left(x_{\mathrm{PRN,E1b}}(t) \oplus x_{\mathrm{ND,250\,bps}}(t)\right)\right]\left(\sqrt{10/11}\cdot x_{\mathrm{SC1,E1}}(t) + \sqrt{1/11}\cdot x_{\mathrm{SC2,E1}}(t)\right)}_{x_{\mathrm{E1b}}(t)} \\ & - \underbrace{\left[1-2\left(x_{\mathrm{PRN,E1c}}(t)\right)\right]\left(\sqrt{10/11}\cdot x_{\mathrm{SC1,E1}}(t) - \sqrt{1/11}\cdot x_{\mathrm{SC2,E1}}(t)\right)}_{x_{\mathrm{E1c}}(t)} \end{aligned} \tag{2.24}$$

where $x_{\mathrm{SC1,E1}}$ and $x_{\mathrm{SC2,E1}}$ are the subcarriers given by:

$$\begin{aligned} x_{\mathrm{SC1,E1}}(t) &= \mathrm{sgn}\left(\sin\left(2\pi \times 1 \times 1.023e6\right)\right) \\ x_{\mathrm{SC2,E1}}(t) &= \mathrm{sgn}\left(\sin\left(2\pi \times 6 \times 1.023e6\right)\right) \end{aligned} \tag{2.25}$$

The autocorrelation function of CBOC(6,1,1/11) is similar to that of BOC(1,1); however, have a sharper main peak and can be written in terms of BOC(1,1) and BOC(6,1) as [Dov08]:

$$R_{\mathrm{CBOC(6,1,1/11)}}(\tau) = \frac{10}{11} R_{\mathrm{BOC(1,1)}}(\tau) + \frac{1}{11} R_{\mathrm{BOC(6,1)}}(\tau) \tag{2.26}$$

The power spectrum of CBOC(6,1,1/11) and BOC(6,1) is plotted in Figure 2-20. BOC(6,1) has 12 lobes with a null-to-null bandwidth of 2×8×1.023= 16.368MHz. The outer lobes of CBOC(6,1,1/11) also have zero-crossings at ±8×1.023MHz. CBOC(6,1,1/11) is opted instead of the BOC(1,1) since the increase in the power level of higher frequencies results in a sharper main peak in the auto-correlation function yielding better tracking and multipath performance [Dov08].

[†] CBOC stands for Composite BOC

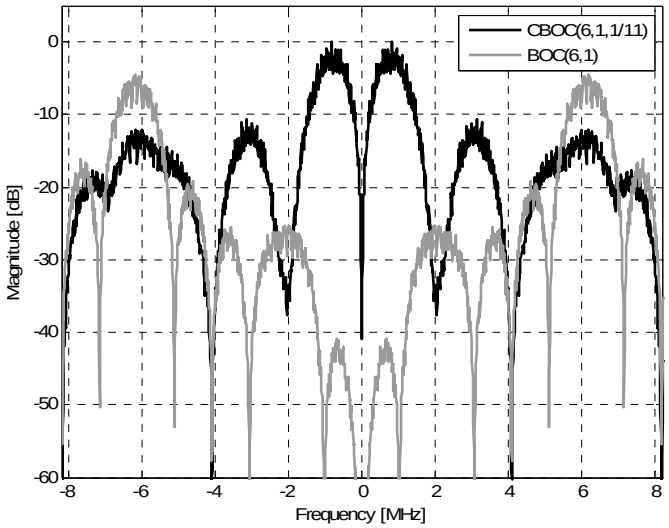


Figure 2-20 Power spectrum of CBOC(6,1,1/11) and BOC(6,1)

The PRS on E1 is $\mathrm{BOC}_C(15,2.5)$ modulated and the two services are multiplexed on the E1 carrier using Coherent Adaptive Subcarrier Modulation (CASM) in order to keep a constant power envelope over time which enables efficient use of payload amplifiers on-board. The combined E1 signal transmitted from GIOVE-B can be written as [Esa07], [Esa10]:

$$\begin{aligned} x_{\mathrm{E1}}(t) = {} & \sqrt{2P}\cdot\alpha\left(x_{\mathrm{E1b}}(t) - x_{\mathrm{E1c}}(t)\right)\cos\left(2\pi f_{\mathrm{E1}}t\right) \\ & -\sqrt{2P}\left[\beta\cdot x_{\mathrm{E1a}}(t) + \underbrace{\chi\left(x_{\mathrm{E1a}}(t)\cdot x_{\mathrm{E1b}}(t)\cdot x_{\mathrm{E1c}}(t)\right)}_{x_{\mathrm{IMP}}(t)}\right]\sin\left(2\pi f_{\mathrm{E1}}t\right) \end{aligned} \tag{2.27}$$

where $\alpha = \sqrt{2/3}$, $\beta = 2/3$, $\chi = 1/3$ ensures a constant power envelope. The InterModulation Product (IMP) is 11.11% of the total transmitted power that is wasted to keep a constant envelope. Signal generation scheme for the Galileo E1 band is illustrated in Figure 2-21 and the power spectrum is plotted in Figure 2-22.

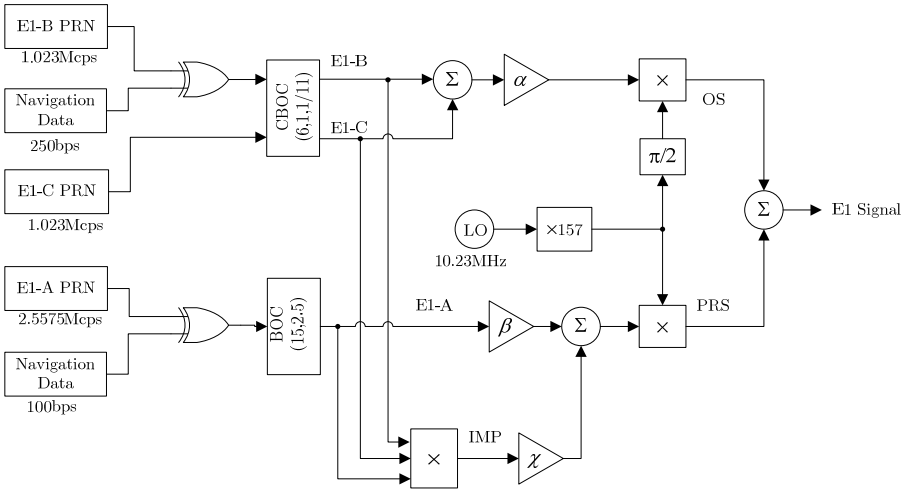


Figure 2-21 Galileo E1 signal generation

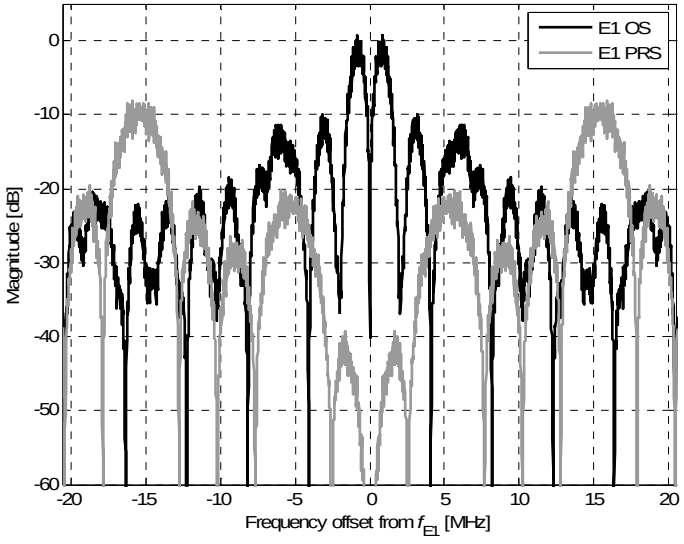


Figure 2-22 Power spectrum of the Galileo E1 OS and PRS

2.4.3 The E5 Signal

In the E5 band, the two spreading codes of the adjacent bands, E5a and E5b, are subdivided into four components, E5a-I, E5a-Q, E5b-I, and E5a-Q:

$$\begin{aligned} x_{\text{E5a-I}}(t) &= 1-2\left[x_{\text{PRN,E5a}}(t) \oplus x_{\text{ND,E5a}}(t)\right] \\ x_{\text{E5a-Q}}(t) &= 1-2\left[x_{\text{PRN,E5a}}(t)\right] \\ x_{\text{E5b-I}}(t) &= 1-2\left[x_{\text{PRN,E5b}}(t) \oplus x_{\text{ND,E5b}}(t)\right] \\ x_{\text{E5b-Q}}(t) &= 1-2\left[x_{\text{PRN,E5a}}(t)\right] \end{aligned} \tag{2.28}$$

which are multiplexed on the E5 carrier using constant envelope Alternative BOC (AltBOC) modulation scheme. The standard AltBOC modulation for multiplexing E5 components of can be written as:

$$x_{\text{AltBOC}}(t) = \left[\left(x_{\text{E5a-I}}(t) + jx_{\text{E5a-Q}}(t)\right)x_{\text{CSC}}(t)\right] + \left[\left(x_{\text{E5a-I}}(t) + jx_{\text{E5a-Q}}(t)\right)x^{*}_{\text{CSC}}(t)\right] \quad (2.29)$$

where $x_{\text{CSC}}(t)$ and $x^{*}_{\text{CSC}}(t)$ are the complex SW subcarriers given as:

$$\begin{aligned} x_{\text{CSC}}(t) &\triangleq \operatorname{sgn}\left(\cos\left(2\pi f_{\text{SC}}t\right)\right) + j\operatorname{sgn}\left(\cos\left(2\pi f_{\text{SC}}t\right)\right) \\ x^{*}_{\text{CSC}}(t) &\triangleq \operatorname{sgn}\left(\cos\left(2\pi f_{\text{SC}}t\right)\right) - j\operatorname{sgn}\left(\cos\left(2\pi f_{\text{SC}}t\right)\right) \end{aligned} \quad (2.30)$$

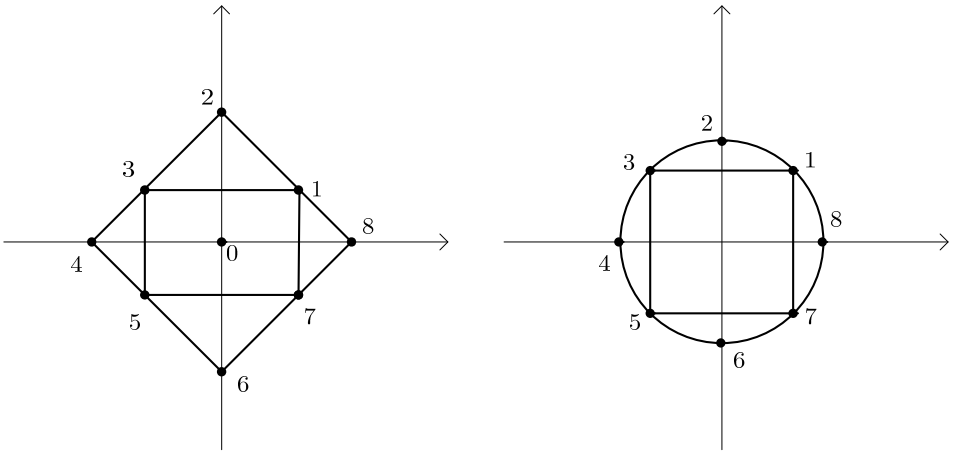
As can be observed from the constellation diagram in Figure 2-23(a), the modulation envelope of the standard AltBOC is not constant [Rie03]. A constant power envelope for the E5 signal can be achieved by introducing the IMPs:

$$\begin{aligned} \overline{x}_{\text{E5a,I}}(t) &\triangleq x_{\text{E5a-Q}}(t)\cdot x_{\text{E5b-I}}(t)\cdot x_{\text{E5b-Q}}(t) \\ \overline{x}_{\text{E5a,Q}}(t) &\triangleq x_{\text{E5a-I}}(t)\cdot x_{\text{E5b-I}}(t)\cdot x_{\text{E5b-Q}}(t) \\ \overline{x}_{\text{E5b,I}}(t) &\triangleq x_{\text{E5b-Q}}(t)\cdot x_{\text{E5a-I}}(t)\cdot x_{\text{E5a-Q}}(t) \\ \overline{x}_{\text{E5b,I}}(t) &\triangleq x_{\text{E5b-I}}(t)\cdot x_{\text{E5a-I}}(t)\cdot x_{\text{E5a-Q}}(t) \end{aligned} \quad (2.31)$$

The constant envelope AltBOC modulation for the E5 signal can then be written as [Reb06], [Kap06], [Esa10]:

$$\begin{aligned} x_{\text{AltBOC,E5}}(t) = {} & \frac{1}{2\sqrt{2}}\left[x_{\text{E5a-I}}(t) + jx_{\text{E5a-Q}}(t)\right]\underbrace{\left[x_{\text{SC1,E5}}(t) - jx_{\text{SC1,E5}}\left(t - T_{\text{SC,E5}}/4\right)\right]}_{x^{*}_{\text{CSC1}}(t)} \\ & + \frac{1}{2\sqrt{2}}\left[x_{\text{E5b-I}}(t) + jx_{\text{E5b-Q}}(t)\right]\underbrace{\left[x_{\text{SC1,E5}}(t) + jx_{\text{SC1,E5}}\left(t - T_{\text{SC,E5}}/4\right)\right]}_{x_{\text{CSC1}}(t)} \\ & + \frac{1}{2\sqrt{2}}\left[\overline{x}_{\text{E5a-I}}(t) + j\overline{x}_{\text{E5-Q}}(t)\right]\underbrace{\left[x_{\text{SC2,E5}}(t) - jx_{\text{SC2,E5}}\left(t - T_{\text{SC,E5}}/4\right)\right]}_{x^{*}_{\text{CSC2}}(t)} \\ & + \frac{1}{2\sqrt{2}}\left[\overline{x}_{\text{E5b-I}}(t) + j\overline{x}_{\text{E5b-Q}}(t)\right]\underbrace{\left[x_{\text{SC2,E5}}(t) + jx_{\text{SC2,E5}}\left(t - T_{\text{SC,E5}}/4\right)\right]}_{x_{\text{CSC2}}(t)} \end{aligned} \quad (2.32)$$

where $T_{SC,E5}=(f_{SC,E5})^{-1}=(15\times1.023\times10^{6})^{-1}$s is the subcarrier period. The modulation scheme for E5 is sometimes referred to as AltBOC(15,10) since the subcarrier frequency is 15×1.023MHz and the chipping rate is 10×1.023MHz. The four-level SW subcarriers are plotted in Figure 2-24. The complex E5 signal can be described as an 8-PSK signal with the constellation diagram given in Figure 2-23(b).



(a) (b)

Figure 2-23 Modulation constellation for the (a) Standard (b) Constant envelope four-component AltBOC

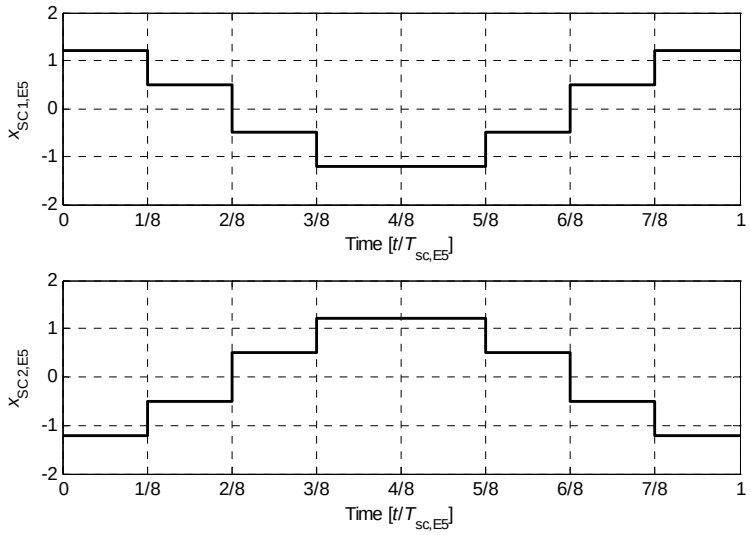


Figure 2-24 One period of the Galileo E5 AltBOC subcarriers

The auto-correlation function of the constant envelope AltBOC(a,b) is similar to that of BOC(a,b); however, the IMP makes the main peak sharper.

The PSD of the constant envelope AltBOC is derived for odd values of k_{AltBOC}[†] is derived to be [Reb05]:

$$S_{\mathrm{E5,AltBOC}}(f) = \frac{4\cos^2\left(\pi f T_{\mathrm{PRN}}\right)}{T_{\mathrm{PRN}}\left(\pi f\right)^2\cos^2\left(\pi f T_{\mathrm{PRN}}/k_{\mathrm{AltBOC}}\right)} \cdot\left[\cos^2\left(\pi f T_{\mathrm{SW}}\right) - \cos\left(\pi f T_{\mathrm{SW}}\right) - 2\cos\left(\pi f T_{\mathrm{SW}}\right)\cos^2\left(\frac{\pi f T_{\mathrm{SW}}}{2}\right) + 2\right] \tag{2.33}$$

The transmitted E5 signal, as illustrated in Figure 2-25, can be written as [Kap06]:

$$x_{\mathrm{E5}}(t) = \sqrt{2P}\,\mathrm{Re}\left\{x_{\mathrm{E5,AltBOC}}(t)\right\}\cos\left(2\pi f_{\mathrm{E5}} + \phi_1\right) - \sqrt{2P}\,\mathrm{Im}\left\{x_{\mathrm{E5,AltBOC}}(t)\right\}\sin\left(2\pi f_{\mathrm{E5}} + \phi_2\right) \tag{2.34}$$

where Re{.} and Im{.} are the real and imaginary parts of the AltBOC(15,10) signal. The power spectrum of the E5 signal is plotted in Figure 2-26. As can be seen from Figure 2-27, complex subcarriers x_{CSC1}(t) and x_{CSC2}(t) shift the baseband signals x_{E5a} and x_{E5b} to $\pm f_{\mathrm{SC,E5}}$ while x_{CSC3}(t) and x_{CSC4}(t) shift the IMPs to $\pm 3f_{\mathrm{SC,E5}}$. The two adjacent bands, E5a and E5b, can be thought as two QPSK(10)-modulated signals centred at $f_{\mathrm{E5}}\pm f_{\mathrm{SC,E5}}$. Therefore, the conventional PSK tracking techniques can be utilized for single sideband tracking. The other option is to perform coherent dual-band processing to get the best performance; however, due to the complex nature of the AltBOC signal, one complex correlation requires four conventional correlators [Tes07]. Innovative techniques for tracking the AltBOC signal are introduced in [Ger05], [DeW06], and [Dov07].

[†] $k_{\mathrm{AltBOC}} \triangleq \frac{2a}{b}$ for AltBOC(a,b)

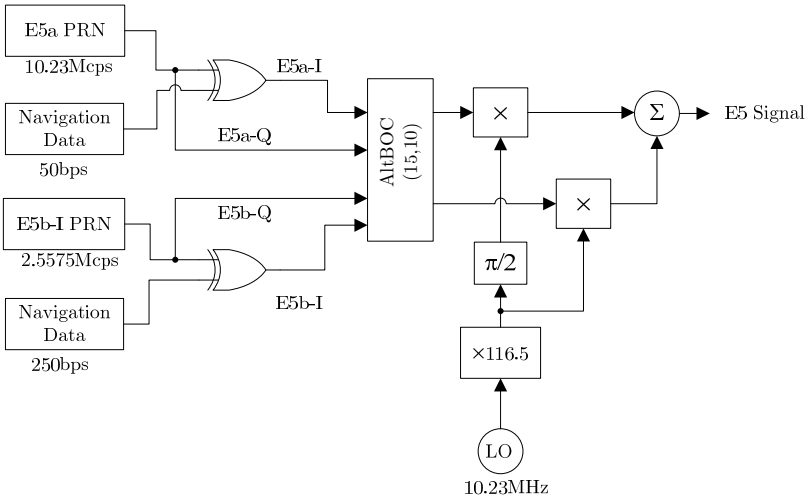


Figure 2-25 Galileo E5 signal generation

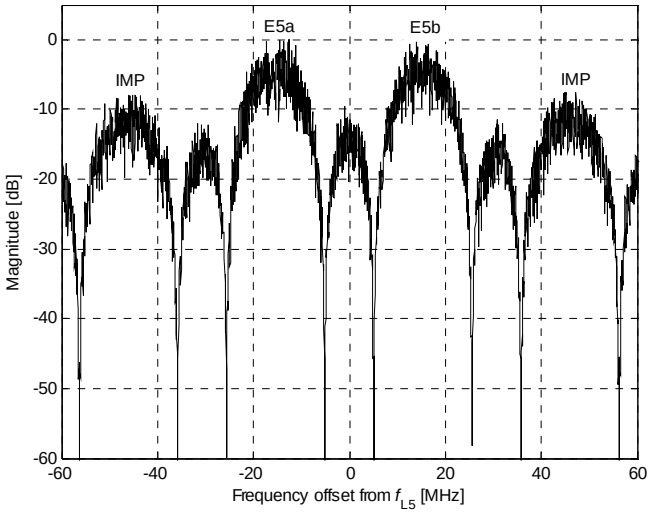


Figure 2-26 Power spectrum of the Galileo E5 signal

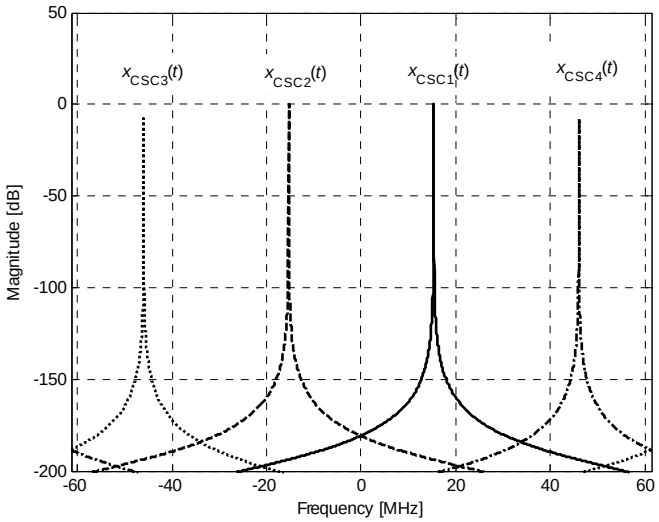


Figure 2-27 Locations of the complex subcarriers in the spectrum

2.4.4 The E6 Band

In the E6 band, BPSK(5) modulated CS signal is multiplexed with $\mathrm{BOC}_C(10,5)$ modulated PRS signal on the E6 carrier using CASM. The composite E6 signal can be written as:

$$\begin{aligned} x_{\mathrm{E6}}(t) = {} & \sqrt{2P}\cdot\alpha\left(x_{\mathrm{E6b}}(t) - x_{\mathrm{E6c}}(t)\right)\cos\left(2\pi f_{\mathrm{E6}}t + \phi_1\right) \\ & -\sqrt{2P}\left[\beta\cdot x_{\mathrm{E6a}}(t) + \underbrace{\chi\left(x_{\mathrm{E6a}}(t)\cdot x_{\mathrm{E6b}}(t)\cdot x_{\mathrm{E6c}}(t)\right)}_{x_{\mathrm{IMP}}(t)}\right]\sin\left(2\pi f_{\mathrm{E6}}t + \phi_2\right) \end{aligned} \tag{2.35}$$

As the CASM for the E1 signal, the coefficients $\alpha = \sqrt{2/3}$, $\beta = 2/3$, and $\chi = 1/3$ ensure a constant power envelope. The power spectrum of the composite E6 signal is plotted in Figure 2-28.

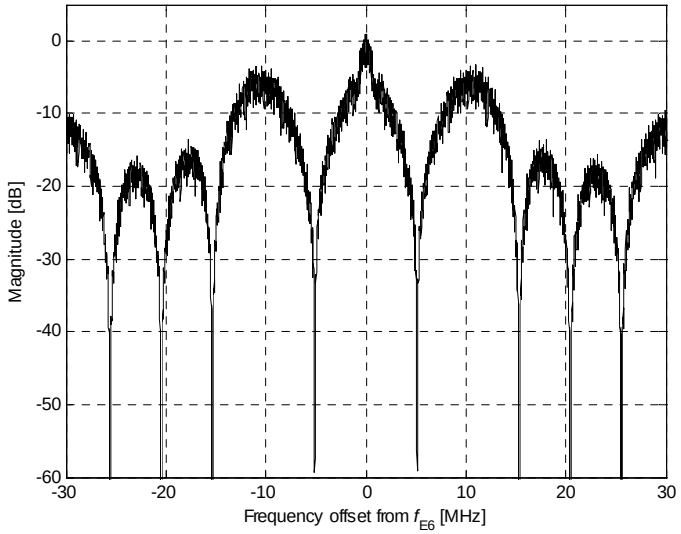


Figure 2-28 Power spectrum of the E6 band

Chapter 3

Design Considerations for a Multi-Constellation GNSS Receiver Front-End

As outlined in Chapter 2, the new radionavigation signals will provide better positioning accuracy and robustness against multipath and interference. The reception of signals from multiple frequencies will provide an estimation of the ionospheric delay. A multi-constellation receiver also benefits from greater signal availability. This chapter is intended to discuss the design considerations for a multi-constellation GNSS receiver front-end. Various RF front-end topologies are compared and their advantage and disadvantages are outlined. This is followed by a noise analysis for subsampling A/D conversion.

3.1 Overview of a GNSS Receiver

A typical GNSS receiver can be divided into four main parts, as depicted in Figure 3-1:

- Antenna
- RF front-end
- ADC
- DSP

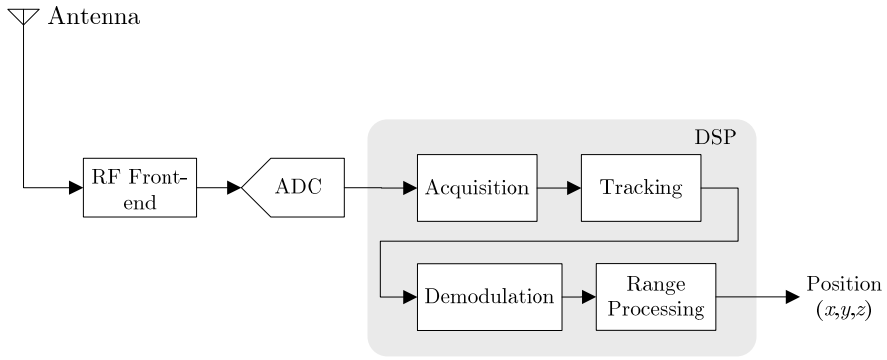


Figure 3-1 Building blocks of a GNSS receiver

GNSS antennas are generally right-hand circularly polarized and provide almost full sky coverage with small gain variation from zenith to azimuth to be able to receive signals from all satellites with comparable strength to minimize self-interference [Bra99]. However, a trade-off exists between the maximum number of visible satellite to the receiver and the magnitude of interference since interfering signals usually come from a low elevation angle [Tsu05]. Radionavigation signals travel more than 20,000km at the speed of light to reach the Earth; therefore, the received signal power at the antenna is below the thermal noise floor of the receiver. The thermal noise power is given as:

$$P_{\mathrm{TN}}[\mathrm{watt}] = k_{\mathrm{B}} \cdot T_0 \cdot \Delta f \tag{3.1}$$

where k_{B}=1.3806×10^{-23}J/^{o}K is the Boltzmann's constant, T_0 is the effective noise temperature in Kelvin, and Δf is the noise bandwidth in Hertz. The PSD

of thermal noise at room temperature (290°K) is 4.0037×10^{-21}watts/Hz or –173.97dBm/Hz. The received signal power is at a minimum when the satellite at 5° elevation. The minimum received signal power for the C/A code is –128.5dBm; therefore, the minimum SNR at the antenna at 290°K in 2.046MHz bandwidth is –17.63dB. The lowest C/N_0 at the input of the antenna for a C/A code receiver is:

$$\begin{aligned}\left(C/N_0\right)_{ANT} &= 10\times\log 10(\triangle f)+\mathrm{SNR}_{C/A}\\ &\simeq 10\times\log 10(2.046\times10^6)-17.63\\ &\simeq 45.47\,\mathrm{dB/\,Hz}\end{aligned} \tag{3.2}$$

which means the signal power is actually at least 35,000 times stronger than the noise power in 1-Hz bandwidth.

The RF front-end amplifies the received signal and down-converts it to an IF. As the received signal is below the thermal noise floor, a low noise figure is essential in the RF front-end. The combined noise figure of the RF front-end and the ADC can be formulated as [Chi03]:

$$\mathrm{NF}_{\mathrm{RF+ADC}} = \mathrm{SNR}_{\mathrm{ANT}} + G_P - \mathrm{SNR}_{\mathrm{PC}} \tag{3.3}$$

where $\mathrm{SNR}_{\mathrm{ANT}}$ is the SNR at the input of the antenna, $\mathrm{SNR}_{\mathrm{PC}}$ is the minimum required SNR at the output of a correlator to demodulate the radionavigation signal (also known as the post-correlation SNR), and G_P is the processing gain of spread spectrum modulation, which is defined as:

$$G_{\mathrm{P}} = 10\times\log 10\left(\frac{f_{\mathrm{PRN}}}{f_{\mathrm{ND}}}\right) \tag{3.4}$$

In other words, a GNSS receiver must have a high sensitivity. Sensitivity of the receiver can be described as [Che10]:

$$S[\mathrm{dBm}]=\underbrace{10\times\log 10(\triangle f)+S_{\mathrm{TN}}[\mathrm{dB/Hz}]+\mathrm{NF}}_{P_N[\mathrm{dB}]}+\mathrm{SNR}_{\mathrm{PC}}-G_{\mathrm{P}} \tag{3.5}$$

where S_{TN} is the PSD of the thermal noise in dB/Hz and P_N is the total noise power in dB.

Most commercial GNSS receivers employ Flash ADCs for A/D conversion. A Flash ADC, as illustrated in Figure 3-2, typically consists of[†]:

- An AA filter for band-limiting the input spectrum
- A Sample and Hold (S/H) or a Track-and-Hold (T/H) for sampling the CT input signal
- A quantizer for mapping the CT voltage or current into Discrete-Time (DT)

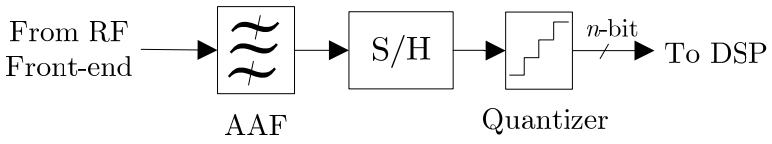


Figure 3-2 Block diagram of a typical Flash ADC

The GNSS signal is still below the thermal noise floor at the input of the ADC; therefore, the amplification provided by the RF front-end raises the thermal noise floor level, not the signal, to ADC's Full Scale Range (FSR). The amplification required is approximately 110dB for a C/A code receiver. Since GNSS signals are spread spectrum, the dynamic range requirement of a GNSS receiver need not be very high; nevertheless, the receiver must accommodate for the maximum expected magnitude of interference [Kap06]. A Variable Gain Amplifier (VGA) must ensure that the magnitude of interference does not exceed the thermal noise floor. Most low-cost commercial GNSS receivers employ single-bit quantization while high-end receivers quantize the signal up to 3-bits. The signal degradation for 1-bit and 3-bit quantization is given in Table 3-1. The VGA is not required when a single-bit ADC is used since; in this case, the ADC is simply a single comparator. Receivers manufactured for military users generally have higher dynamic range to avoid the saturation of the ADC by a strong jamming signal.

[†] In high-speed Flash ADCs, sampling is generally performed within the quantizer by latched comparators rather than with a separate front-end S/H circuit as latched comparators operate faster [Raz95].

Table 3-1 Signal degradation due to quantization [Bra99]

	Quantization	
IF Bandwidth	1-bit	3-bit
$1/T_{\text{PRN}}$	3.5dB	0.7dB
$5/T_{\text{PRN}}$	2.25dB	0.3dB

The digitized signal is first processed by the acquisition block where the coarse values of code and carrier for the visible satellites are determined. There are several techniques to detect the visible satellites. The serial search acquisition performs time-domain correlation, which carries out two different sweeps: A frequency search over all possible carrier frequencies and a code phase search over all different code phases to find the correlation peak. For the C/A code the number of sweeps required is:

$$\underbrace{1023}_{\substack{\text{code phase}\\ \text{combinations}}} \times \underbrace{\left(2 \times \frac{10,000\text{Hz}}{500\text{Hz}} + 1\right)}_{\substack{\text{carrier phase}\\ \text{combinations}}} = 41,943 \tag{3.6}$$

In Equation (3.6), it is assumed that the frequency precision is 500Hz and that the combined motion of the satellite and the receiver may cause the centre frequency of the carrier to shift by up to ±10kHz [Bor07]. This method is quite time consuming and is not suitable for a multi-constellation receiver especially since the length of the spreading codes for the new signals are much longer. The parallel code phase search technique, as illustrated in Figure 3-3, parallelizes the search for the code phase by calculating the correlation in the frequency domain [Lin98]. The search space is cut down to carrier phase combinations at the expense of increased hardware complexity. At each search step, IF carrier generated by a Numerically Controlled Oscillator (NCO) is shifted by an amount equal to the carrier phase search precision. Since the carrier phase is unknown, a quadrature mixer is needed to search for both I and Q channels for a certain spreading code. The frequency domain representation of the circular correlation is calculated by multiplying the Discrete Fourier Transform (DFT) of the incoming signal with the complex conjugate of the DFT of the spreading code. The frequency domain representation of correlation values is translated into time-domain by taking the Inverse DFT (IDFT) at each search step in order to find the correlation

peak. The acquisition process is repeated until signals from all visible satellite are acquired and the results obtained are utilized to initialize the tracking channels where code and carrier phase are fine-tuned, as illustrated in Figure 3-4 [Kap06].

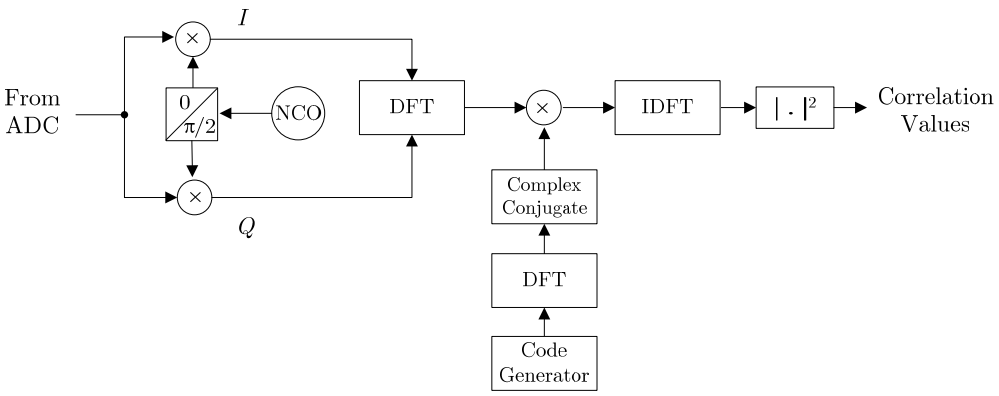


Figure 3-3 Parallel code phase search acquisition

Code tracking is performed with a Delayed Lock Loop (DLL) where three or more code replicas, often separated by half a chip length, are generated and correlated with the incoming signal. Carrier tracking, on the other hand, is performed with a Phase Locked Loop (PLL) that is insensitive to navigation bit transitions, called the Costas Loop. Pilot channels, which do not contain navigation data, can be tracked with an ordinary PLL, as explained in Chapter 2. As the acquisition process is computationally intensive and time consuming, it is vital that the tracking channels keep a lock on acquired signals. When a lock is established on the visible radionavigation signals, the navigation message is demodulated in order to compute user position, which is carried out in the range-processing unit. Under ideal conditions, i.e. with no interference and multipath, the accuracy of a receiver can be related with the post-correlation C/N_0 as [Mis06]:

$$\sigma_{\Delta\tau}[m] = c \cdot T_{\mathrm{PRN}} \sqrt{\frac{1}{4T_A \cdot \left(C/N_0\right)_{\mathrm{PC}}}} \tag{3.7}$$

where $\sigma_{\Delta\tau}$ is the standard deviation of the ranging error and T_A is the averaging time used by the tracking loop.

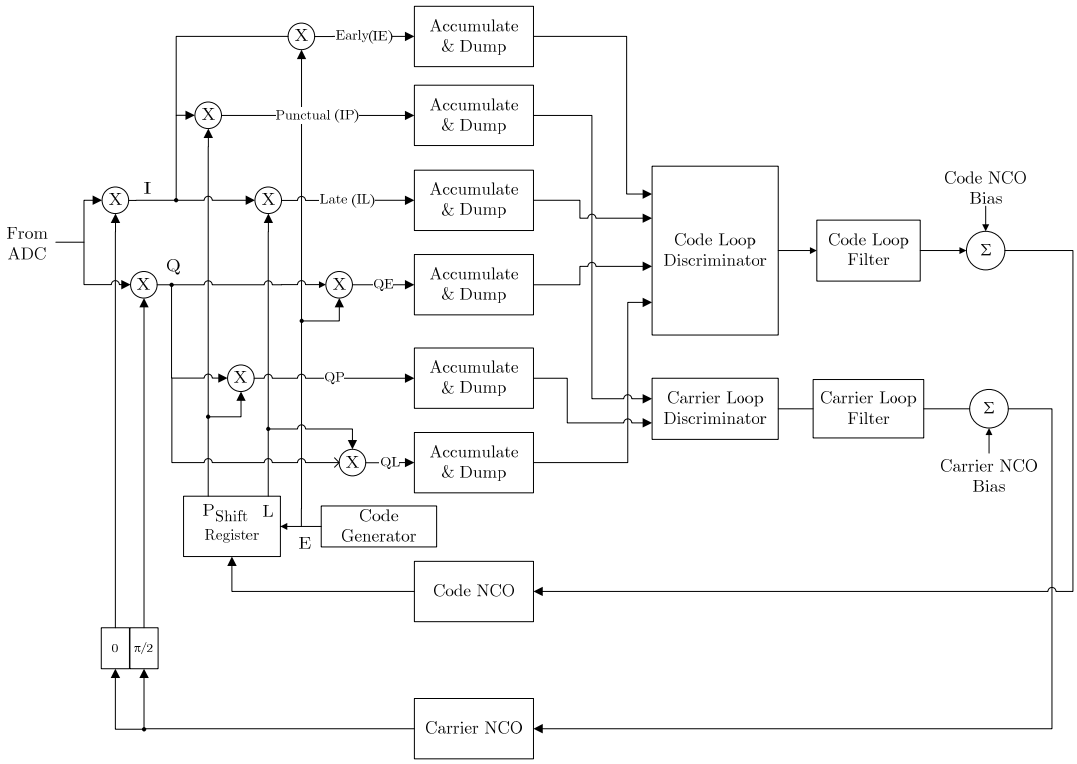


Figure 3-4 DLL and Costas loop for code and carrier tracking with six correlators

3.2 Conventional RF Front-End Topologies

The main difference among the RF front-end topologies is the number of steps required to down-convert the RF signal into baseband. Selectivity[†] and complexity of a receiver generally increases with the number of down-conversions. In a GNSS receiver, the front-end provides an IF signal to the ADC as signal acquisition is generally performed on the digital IF signal. The three most commonly used RF front-end topologies are discussed in this section.

3.2.1 Heterodyne Receiver

The heterodyne receiver [Dou90] has been the most popular topology for commercial receivers as it provides superior sensitivity and selectivity. In

[†] Selectivity is defined as the ability of a receiver to extract the desired signal satisfactorily in the presence of strong interferes and channel blockers

heterodyne receivers, the signal at the output of the antenna is amplified and down-converted to baseband in multiple frequency translation steps. A block diagram of the dual-conversion heterodyne receiver is given in Figure 3-5 [Cet02]. Here, the RF signal at the output of the antenna is first filtered by an RF filter and amplified by a Low-Noise Amplifier (LNA). The function of the RF filter is to suppress the image and the interference. The overall noise figure of the receiver is pretty much set by the first component after the antenna, which is the RF filter in most receivers. The LNA also plays a crucial role in achieving good reception sensitivity. The signal is then passed through an Image-Reject Filter (IRF) before being frequency translated to an Intermediate Frequency (IF) by the first Local Oscillator (LO). The IRF must sufficiently attenuate any undesired signal at the image frequency, f_{IM}, which would otherwise be down-converted to the IF by the mixer, as illustrated in Figure 3-6 [All06].

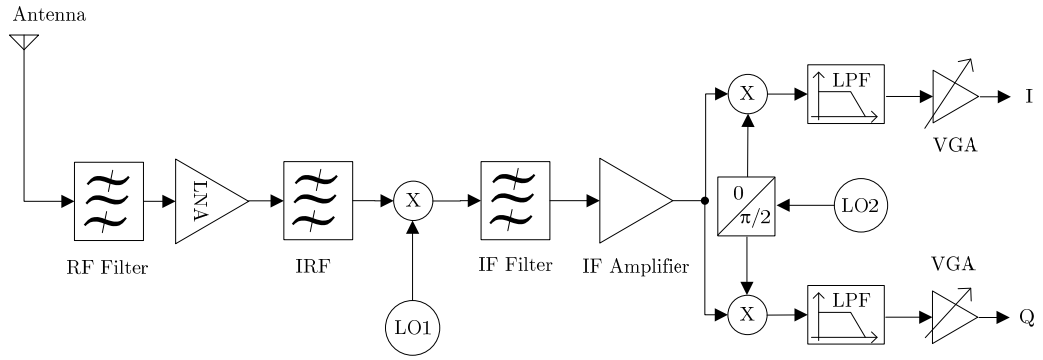


Figure 3-5 Block diagram of the dual-conversion heterodyne receiver

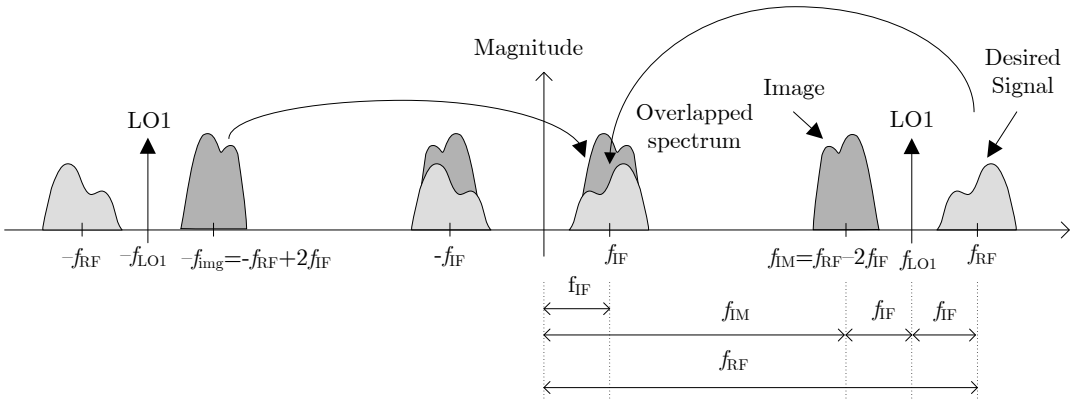


Figure 3-6 Image signal overlapping the desired signal [Cet02]

At the IF stage, the signal is further filtered and amplified before being frequency translated into the baseband. Downconversion to baseband is generally performed by a quadrature mixer to generate I and Q components.

The primary design choice in a heterodyne receiver is the location of IF(s). In a dual-conversion heterodyne receiver, a higher IF leads to a larger separation between the desired signal and the image, which is at $2f_{IF}$. This relaxes the requirements of the RF filter. However, a higher IF requires an IF filter with a higher Q-factor[‡] to suppress the adjacent channel interferers. Therefore, there is a trade-off between the image suppression and channel selection. Dual-IF heterodyne receiver eliminates this trade-off; however, at the expense of introducing additional components [Raz97].

Heterodyne receiver topology for GNSS is slightly different from the classical heterodyne receiver as digital IF signal is needed at the output of the RF front-end. Piazza and Huang [Pia98] reported a triple conversion (IF_1=179MHz, IF_2=4.7MHz, and IF_3=1.05MHz) front-end with a 8.1dB noise figure in 1.0μm Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) technology. Kadoyama et al. [Kad04] reported a dual-conversion (IF_1=2MHz and IF_2=1MHz) front-end with a 4dB noise figure in 0.18μm CMOS. Both receivers utilize single-bit quantization and employ external Surface Acoustic Wave (SAW) RF filters to attenuate strong out-of-band interferers. While SAW filters are passive and provide nearly unlimited dynamic range and a high Q-factor, they hinder integration of the receiver monolithically. The current trend for designing RF filters is to utilize Q-enhancement techniques for LC circuits in CMOS and BiCMOS process technologies to achieve fully-integrated circuit implementations [Soo02], [Xin05], [Dan05]. The obvious disadvantage of superheterodyne receivers is high power consumption and cost due to the relatively large number of components required.

[‡] Q-factor of a circuit in resonance can be defined as the ratio of the maximum instantaneous energy stored in the circuit to the energy being dissipated per cycle, or the ratio of the centre frequency to the –3 dB bandwidth

3.2.2 Zero-IF Receiver

The zero-IF receiver, depicted in Figure 3-7, directly converts the RF signal at the output of the antenna to baseband, which eliminates the need for image suppression. This greatly simplifies the receiver design as the entire IF stage is eliminated. However, direct translation from RF to DC leads to two significant problems. First, DC offsets originated from LO self-mixing[†] and even-order harmonic distortion might saturate the baseband analog circuits and, if uncorrected, cause signal degradation [Raz97], [Cet02]. Second, flicker noise component can be relativity large near DC to corrupt the desired signal. This is a significant problem as most of the signal energy in BPSK/QPSK-modulated GNSS signals is concentrated at DC. Lim et al. [Lim06] reported a zero-IF receiver for GPS and CDMA applications in 0.35μm BiCMOS process technology. The receiver does not comprise an RF filter and achieves a noise figure of 1.7dB.

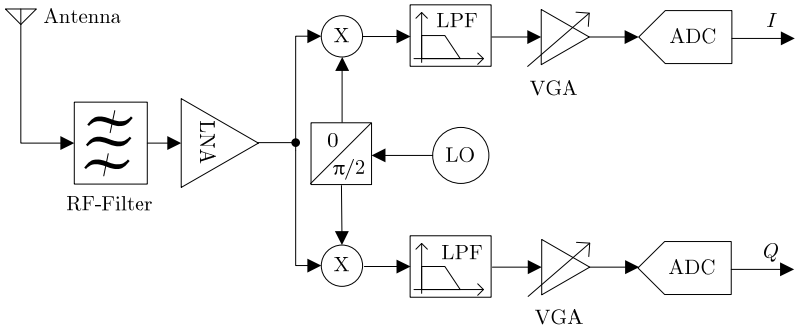


Figure 3-7 Block diagram of the zero-IF receiver

3.2.3 Low-IF Receiver

Low-IF receivers utilize quadrature mixers to down-convert the RF signal to an IF, typically within a few hundred kHz to a few MHz, in order to avoid problems associated with DC offsets and flicker noise. The low-IF topology employing a complex filter is given in Figure 3-8 [Cro98].

[†] LO self-mixing occurs when the LO signal radiates through the mixer input to mix with itself creating a DC component

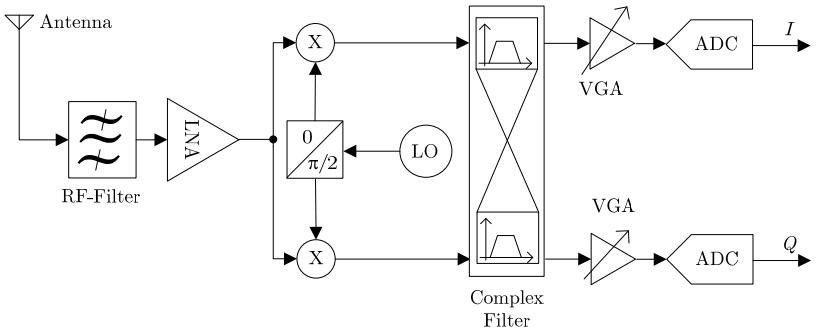


Figure 3-8 The low-IF receiver with a complex filter

As the signal is down-converted to an IF, low-IF receivers are also prone to the image problem. Additionally, the quadrature mixers suffer from analog impairments such as gain and phase imbalances in the I and Q paths of the receiver [Cet01], [Val01]. Sources of these imbalances are the RF splitter used to divide incoming RF signal between the I and Q paths, the differences in the length of the two paths, and the imperfections in the quadrature phase splitter. The I/Q imbalance can be modelled as a leaked LO which leads to image interference at the IF as illustrated in Figure 3-9.

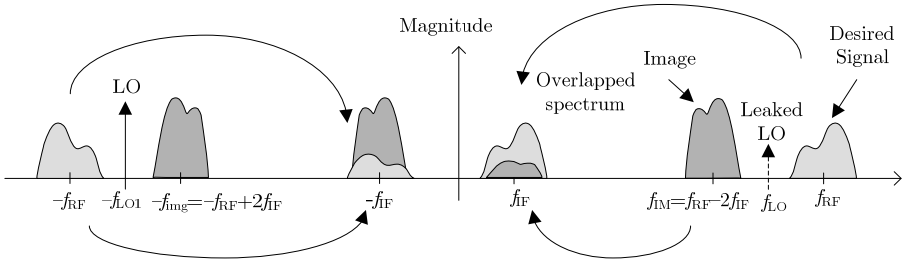


Figure 3-9 The effect of I/Q imbalance in a low-IF receiver

In Low-IF receivers, a complex filter can be employed to achieve a frequency response that is not symmetrical around DC in order to eliminate the undesired components in the signal spectra. The complex filter can be realized either by frequency shifting a LowPass Filter (LPF) into complex band-pass or by employing a direct synthesis with complex summers, amplifiers, and integrators for deriving the complex transfer function [Mar04]. Mismatches in the complex filter also corrupt the signal, as illustrated in Figure 3-10 [Mat06], [Uca08a]. An adaptive algorithm to mitigate the effects of I/Q imbalances in the DSP domain was proposed in [Cet01]. The method was later applied by the author to mitigate the effects of both I/Q imbalances

and the complex filter mismatches of a low-IF GPS L1 receiver. It was shown that the image rejection performance could be enhanced by 75dB [Uca08a].

Low-IF topology has been an attractive choice for the civilian GPS L1 receivers due to the relatively narrow bandwidth of the C/A code. Shaeffer et al. reported the implementation of a low-IF receiver with 2.8dB noise figure in 0.5μm CMOS technology, which employs off-chip RF filtering [Sha98]. The receiver employs single-bit quantization and achieves 17dB post-correlation SNR. The 0.35μm CMOS implementation reported by Behbahani employs a 5^{th}-order elliptic complex filter with single-bit quantization to achieve 4dB noise figure [Beh02]. Gramegna et al. reported a System-on-Chip (SoC) GPS L1 receiver with a noise figure of 4.8dB in 0.18μm CMOS process [Gra06]. It also comprises an off-chip RF filter and employs single-bit quantization.

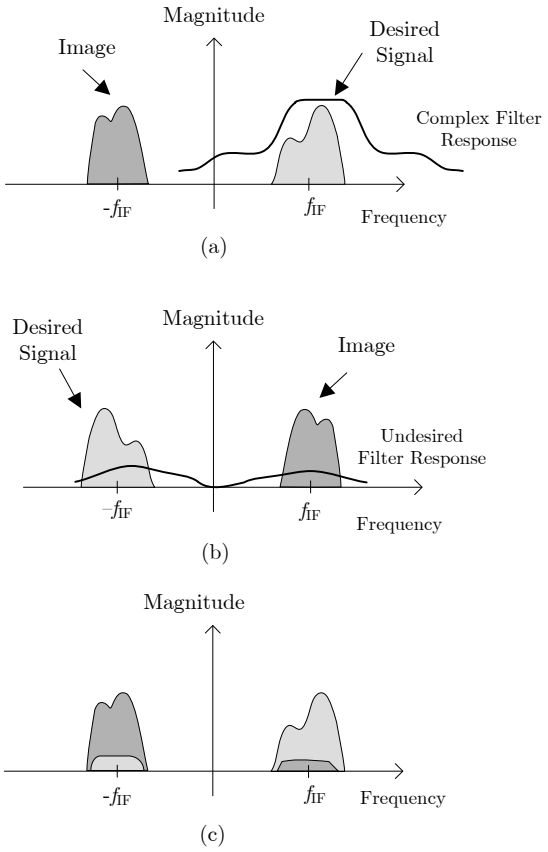


Figure 3-10 The effect of complex filter mismatch in a low-IF receiver (a) Complex filter response on the input spectrum (b) Undesired filter response due to the filter mismatches on the complex conjugate of the input spectrum (c) Resulting signal spectrum

3.3 Subsampling Receiver

The realization of multi-band receivers with conventional receiver topologies put stringent requirements on either the RF front-end or the ADC. Sampling at IF in a multi-carrier receiver requires multiple IF filters and amplifiers and high-speed frequency synthesizers, which increases the cost, the size, and the power dissipation of the front-end. Alternatively, providing direct RF sampling at Nyquist rate in an effort to minimize the number of analog components would increase the power dissipation of the ADC as well as the noise figure of the receiver due to sampling jitter.

Multi-band capability in a receiver can be achieved with lower power and cost by employing subsampling (also known as band-pass sampling or undersampling) at RF. Subsampling achieves frequency translation via intentional aliasing. This enables shifting the IF stage into the digital domain thereby eliminating the need for analog mixers and IF analog filters, consequently minimizing the signal distortion caused by the analog impairments [Uca08b]. The RF front-end of a subsampling receiver, as illustrated in Figure 3-11, can be implemented with minimal number of analog components and with an IF frequency synthesizer. Additional miniaturization can be achieved when the I and Q paths are eliminated.

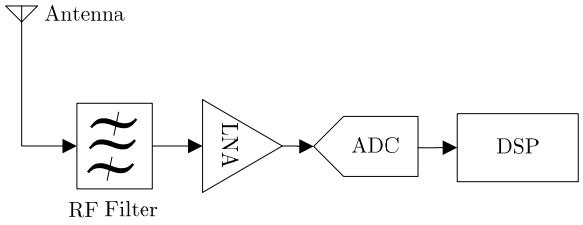


Figure 3-11 Subsampling receiver topology

Despite all the advantages, the use of subsampling receivers in wireless communication systems has been limited due to several issues. First, the sampling rate has to be chosen carefully in order to avoid destructive aliasing especially in multi-carrier receivers where a limited set of sampling rates are available to the receiver. Second, down-converting the RF signal to an IF by employing subsampling results in a poorer SNR than that from performing

downconversion with an analog mixer [Vau91]. Finally, the jitter noise power is higher in a subsampling receiver than that of a receiver performing sampling at IF as the input signal frequency is at RF.

3.3.1 Sampling Rate Selection

Let a CT signal with a centre frequency f_0 be band-limited from f_L to f_U, as shown in Figure 3-12. The subsampling theory states that the signal can be reconstructed from its samples if it is uniformly sampled with a sampling rate satisfying the conditions [Vau91]:

$$\frac{2f_U}{n} \le f_S \le \frac{2f_L}{n-1} \text{ and } f_S \ge 2\Delta f \tag{3.8}$$

where n is an integer given by:

$$1 \le n \le \left\lfloor \frac{f_U}{\Delta f} \right\rfloor \tag{3.9}$$

The notation $\lfloor . \rfloor$ denotes the largest integer. Notice that, in LowPass Sampling (LPS), n=1 and $f_S \ge 2f_U$. With an ideal sampler, the sampled signal will have aliases located at:

$$f_A = \pm f_0 \pm kf_S \tag{3.10}$$

where k=1,2,... is the index of the aliases.

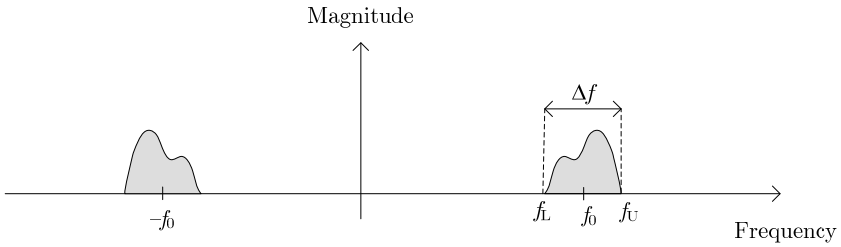


Figure 3-12 Spectrum of the band-limited CT signal

When multi-carrier signals are subsampled simultaneously, the sampling rate must be chosen carefully to avoid spectral overlap between signal aliases. In this case, the alias ladder diagram can be used to determine the suitable

sampling rates [Ako97]. For the civilian multi-constellation GNSS receiver, the signals of interest for this Ph.D. study are given in Table 3-2. The alias ladder diagram for the relevant signals is plotted in Figure 3-13 assuming that the RF front-end provides perfect filtering on the signals over their respective null-to-null bandwidths as given in Table 3-2. In Figure 3-13, L1 C/A and E1 OS share the carrier frequency; therefore, they are assumed to be in the same band (denoted L1-E1 in the figure) having a bandwidth equal to the widest signal of the two. This also applies to L5 and E5a. The alias ladder gives the location of the aliases of the relevant signals in the first Nyquist zone. As can be observed, there is no spectral overlap between the signals at 111Msps (mega samples per second), which can be considered as the minimum sampling rate for simultaneous processing of the signals of interest.

Table 3-2 Civilian GPS/Galileo signals

	Carrier [MHz]	Bandwidth [MHz]
L1 C/A	1575.42	2.046
L2C	1227.60	2.046
L5	1176.45	20.46
E1 OS	1575.42	16.368
E5a	1176.45	20.46

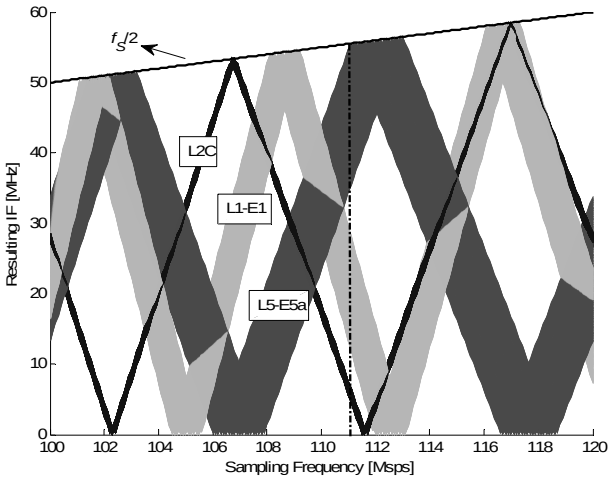


Figure 3-13 The alias ladder diagram for the civilian GPS/Galileo signals

3.3.2 Noise Aliasing

Noise aliasing is a phenomenon that is present regardless of the sampling rate; however, SNR degradation due to noise aliasing is more severe in subsampling receivers [Vau91], [Eri99], [Pek06]. There are three types of noise present in the CT signal spectrum of a receiver:

- Thermal noise has a flat PSD and originates from the random currents due to Brownian motion of electrons [Qiz05]
- Flicker noise has a PSD inversely proportional with frequency. Its origin is not well understood; however, it is thought to be related with the imperfections in the crystalline structure of the semiconductors [Car09]
- Shot (Schottky) noise has a flat PSD and is caused by random fluctuations in the motion of charge carriers in a conductor

In addition to these, timing error during sampling also increases the noise floor of the sampled signal as explained in Section 3.3.3. Even if an AA filter eliminates all the out-of-band noise present prior to sampling, the noise generated within the sampler would still degrade the SNR of the sampled signal.

A simple S/H circuit, depicted in Figure 3-14, can be used to analyze noise aliasing phenomenon. In such a circuit, when the sampling switch is closed (sampling phase), the CT input voltage is charged onto the sampling capacitor, C, through the switch. The resistance of the switch, R, and the sampling capacitor construct a LPF with a transfer function given as [Pla03]:

$$H(f) = \frac{1}{1 + j2\pi fRC} \tag{3.11}$$

with the –3dB bandwidth:

$$\Delta f_{\text{S/H}} = \frac{1}{2\pi RC} \tag{3.12}$$

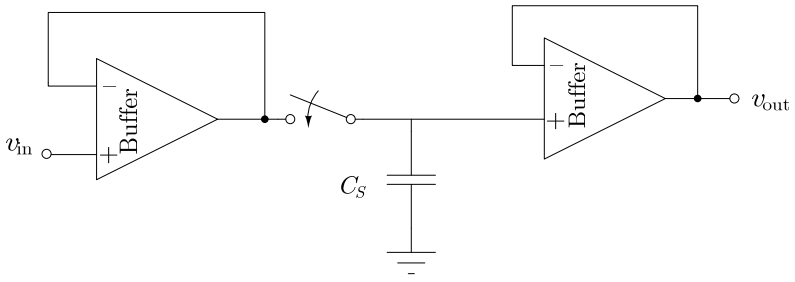


Figure 3-14 A simple S/H circuit [Nat95]

The dominant contributor of noise is the thermal noise of the resistance, which has the PSD $4k_BT_0R$. This will appear at the output of the S/H after being shaped by the LPF. The two-sided PSD of the shaped noise can be written as:

$$S_{\text{SAMPLE}}\left(f\right) = 2Dk_BT_0R\left|\frac{1}{1+j2\pi fRC}\right|^2 = \frac{2Dk_BT_0R}{1+\left(2\pi fRC\right)^2} \tag{3.13}$$

where $0<D<1$ is the duty cycle of the sampling clock. The mean square power of $S_{\text{SAMPLE}}(f)$ for all frequencies can be obtained as:

$$P_{\text{SAMPLE}} = \int_{-\infty}^{\infty} S_{\text{SAMPLE}}\left(f\right)df = D\frac{k_BT_0}{C} \tag{3.14}$$

The shaped noise at the output of the S/H amplifier when the switch is closed can be modelled as a noise source with a flat PSD and an effective bandwidth:

$$\Delta f_E = \int_{-\infty}^{\infty}\left|H\left(f\right)\right|^2 df = \frac{1}{2RC} \tag{3.15}$$

as illustrated in Figure 3-15. When the switch is open (hold phase), C holds the instantaneous value of the input voltage as well as the noise introduced by the resistance of the switch. The PSD of noise during the hold phase can be expressed as [Gre86]:

$$S_{\text{HOLD}}\left(f\right) = \left(1-D\right)^2\,\text{sinc}^2\left(\left(1-D\right)Tf\right)\sum_{k=-\infty}^{\infty} S_{\text{SAMPLE}}\left(f-kf_S\right) \tag{3.16}$$

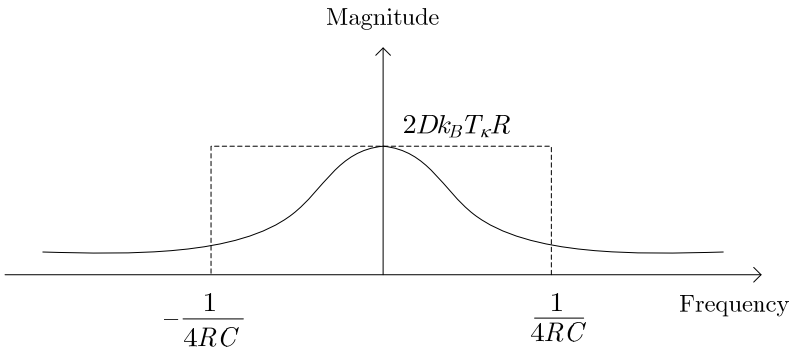


Figure 3-15 Effective noise bandwidth of the S/H amplifier

where $T=1/f_S$ is the sampling period. Using the flat PSD model, the summation in Equation (3.16) can be expressed as:

$$\sum_{k=-\infty}^{\infty} S_{\text{SAMPLE}}\left(f - kf_S\right) = \frac{\Delta f_E}{f_S} S_{\text{SAMPLE}}\left(f\right) \tag{3.17}$$

Assuming the noise introduced during the sampling phase is uncorrelated with that introduced during the hold phase and D=1/2, the overall noise PSD at the output of the S/H is:

$$S_{\text{S/H}}\left(f\right) = S_{\text{SAMPLE}}\left(f\right)\left(1 + \frac{1}{4} m \,\text{sinc}^2\left(\frac{T}{2} f\right)\right) \tag{3.18}$$

where m is the noise aliasing ratio (also known as the noise folding ratio), which is simply the number of f_S bands within $(-\Delta f_E/2, \Delta f_E/2)$:

$$m \triangleq \left\lfloor \frac{\Delta f_E}{f_S} \right\rfloor \tag{3.19}$$

In a receiver employing LPS (i.e. a down-conversion mixer followed by a LPF and a S/H), charging time constant is generally 10 times lower than the duration of the sampling phase [Gre86], [Mal07]:

$$DT \geq 10RC \rightarrow \frac{1}{10RC} \geq 2f_S, \;\; \frac{1}{2RC} = \Delta f_E \geq 10 f_S \tag{3.20}$$

On the other hand, Equation (3.20) is not necessarily valid in a subsampling receiver employing the same sampling rate since –3dB bandwidth of the S/H amplifier must be wide enough to pass the analog input signal:

$$\Delta f_{\mathrm{S/H}} = \frac{1}{2\pi RC} \geq f_U \rightarrow \frac{1}{2RC} = \Delta f_E \geq \pi f_U \tag{3.21}$$

Therefore, it can be concluded that the resulting SNR in a subsampling system is most likely to be poorer than an equivalent LPS system as illustrated in Figure 3-16. For a fixed sampling rate, the SNR degradation in a subsampling receiver increases as the highest frequency component of the RF signal increases.

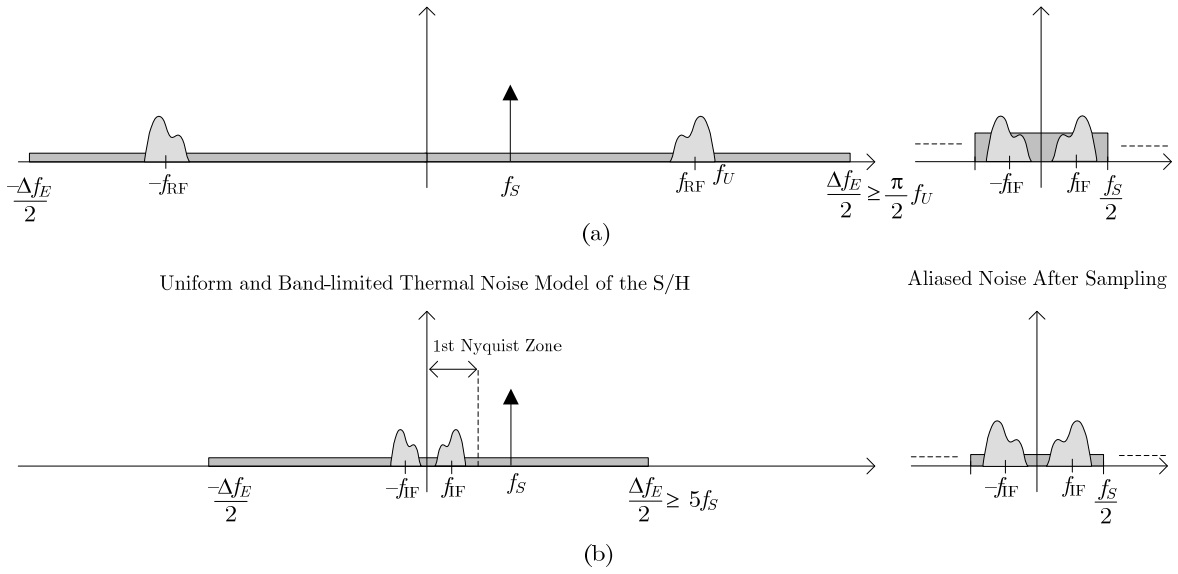


Figure 3-16 Noise aliasing in a (a) Subsampling receiver (b) LPS receiver

3.3.3 Jitter

Jitter is defined as the deviation in the nominal value of the sampling instants. There are two contributors of jitter in S/H amplifiers. Clock jitter is due to the phase noise of the Voltage-Controlled Oscillator (VCO) that feeds the S/H amplifier. Aperture jitter is the unpredictable delay between the logic that generates the sampling phase and the effective sampling time, which is due to the noise contributed by the clock regeneration and distribution circuit in the S/H [Mal07], [Zan08]. Jitter is often specified as a Root Mean Square (RMS) value, which represents the standard deviation in the sampling time [Nat95]. Phase noise can be related with RMS jitter as described in Section 5.3.2. Assuming no correlation exists between the clock jitter and the aperture jitter, the total jitter in a S/H can be written as [Kes05]:

$$\sigma_J = \sqrt{\sigma_{\mathrm{CJ}}^2 + \sigma_{\mathrm{AJ}}^2} \tag{3.22}$$

where σ_{CJ}^2 and σ_{AJ}^2 are the variance of the timing error due to the clock and aperture jitter, respectively.

Let the jittered sampling instants provided by a sampler be

$$t_n = nT + \Delta T\left(n\right), n = 0,1,2,\ldots \tag{3.23}$$

where T=1/f_{S} is the sampling time and $\triangle T(n)$ is the independent identically distributed (i.i.d.) jitter random variable for the n^{th} sampling instant. The dominant contributor of noise is the aperture jitter, which is generally modelled as a white noise source by assuming that each random variable has zero-mean and a Gaussian PDF [Awa98], [Loh03]. When a signal $x(t)$ is applied, the timing error introduced at the output of the S/H can be written as:

$$\varepsilon_t(n) = x(t + \Delta T) - x(t) \tag{3.24}$$

The jitter "noise" power can be related with the timing error as:

$$P_J = E\left\{\varepsilon_t^2(n) - \varepsilon_t(n)\right\}^2 = E\left\{\varepsilon_t^2(n)\right\} \tag{3.25}$$

For a sinusoidal input signal, $A{\cdot}\sin(2\pi f_0 t)$, the jitter noise power is derived to be [Shi90], [Awa98]:

$$P_J = \begin{cases} \sigma_J^2\left(A \cdot 2\pi f_0\right)^2, \sigma_J 2\pi f_0 \ll 1 \\ A^2\left(1 - e^{-\sigma_J^2\left(2\pi f_0\right)^2}\right), \text{otherwise} \end{cases} \tag{3.26}$$

Equation (3.26) indicates that the jitter noise power increases with the input frequency. Therefore, the SNR degradation is more severe in subsampling receivers as the input signal to the S/H is at RF. It must be noted that the wideband jitter noise aliases into each f_S band as a result of subsampling.

Dempster and Amin applied the analysis presented in [Shi90] to derive the jitter noise power of BPSK, QPSK and BOC modulated signals [Dem05],

[Ami07]. By assuming $\sigma_J 2\pi f_0 \ll 1$, the jitter noise power of the relevant signals are derived as:

$$P_{J,\mathrm{BPSK}} = P_{J,\mathrm{QPSK}} \approx A^2 \left(\sqrt{\frac{2}{\pi}} \frac{\sigma_{\Delta T}}{T_{\mathrm{PRN}}} + \frac{\sigma_{\Delta T}^2 \left(2\pi f_0\right)^2}{2} \right) \tag{3.27}$$

$$P_{J,\mathrm{BOC}_S(a,a)} = A^2 \left(3\sqrt{\frac{2}{\pi}} \frac{\sigma_{\Delta T}}{T_{\mathrm{PRN}}} + \frac{\sigma_{\Delta T}^2 \left(2\pi f_0\right)^2}{2} \right) \tag{3.28}$$

$$\begin{aligned} P_{J,\mathrm{CBOC(6,1,1/11)}} &= \frac{10}{11} P_{J,\mathrm{BOC(1,1)}} + \frac{1}{11} P_{J,\mathrm{CBOC(6,1)}} \\ &= A^2 \left(\frac{53}{11} \sqrt{\frac{2}{\pi}} \frac{\sigma_{\Delta T}}{T_{\mathrm{PRN}}} + \frac{\sigma_{\Delta T}^2 \left(2\pi f_0\right)^2}{2} \right) \end{aligned} \tag{3.29}$$

$$P_{J,\mathrm{AltBOC}} = 2A^2 \left(5\sqrt{\frac{2}{\pi}} \frac{\sigma_{\Delta T}}{T_{\mathrm{PRN}}} + \frac{\sigma_{\Delta T}^2 \left(2\pi f_0\right)^2}{2} \right) \tag{3.30}$$

Equations (3.27) to (3.30) indicate that jitter noise power increases with the chipping rate. This is expected as higher chipping rates increase the frequency of zero-crossings in the modulated signal, which results in larger timing errors.

3.4 Subsampling S/H Amplifiers

Reported noise figures of integrated subsampling S/H amplifiers (also known as subsampling mixers) are as high as 47dB, as given in Table 3-3. Noise figure of a device can be defined as [Bra08]:

$$\mathrm{NF} \triangleq \mathrm{SNR}_{\mathrm{IN}} - \mathrm{SNR}_{\mathrm{OUT}} \tag{3.31}$$

where $\mathrm{SNR}_{\mathrm{IN}}$ is the SNR at the input, $\mathrm{SNR}_{\mathrm{OUT}}$ is the SNR at the output of the device. Assuming the S/H amplifier is just a buffer; the noise figure of the S/H can be written as:

Table 3-3 Noise figure comparison of subsampling S/H amplifiers

	Technology	Bandwidth [MHz]	Sampling Rate [Msps]	NF [dB]
[She96]	0.6μm CMOS	910	78	47
[Par97]	0.6μm GaAs	1,600	100	29
[Vas99]	0.6μm CMOS	900	1	20
[Jak03]	0.35μm CMOS	1,600	1,550	25
[Pek05]	0.18μm CMOS	2,400	100	21.8

$$\begin{aligned} \mathrm{NF}_{\mathrm{S/H}} &= \left(P_{S,\mathrm{IN}} - P_{N,\mathrm{IN}}\right) - \left(P_{S,\mathrm{OUT}} - P_{N,\mathrm{OUT}}\right) \\ &= P_{N,\mathrm{OUT}} - P_{N,\mathrm{IN}} \end{aligned} \tag{3.32}$$

where $\mathrm{P}_{S,\mathrm{IN}}$ is the input signal power, $P_{S,\mathrm{OUT}}$ is the output signal power, $P_{N,\mathrm{IN}}$ is the input noise power, and $P_{N,\mathrm{OUT}}$ is the output noise power, all in dBs. Therefore, a higher noise figure in the S/H results in a higher noise floor, which reduces the dynamic range of the ADC. It can be concluded that, an ADC employing subsampling require a higher dynamic range than an ADC employing LPS. Noise aliasing is especially a concern in GNSS receivers as the thermal noise floor is approximately 30dB above the signal of interest at the input of the ADC. Employing subsampling in a GNSS receiver might result in the saturation of the ADC if the dynamic range requirement is not carefully determined. The dynamic range of an ideal ADC can be written as [Ort06]:

$$\mathrm{DR}_{\mathrm{ADC}}[\mathrm{dB}] = 6.02 \cdot b + 1.76 + 10\log_{10}(\mathrm{OSR}) \tag{3.33}$$

where b is the number of bits. Equation (3.33) suggests that the dynamic range can be enhanced by either increasing the OverSampling Ratio (OSR) or the number of bits. Both result in increased complexity and power dissipation.

Traditionally, ΔΣ ADCs have been an attractive choice for digitizing narrowband signals when a high-resolution is required [Azi96]. Nevertheless, based on the analysis presented in this chapter, employing A/D conversion in a subsampling GNSS receiver with a CT-ΔΣ ADC, as depicted in Figure 3-17, could lead to a reduced-complexity solution. This reasoning is based on three aspects of CT-ΔΣ modulators [Uca08b]:

- As sampling is performed inside the feedback loop of the modulator, noise introduced by the sampler is shaped away by the Noise Transfer Function (NTF) of the modulator
- An AA filter may not be required as the Signal Transfer Function (SFT) of the modulator provides inherent AA filtering on the input signal path
- CT-ΔΣ ADCs are suitable for high speed, wide bandwidth, and low power applications

NTF and STF of a first order low-pass CT-ΔΣ modulator are illustrated in Figure 3-18. Despite the noise-shaping property, conventional CT-ΔΣ modulators are not suitable for subsampling A/D conversion as outlined in Chapter 1. Chapter 5 introduces a novel CT-ΔΣ modulator that is capable of compensating for the problems associated with subsampling in ΔΣ modulators.

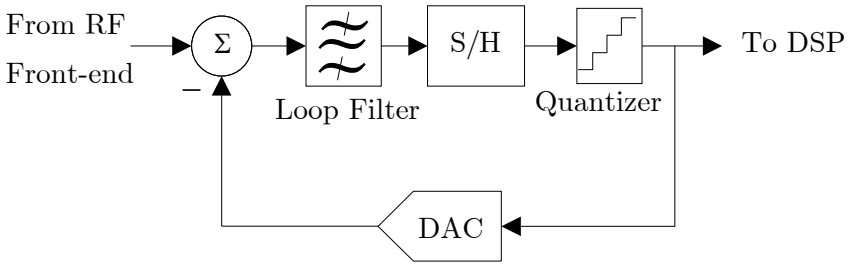


Figure 3-17 Block diagram of a conventional CT-ΔΣ modulator

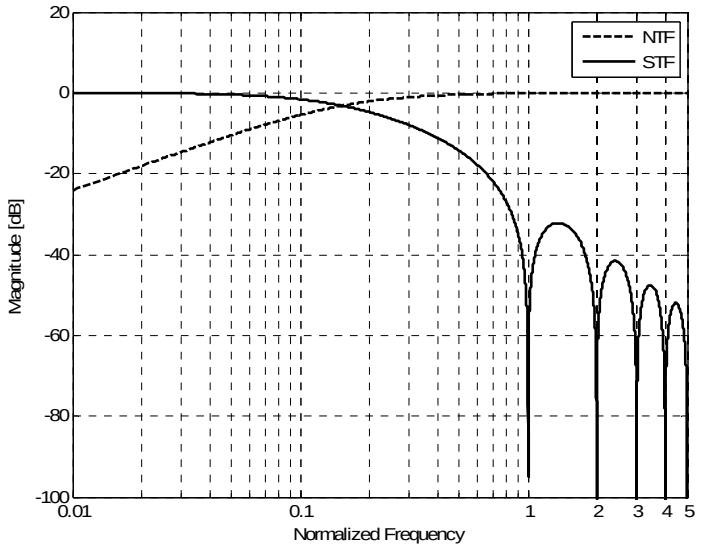


Figure 3-18 NTF and STF of the first-order low-pass CT-ΔΣ modulator

Chapter 4

Delta-Sigma Modulators – An Overview

Oversampling and noise-shaping using first and second-order loops were first introduced in 1952 by C.C. Cutler [Cut52]; however, the name "ΔΣ Modulation" was first mentioned by Inose et al. [Ino62] since the concept was based on delta modulation with integration. The basic idea was modulating the analog input into a bit stream with a spectrum that approximates that of the input in a narrow frequency range and shaping away the quantization noise from this range [Che98]. Data conversion by means of ΔΣ modulation had not received much attention until the 1980s since IC technologies were expensive. As IC technologies improved, ΔΣ data converters became an attractive choice for high-resolution, low/medium speed applications. This chapter provides an overview of ΔΣ modulators with an emphasis on the theory and practical implementation of CT-ΔΣ modulators.

4.1 Quantization and Oversampling

ΔΣ modulators can be realized with DT or CT circuitry. A typical DT-ΔΣ ADC, as depicted in Figure 4-1, consists of [Med99]:

- An AA filter for band-limiting the input spectrum
- A S/H amplifier for sampling the CT input signal at a rate higher than the Nyquist rate
- A ΔΣ modulator for performing noise shaping on the oversampled signal
- A decimator for lowering the sampling rate of the signal to reduce the complexity of further digital signal processing

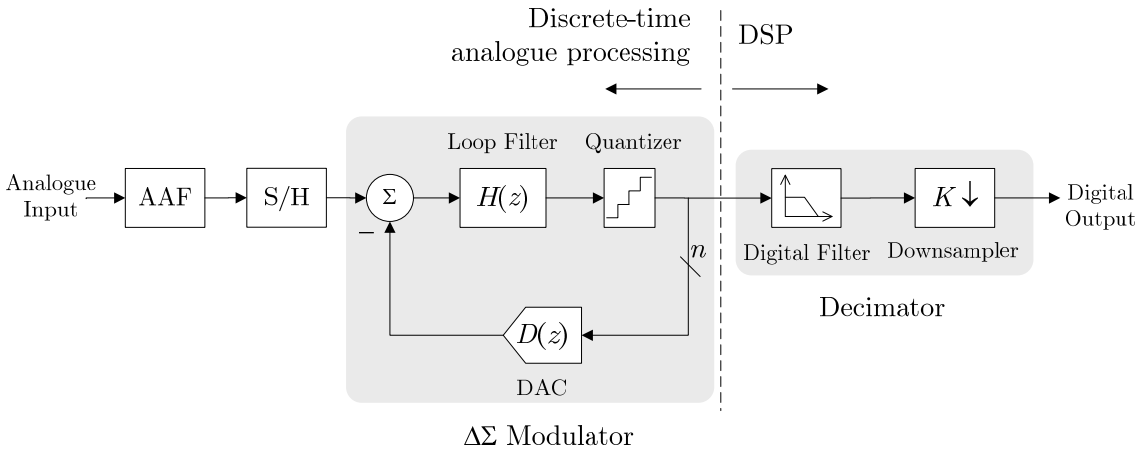


Figure 4-1 Discrete-time ΔΣ ADC

The block diagram of the first-order single-loop DT-ΔΣ modulator is illustrated in Figure 4-2(a). It comprises a DT loop filter, a low-resolution quantizer (typically single-bit), and a Digital-to-Analog Converter (DAC) in the feedback loop. The quantizer is a nonlinear circuit, which makes it difficult to analyze the overall behaviour of ΔΣ modulators. The additive white noise representation of the quantizer leads to the linearized model of the ΔΣ modulator, as illustrated in Figure 4-2(b). The linearized model simplifies the analysis since the deterministic nonlinear system is replaced by a stochastic linear system [Sch04]. The conditions for the white noise approximation (also known as Bennett's Conditions) can be summarized as follows [Ben48]:

- The input is never in the overload region of the quantizer
- The quantizer has asymptotically large number of quantization levels.
- The quantization step size Δ is asymptotically small.
- The joint PDF of the input signal at different sample times is smooth

When the Bennett's Conditions hold, the quantization error sequence has the following properties [Nor97]:

- The PDF of the quantization error sequence, $q(n)$, is uniform and approximately equal to $1/\Delta$[†] over the range [-Δ/2,Δ/2]
- The quantization error sequence is approximately an i.i.d. sequence

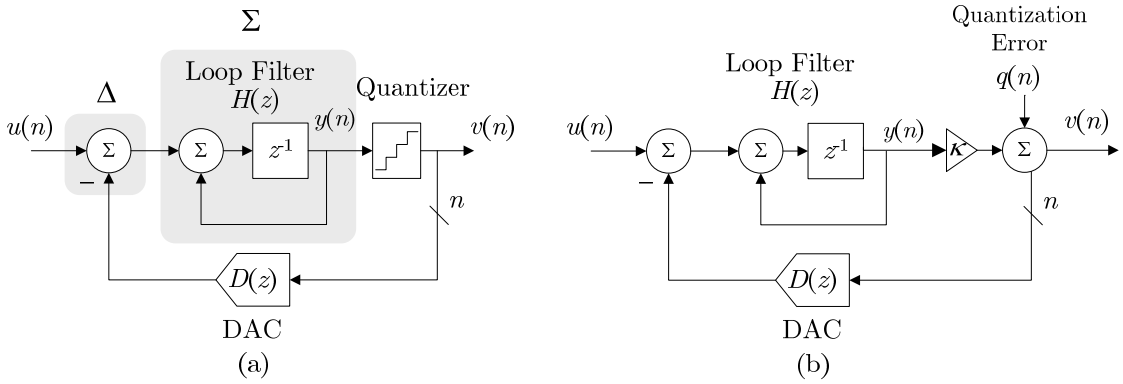


Figure 4-2 (a) Basic components of the first-order ΔΣ modulator (b) Linearized model of the modulator

Although conditions for the white noise approximation are not rigorously met, higher order ΔΣ modulators often exhibits quantization noise that appears to be approximately white [Koz03]. The mean square quantization noise power is the variance of the quantization noise, which can be derived as:

$$P_Q = \sigma_Q^2 = \int_{-\infty}^{\infty} q^2 \frac{1}{\Delta} dq = \int_{-\Delta/2}^{\Delta/2} q^2 \frac{1}{\Delta} dq = \frac{\Delta^2}{12} \tag{4.1}$$

[†] Δ=FSR/($2^{\#\text{ of bits}}$–1) is the quantization step size, where FSR is the Full-Scale Range of the quantizer

The in-band quantization noise power can be reduced by increasing the sampling frequency above the Nyquist rate, resulting in oversampling. The PSD of the oversampled noise power is given by:

$$S_Q\left(f\right) = \frac{\sigma_Q^2}{f_S} = \frac{\Delta^2}{12 f_S} \tag{4.2}$$

The in-band mean square quantization noise power for an oversampled converter is then calculated as:

$$P_{Q,\mathrm{INB}} = \sigma_{Q,\mathrm{INB}}^2 = \int_{-\Delta f}^{\Delta f} S_Q\left(f\right) df = \frac{\Delta^2 \cdot 2\Delta f}{12 f_S} = \frac{\sigma_Q^2}{\mathrm{OSR}} \tag{4.3}$$

where Δf is the single-sided signal bandwidth. The equation describing the linearized model of the modulator is given as [Sch04]:

$$V\left(z\right) = \left[U\left(z\right) - V\left(z\right) D\left(z\right)\right] \times \kappa H\left(z\right) + Q\left(z\right) \tag{4.4}$$

where κ is the quantizer gain. Assuming $D(z)=1$, Equation (4.4) can be written as

$$V\left(z\right) = \frac{1}{\frac{1}{\kappa H(z)} + 1} \cdot U\left(z\right) + \frac{1}{\kappa H(z) + 1} \cdot Q\left(z\right) \tag{4.5}$$

Equation (4.5) shows that the input signal and the quantization noise pass through two different transfer functions called the Signal Transfer Function (STF) and the Noise Transfer Function (NTF). Hence, Equation (4.5) can be written as:

$$V\left(z\right) = \mathrm{STF}(z) \cdot U\left(z\right) + \mathrm{NTF}(z) \cdot Q\left(z\right) \tag{4.6}$$

For the first-order DT-ΔΣ modulator, $\mathrm{STF}(z)=z^{-1}$ and $\mathrm{NTF}(z)=(1-z^{-1})/\kappa$. The input signal is only delayed by one clock cycle at the output without any attenuation since $|\mathrm{STF}(z)|=1$ while the quantization noise is high-pass filtered by the NTF:

$$\mathrm{NTF}(z \to e^{j2\pi\nu}) = \frac{1 - e^{-j2\pi\nu}}{\kappa} = \frac{2je^{-j\pi\nu}}{\kappa}\sin\left(\pi\nu\right) \tag{4.7}$$

where $\nu = f/f_S$ is the normalized frequency. The SFT and NTF of the first-order modulator are depicted in Figure 4-3.

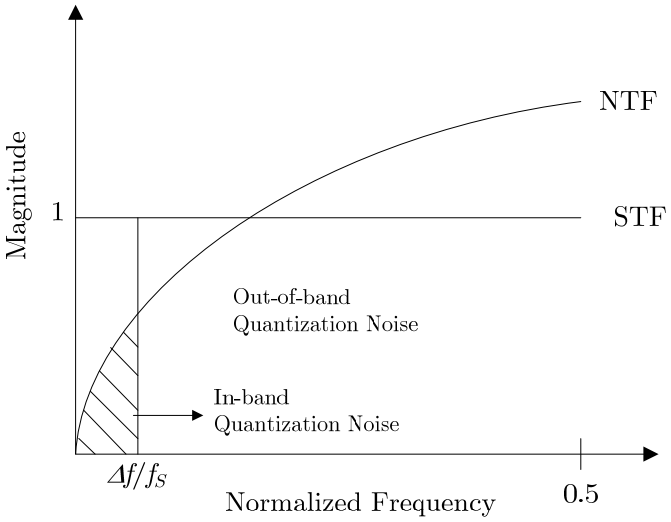


Figure 4-3 STF and NTF of the first-order ΔΣ modulator

The shaped PSD of the quantization noise at the output of the first-order modulator is:

$$S_{Q,\Delta\Sigma 1}\left(f\right) = S_Q\left(f\right)\left|1 - e^{-j2\pi\nu}\right|^2 = S_Q\left(f\right)\frac{4}{\kappa^2}\sin^2\left(\pi\nu\right) \tag{4.8}$$

The in-band quantization noise power can be calculated by approximating the sine function for large OSR as $\sin(\pi\nu) \approx \pi\nu$ [Mal07]:

$$P_{Q,\mathrm{INB},\Delta\Sigma 1} = \int_{-\Delta f}^{\Delta f} \frac{\Delta^2}{12 f_S} \times \frac{4}{\kappa^2}\sin^2\left(\frac{\pi f}{f_S}\right) df \approx \frac{\Delta^2\pi^2}{36\kappa^2\mathrm{OSR}^3} \tag{4.9}$$

From Equations (4.1) and (4.9), the SNR of the modulator can derived as [Zhu07]:

$$\mathrm{SNR}_{\Delta\Sigma,1} \approx 10\log\left(\sigma_S^2\right) - 10\log\left(\sigma_Q^2\right) - 10\log 10\left(\frac{\pi^2}{3\kappa^2}\right) + 30\log 10\left(\mathrm{OSR}\right) \tag{4.10}$$

where σ_S^2 is the variance of the input signal. Therefore, every doubling of OSR increases the SNR by 9 dB, which is 3 times better than the ordinary oversampling ADC.

4.2 Higher Order Modulators and Stability

To further improve the SNR, higher order modulators can be utilized. An Nth order linearized model of the modulator can be defined as:

$$\mathrm{STF}(z) = \left(z^{-1}\right)^N, \quad \mathrm{NTF}(z) = \left(1 - z^{-1}\right)^N \tag{4.11}$$

The magnitude responses of the NTFs with N values up to four are illustrated in Figure 4-4. As can be observed, higher values of N give better noise shaping performance. It must be noted that, the noise-shaping performance shown in Figure 4-4 cannot be achieved in practice due to two reasons:

- The analysis given here is based on the linearized model of the quantizer
- Circuit non-idealities degrade the noise-shaping performance

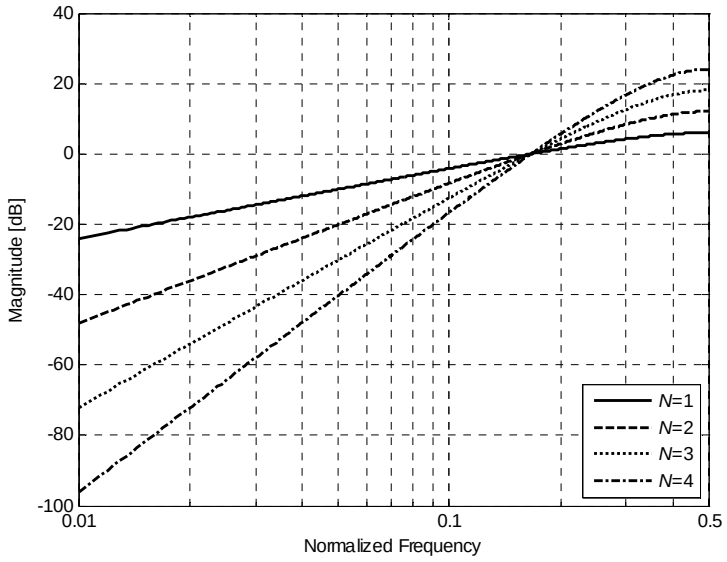


Figure 4-4 NTF of the N-th order ΔΣ modulator with N=1,2,3, and 4

The output of the quantizer in Figure 4-2(b) can be written as:

$$v(n) = k_Q \times q(n) + q(n) \tag{4.12}$$

When $y(n)$ is within the range of [–FSR/2,FSR/2], $q(n)$ is bounded by the range [-Δ/2,Δ/2]. Quantizer inputs beyond ±FSR/2 result in monotonously increasing quantization error. This is known as the quantizer overload. In a stable ΔΣ modulator, all internal state variables, which are the integrator outputs, remain bounded over time [Ris94]. Quantizer overload limits the amount of negative feedback available to the loop filter. With insufficient feedback, the integrators saturate to their maximum or minimum values causing the modulator not to track the input anymore. In a single-bit modulator, instability occurs as long sequences of consecutive of ±FSR/2 [Bou03]. The first-order modulator is intrinsically stable for whatever input within the range [–FSR/2,FSR/2]. A second-order modulator, illustrated in Figure 4-5, is stable when the input is within the range 0.9×[–FSR/2,FSR/2] and $g_3/(g_1 \times g_2) > 1.25$ [Can85]. When $N>2$, it is not possible to determine a stability condition analytically.

One method to ensure stability in a modulator is to control the loop-gain by limiting the infinity norm of the NTF, $|\text{NTF}|_\infty$ [Lee87]. This method has been used to design numerous commercial modulators despite the lack of a rigorous theory for the stability of high-order modulators.

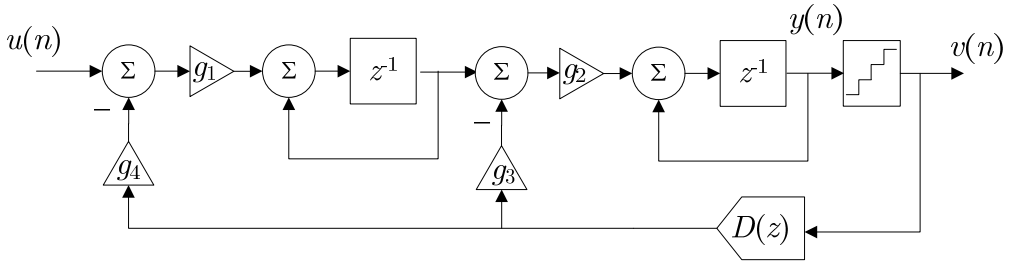


Figure 4-5 Second-order ΔΣ modulator in cascade of integrators distributed feedback topology

4.3 NTF Synthesis

NTF synthesis is the first step to design a modulator for a given set of specifications such as SNR, signal bandwidth, and dynamic range. NTF of the

modulator can be represented as the ratio of two rational polynomials in the z-domain as:

$$\mathrm{NTF}(z) = \frac{a_0 + a_1 z^{-1} + \ldots + a_n z^{-n}}{b_0 + b_1 z^{-1} + \ldots + b_n z^{-n}} \tag{4.13}$$

where $a_0, a_1, \ldots, a_n$ and $b_0, b_1, \ldots, b_n$ are coefficients of the numerator and denominator, respectively. When the quantizer is assumed to have unity gain, κ=1, the loop filter can be written as

$$H(z) = \frac{1 - \mathrm{NTF}(z)}{\mathrm{NTF}(z)} = \frac{(b_0 - a_0) z^n + (b_1 - a_1) z^{n-1} + \ldots + b_n - a_n}{a_0 z^n + a_1 z^{n-1} + \ldots + a_n} \tag{4.14}$$

According to the causality constraint of the modulator, there must be at least one unit of delay along the loop since otherwise the quantizer output in the current time step would form the current input [Nor97]. This constraint can be met by setting a_0=b_0, hence the order of the numerator is smaller than that of the denominator. This is equivalent to requiring the first sample of the impulse response of the NTF to be unity. Once the causality constraint is met, $|\mathrm{NTF}|_\infty$ must be adjusted to ensure the stability of the modulator. There have been several attempts to derive a rule-of-thumb to determine $|\mathrm{NTF}|_\infty$ through simulations. For a fourth-order modulator, Lee suggested that it should be less than or equal to 2 [Lee87]:

$$\max_{\nu} \left| \mathrm{NTF}(\nu) \right| \leq 2 \tag{4.15}$$

Schreier argued that Lee's criterion is too conservative for second-order modulators, is approximately correct for third-order modulators, but is too relaxed for higher order modulators [Sch93]. As can be observed from Figure 4-6, increasing the $|\mathrm{NTF}|_\infty$ gives better noise shaping; however, it also pushes the modulator to the edge of instability. Therefore, the $|\mathrm{NTF}|_\infty$ of the NTF in a modulator should be adjusted by trial-and-error through simulations for a specific design. An efficient NTF synthesis strategy is to determine NTF poles and zeros separately as shown in Figure 4-7 [Sch00]. The NTF of a modulator can be written in Zero, Pole, and Gain (ZPK) form as:

$$\mathrm{NTF}(z) = k\frac{\Pi_{i=1}^{N}(z - z_i)}{\Pi_{i=1}^{N}(z - p_i)} \tag{4.16}$$

where z_i are the zeros, p_i are the poles, and k is the gain of the NTF. In-band noise power can be minimized by tuning the NTF zeros while the $|\mathrm{NTF}|_\infty$ can be set to a specific level by tuning the NTF poles. For narrow-band applications, zeros can be put together at DC (Butterworth zeros) to form a deep notch, while for wide-band applications the minimum in-band noise power can be obtained by Chebyshev type-II or elliptic zeros. A detailed synthesis procedure for this method is given in [Sch04] and [Zhu07].

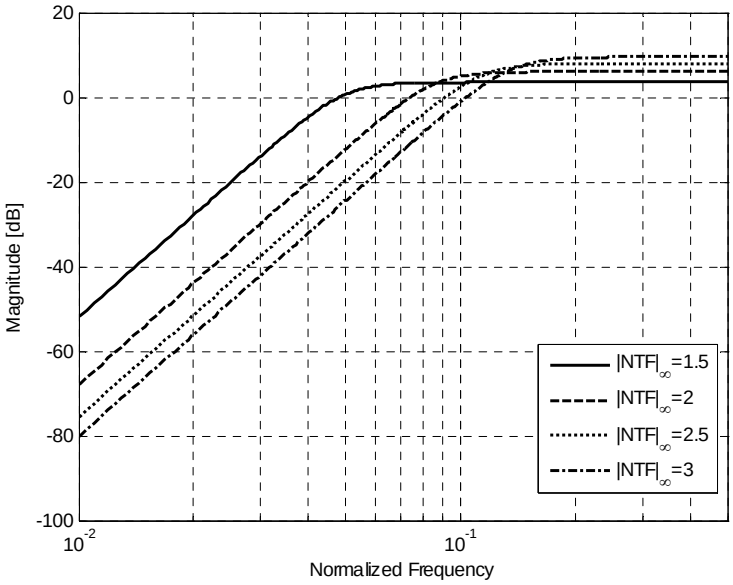


Figure 4-6 Fourth-order NTF for different values of $|\mathrm{NTF}|_\infty$

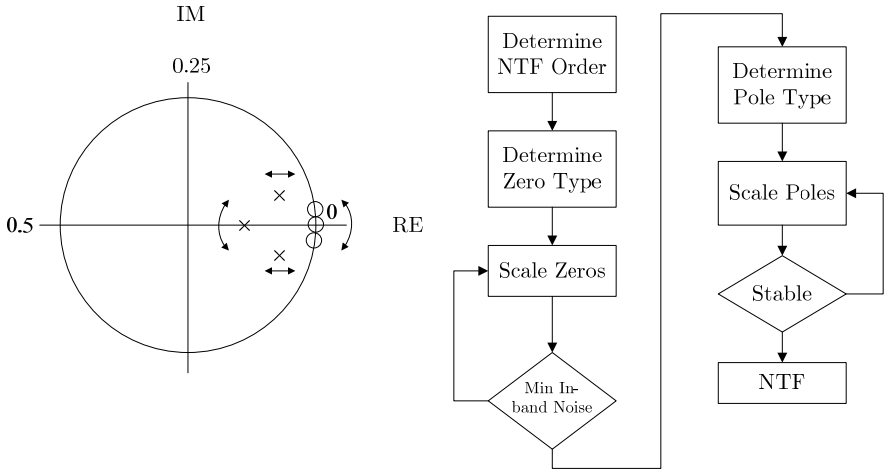


Figure 4-7 (a) NTF pole and zero tuning (b) NTF synthesis strategy [Zhu07]

4.4 Band-pass ΔΣ Modulators

Low-pass ΔΣ modulators are not suitable for RF/IF ADCs since the OSR has to be increased to an unreasonable level to obtain a suitable SNR for the band from DC to the signal bandwidth. The practical solution is to replace the low-pass loop filter with a band-pass one. Band-pass ΔΣ modulators are immune to flicker noise and are especially suitable for multi-band applications since A/D conversion can be done at RF without requiring any extra analog components to down-convert the input signal. The following transformation can be used to obtain a BPF from its prototype LPF [Opp98]:

$$z^{-1} \rightarrow z^{-1}\frac{z^{-1}-\alpha}{1-\alpha z^{-1}}, \quad -1<\alpha<1 \tag{4.17}$$

where α is a real number. The order of the resulting BPF is twice as high as that of the low-pass prototype. Placing the band centre at simple fractions of ν=0.5 reduces the complexity of the decimation filter [Sch90], [Kru03]. When α=0, $z^{-1}\rightarrow -z^{-2}$ transformation places the band to ν=0.25 or $f_S/4$. Applying this transformation to STF and NTF of a first-order ΔΣ modulator gives the second-order band-pass ΔΣ modulator with the STF and NTF given as:

$$\mathrm{STF}\left(z\right)=z^{-2}, \quad \mathrm{NTF}\left(z\right)=1+z^{-2} \tag{4.18}$$

As can be observed from Equation (4.18), the STF now delays the input signal by two clock cycles and the zeros of the NTF are moved from DC to ν=±0.25 as illustrated on the unit circle in Figure 4-8. Therefore, the quantization noise is shaped by a notch transfer function around $\pm f_S/4$. As can be observed from Figure 4-8, the $z^{-1} \rightarrow -z^{-2}$ transformation does not change the dynamics of the low-pass prototype; therefore, a stable low-pass modulator produces a stable band-pass one [Sho95a].

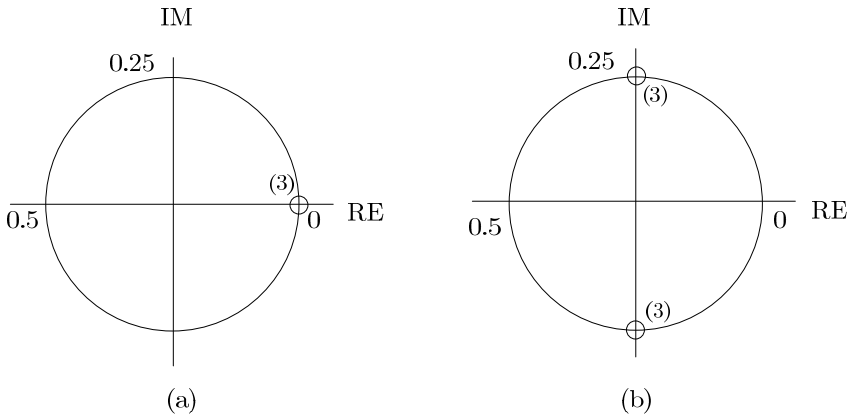
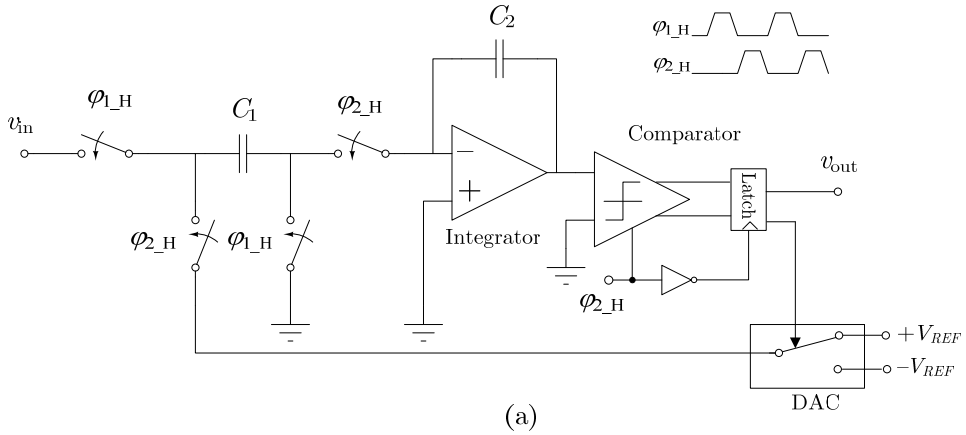


Figure 4-8 NTF zeros for a (a)Third-order low-pass modulator (b)Sixth-order $f_S/4$ band-pass modulator

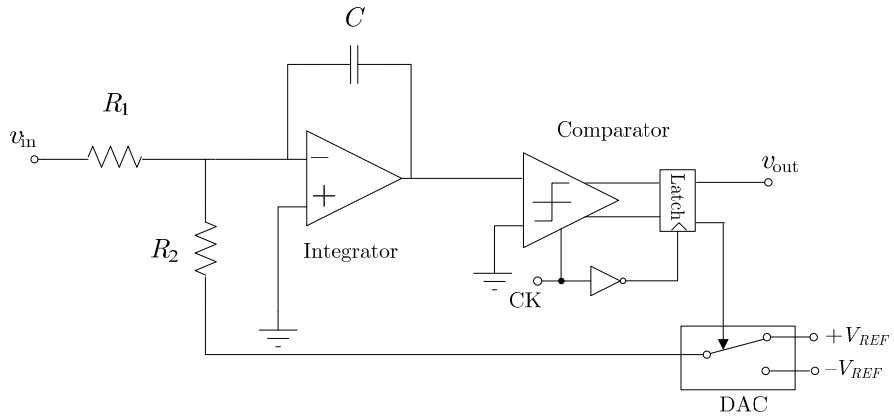
4.5 Continuous-Time ΔΣ Modulators

The majority of integrated ΔΣ modulators have been built with DT loop filters using the Switched-Capacitor (SC) circuit technique. A single-ended SC implementation of the first-order modulator with a two-phase non-overlapping clock is given in Figure 4-9(a) [Gre86]. SC-ΔΣ modulators are well suited to MOS integration, provide a good control of the loop filter's coefficients, and are relatively insensitive to clock jitter at the output of the feedback DAC [Won96]. For band-pass modulators, SC implementation has the advantage of not requiring any automatic tuning scheme since the centre frequency of a SC BPF is fixed by capacitor ratios [Tha06]. However, the maximum clock rate, and therefore, the conversion bandwidth are limited in SC implementations due to the capacitor settling time. When a two-phase non-overlapping clock is

utilized, the SC integrator has to settle to the final value within one-half of the clock period. This translates to very high slew rate demands for the integrator amplifiers; therefore, a SC-ΔΣ modulator built in a process with f_T[†] has the maximum clock rate on the order of $0.01 \times f_T$ [Che98], [Mur08]. On the other hand, a CT modulator could be clocked up to ten times faster in the same technology[‡] since waveforms vary continuously. Moreover, a CT modulator provides a certain amount of AA filter at no extra cost, suppresses the noise injected by sampling, and is better suited to lower supply voltages since CT filters do not require high voltages to properly switch on and off like their SC counterparts.



(a)



(b)

Figure 4-9 (a) Switched-capacitor (b) Active RC implementation of the first-order single-bit ΔΣ modulator

[†] f_T is frequency where the small-signal current gain of a transistor drops to unity

[‡] In [Che98], it was suggested that the sampling rate should not exceed $0.2 \times f_T$ in CT-ΔΣ modulators to keep the modulator stable

These advantages make CT modulators a suitable candidate for high speed, wide bandwidth, and low power applications [Bre04], [Dag04], [Mit06], [Cha07], [Zhi07]. The main drawback of the CT modulators is their vulnerability to clock jitter resulting from the feedback DAC. The active RC implementation of the first-order CT modulator is depicted in Figure 4-9(b) [Ban83]. When the feedback DAC waveform is rectangular in a CT modulator, charge is transferred at a constant rate over a clock period. Since the CT modulator integrates the feedback waveform over time, any timing error at the output of the DAC translates to amplitude errors increasing the overall noise floor. In contrast, most of the charge transfer occurs at the start of the clock period in a DT modulator; therefore, the amount of charge lost due to timing errors is relatively small [Che98].

4.5.1 Feedback DAC

The feedback DAC is a significant design parameter in CT-ΔΣ modulators since the overall transfer function of a CT modulator depends on the pulse shape of the DAC. Therefore, the feedback DAC affects key performance metrics of the modulator such as linearity, clock jitter, speed, and power consumption. The most commonly used pulse shapes for the DAC are rectangular ones since they can easily be implemented with the switched-current (SI) approach as illustrated in Figure 4-10 [Tou93]. The SI-DAC is very fast, occupies relatively small area for low resolutions, and power efficient since almost all power is directed to the output [Wik01]. The main disadvantage is its sensitivity to device mismatches.

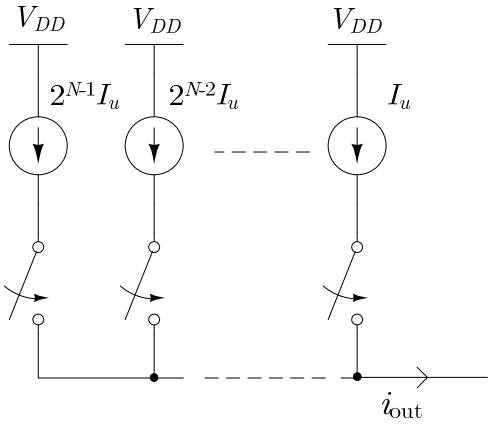
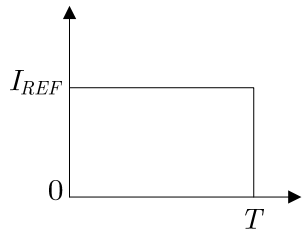


Figure 4-10 N-bit switched-current DAC

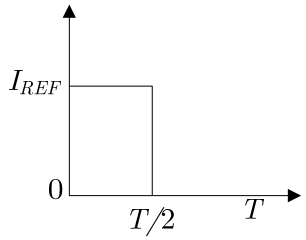
Rectangular pulse shapes, as illustrated in Figure 4-11, can be implemented with a single-bit SI-DAC. In a Non-Return-to-Zero (NRZ) DAC, the output is held during the entire cycle while in a Return-to-Zero (RZ) or a Half-Return-to-Zero (HRZ) DAC, the output needs to settle and recover in each cycle of the clock. The NRZ-DAC is less sensitive to clock jitter than the RZ and HRZ-DAC since pulse transition (from $+I_{\mathrm{REF}}$ to $-I_{\mathrm{REF}}$ or vice versa) only occurs when there is a change in the polarity of the comparator output. On the other hand, the RZ-DAC is preferred to the NRZ-DAC in multi-bit $\Delta\Sigma$ modulator since it is less sensitive to errors related with unequal rise/fall times [Zha02], [Zar08]. However, multi-bit DACs suffer from linearity problems and their relatively high power consumption. Other feedback DAC types include SC-DAC [You01], the sine-shaped DAC (SINDAC) [Esh02], and the jitter insensitive Switched Shaped-Current (SSI) DAC [Zar08]. A performance comparison of the various feedback DACs is given in Table 4-1 [Zar08].



$$d_{NRZ}(t) = \begin{cases} I_{REF}, & 0 \le t \le T \\ 0, & \text{otherwise} \end{cases}$$

$$D_{NRZ}(s) = \frac{1 - e^{-sT}}{s}$$

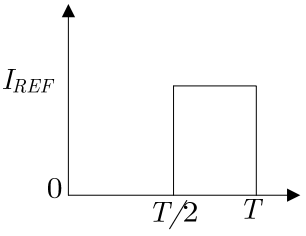
(a)



$$d_{RZ}(t) = \begin{cases} I_{REF}, & 0 \le t \le T/2 \\ 0, & \text{otherwise} \end{cases}$$

$$D_{RZ}(s) = \frac{1 - e^{-sT/2}}{s}$$

(b)



$$d_{HRZ}(t) = \begin{cases} I_{REF}, & T/2 \le t \le T \\ 0, & \text{otherwise} \end{cases}$$

$$D_{HRZ}(s) = \frac{e^{-sT/2} - e^{-sT/2}}{s}$$

(c)

Figure 4-11 Pulse shape and transfer function of (a) NRZ-DAC, (b) RZ-DAC, and (c) HRZ-DAC [Ort06]

Table 4-1 Performance comparison of the feedback DACs

	NRZ	Multi-bit NRZ	SC-DAC	SINDAC	SSI
Ease of Realization	+ +	+	+ +	– –	+
Jitter Cancellation	–	+	+ +	–	+ +
Linearity	+ +	– –	+	–	+
Speed	+	+	–	+	–
Power Consumption	+	–	– –	–	+

4.5.2 Semi-Digital FIR Filter

An important D/A conversion technique is the semi-digital Finite Impulse Response (FIR) filter (also known as the FIRDAC [Oli03]), which is illustrated in Figure 4-12 [Su93]. The semi-digital FIR filter cannot actually be classified as another type of DAC since any single-bit DAC can be utilized within the structure. The pulse shape of the single-bit DAC and the reference levels (tap-weights of the filter) define the transfer function of the semi-digital FIR filter, which can be written as:

$$F(s) = D(s)\left(a_0 e^{-s} + a_1 e^{-2s} + \ldots + a_{n-1} e^{-(n-1)s}\right) \tag{4.19}$$

where $a_0,\ldots,a_{n-1}$ are the coefficients of the filter. In a semi-digital FIR filter, the single-bit digital signal is shifted in time as it is weighed and converted to analog at each stage to give a piece-wise linear output, thus reducing the clock jitter sensitivity. The advantage of the semi-digital FIR filter over a multi-bit DAC is its inherent linearity since its output is a linear combination of the outputs of single-bit DACs and any single-bit DAC has linear DC transfer characteristics. The semi-digital FIR filter also acts as a reconstruction filter and helps to smooth the analog output. Matching errors in the weights of the DACs slightly affect the transfer function, as illustrated in Figure 4-13, but without introducing any distortion and affecting the linear DC transfer characteristics. In a practical implementation, distortion would be introduced as a result of other circuit non-idealities such as finite output impedance and non-linear switches. [Wik99a].

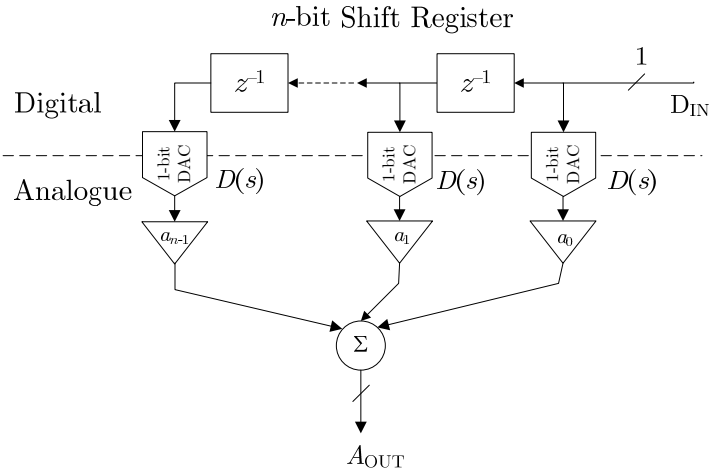


Figure 4-12 Block diagram of the semi-digital FIR filter

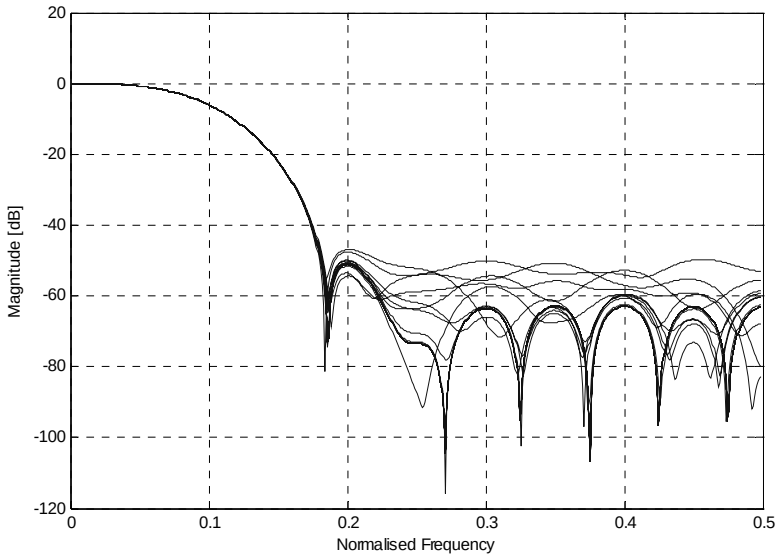


Figure 4-13 Monte Carlo simulation of a 20-tap low-pass semi-digital FIR filter assuming a random mismatch of 0.5% on every weight

4.5.3 Discretization of CT-ΔΣ Modulators

The block diagrams of single-loop DT and CT-ΔΣ modulators are given in Figure 4-14(a). Although it is a common practice to sample the CT signal within the quantizer rather than with a S/H or a T/H in CT modulators, the S/H block is shown in Figure 4-14 for convenience since this would not affect the mathematical analysis presented in this section. As sampling is performed inside the feedback loop, the overall loop transfer function of the CT

modulator is actually a DT transfer function [Sho95a]. Breaking the loop at the input of the feedback DAC and applying zero input enables to study the behaviour of the linear portion of the feedback loop [Che02]. This leads to the open loop diagram as depicted in Figure 4-14(b). The hat notation, ^, is used here is for distinguishing the CT variables from the DT ones.

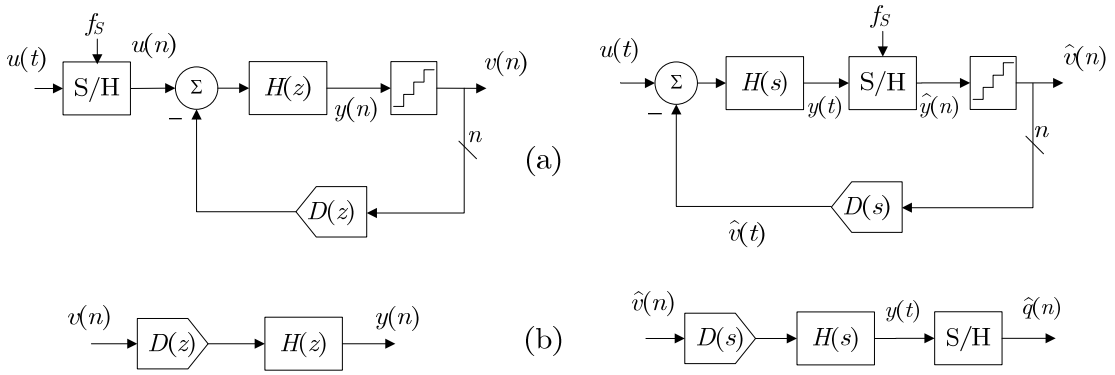


Figure 4-14 Block diagram of the (a) DT and CT-ΔΣ modulators (b) Their open-loop diagram

When input voltages to the quantizer are equal at sampling instants,

$$y(n) = y(t)_{t=kT},\ k = 0,1,2,\ldots \tag{4.20}$$

the output bit streams of the modulators would be equal. This condition directly translates into [Thu91]:

$$Z^{-1}\left\{H\left(z\right)\right\} \equiv L^{-1}\left\{D\left(s\right)H\left(s\right)\right\}_{t=kT},\ k = 0,1,2,\ldots \tag{4.21}$$

where $Z\{.\}$ and $L\{.\}$ denote the z- and Laplace transforms, respectively. This $s \leftrightarrow z$ mapping is called Impulse-Invariant Transformation (IIT) since the open-loop impulse responses are required to be equal at sampling instants [Gar86]. In IIT, one sample period delay in CT-domain corresponds to one sample delay in DT-domain.

$$\delta\left(t - T\right) \leftrightarrow e^{-sT} \leftrightarrow z^{-1} \tag{4.22}$$

The discretization of a CT modulator employing NRZ-DAC can be expressed as:

$$\hat{H}(z) \triangleq \mathrm{IIT}_{\mathrm{NRZ}}\left\{H(s)\right\} = Z\left\{L^{-1}\left\{H(s)\frac{1-e^{-sT}}{s}\right\}\right\} = \left(1-z^{-1}\right)Z\left\{L^{-1}\left\{\frac{H(s)}{s}\right\}\right\} \quad (4.23)$$

IIT enables the design of a CT loop filter with a specific DAC pulse shape that matches the exact noise-shaping behaviour of its DT counterpart by matching the discretizated open-loop CT transfer function $\hat{H}(z)$ to its DT prototype $H(z)$. Due to the causality property of convolution, the impulse response of a CT loop filter's first sample is zero. Therefore, in order to derive a CT loop filter from its DT equivalent, it is required to have at least one delay in the numerator [Sho95a]. The $s \leftrightarrow z$ mapping of the first-order integrator and the second-order resonator with RZ- and NRZ-DAC pulse shapes are given in Table 4-2. Higher order mappings can be calculated with the help of a symbolic mathematics software package, e.g., MATHEMATICA [Wol08].

Table 4-2 First-order LPF and second-order resonator $s \leftrightarrow z$ mappings for DT and CT modulators with RZ and NRZ DAC pulse shapes

DT Loop Filter $H(z)$	CT Loop Filter $H(s)$	
	RZ-DAC	NRZ-DAC
$\frac{z^{-1}}{1-z^{-1}}$	$\frac{2}{sT}$	$\frac{1}{sT}$
$\frac{-z^{-2}}{1+z^{-2}}$	$\frac{\frac{2.414\pi}{4T}s - \frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$	$\frac{\frac{\pi}{4T}s - \frac{1}{2}\left(\frac{\pi}{2T}\right)^2}{s^2+\left(\frac{\pi}{2T}\right)^2}$

4.5.4 STF and NTF in CT-ΔΣ Modulators

The two-input linearized model of the DT-ΔΣ modulator [Jan93], as depicted in Figure 4-15(a), can be utilized to investigate the STF and NTF of the CT modulator. When $D(z)$=1, the STF and NTF of the DT-ΔΣ modulator can be written as:

$$\mathrm{STF}\left(z\right)=\frac{\kappa H_0\left(z\right)}{1-\kappa H_1\left(z\right)},\ \ \mathrm{NTF}\left(z\right)=\frac{1}{1-\kappa H_1\left(z\right)} \tag{4.24}$$

This representation, in fact, is the generalized form of the single-input linearized model described in Section 4.1 in which the difference $u(n)$–$v(n)$ enters the loop filter $H(z)=H_0(z)=-H_1(z)$. The equivalent representation of this for the CT modulator, depicted in Figure 4-15(b), reveals that the NTF matches the noise-shaping behaviour of its DT counterpart [Sho95a]. Indeed, the NTF of the modulators are made equivalent by the $s \leftrightarrow z$ mapping as described in Section 4.5.3. For the single-input linearized model of the CT modulator with a NRZ-DAC, the NTF can be written as in the z-domain as:

$$\mathrm{NTF}\left(z\right)=\frac{1}{1+\kappa\,\mathrm{IIT}_{\mathrm{NRZ}}\left\{H\left(s\right)\right\}}=\frac{1}{1+\kappa\hat{H}\left(z\right)} \tag{4.25}$$

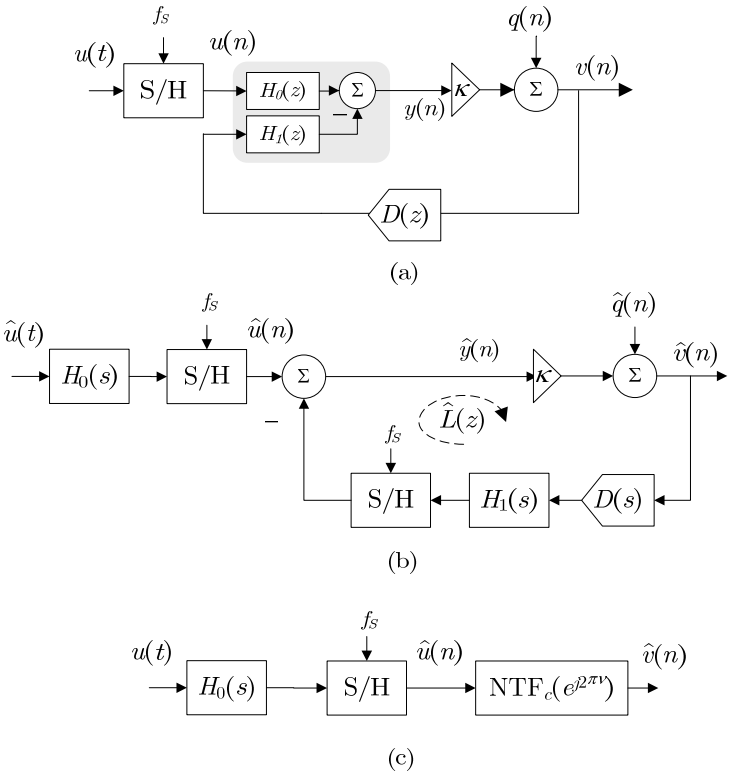


Figure 4-15 (a) Two-input linearized model of the DT-ΔΣ modulator, (b) An equivalent representation of the two-input model for the CT-ΔΣ modulator (c) Another equivalent representation with an emphasis on implicit AA filter

where $\hat{H}(z)$ is the IIT of $H(s)$. The describing equation of the linearized model of the DT modulator, given in Equation (4.6), can be redefined for CT modulator depicted in Figure 4-15(b) as:

$$\hat{V}\left(z\right)=\frac{\kappa Z\left\{L^{-1}\left\{U\left(s\right)H_0\left(s\right)\right\}\right\}}{1-\kappa Z\left\{L^{-1}\left\{D\left(s\right)H_1\left(s\right)\right\}\right\}}+\frac{Q\left(z\right)}{1-\kappa Z\left\{L^{-1}\left\{D\left(s\right)H_1\left(s\right)\right\}\right\}} \tag{4.26}$$

For the single-input case with a NRZ-DAC, the STF can be expressed as:

$$\hat{V}\left(z\right)=\frac{\kappa Z\left\{L^{-1}\left\{U\left(s\right)H_0\left(s\right)\right\}\right\}}{1+\kappa\hat{H}\left(z\right)}+\frac{Q\left(z\right)}{1+\kappa\hat{H}\left(z\right)} \tag{4.27}$$

Since

$$Z\left\{L^{-1}\left\{U\left(s\right)H_0\left(s\right)\right\}\right\}\neq Z\left\{L^{-1}\left\{U\left(s\right)\right\}\right\}\times Z\left\{L^{-1}\left\{H_0\left(s\right)\right\}\right\} \tag{4.28}$$

the STF of a CT modulator cannot be represented in the z-domain. If forward filter $H_0(s)$ is assumed to be attenuating the high frequency components adequately, the STF can be approximated by Equation (4.29) as illustrated in Figure 4-15(c) [Sho95a]:

$$\mathrm{STF}\left(\nu\right)=\frac{V\left(\nu\right)}{U\left(\nu\right)}\approx H_0\left(\nu\right)\times\underbrace{\frac{e^{-j\pi\nu}\times\sin\left(\pi\nu\right)}{\pi\nu}}_{\text{S/H}}\times\underbrace{\frac{1}{1+\kappa H\left(z\rightarrow e^{j2\pi\nu}\right)}}_{\text{NTF}} \tag{4.29}$$

For the sake of comparison between the STFs of DT and CT modulators, the sinc term associated with S/H term can be removed from Equation (4.29) as sampling is present in both modulators. The approximated STF is written as:

$$\mathrm{STF}\left(\nu\right)\approx\hat{H}_0\left(\nu\right)\mathrm{NTF}\left(z\rightarrow e^{j2\pi\nu}\right) \tag{4.30}$$

Equation (4.3) also shows that the CT-ΔΣ modulator provides inherent AA filtering on the input signal since the sinc function attenuates the input spectrum at multiples of the sampling frequency as shown in Figure 4-16. The STF does not provide any AA filtering in DT modulators since the input shaped by the sinc function after sampling.

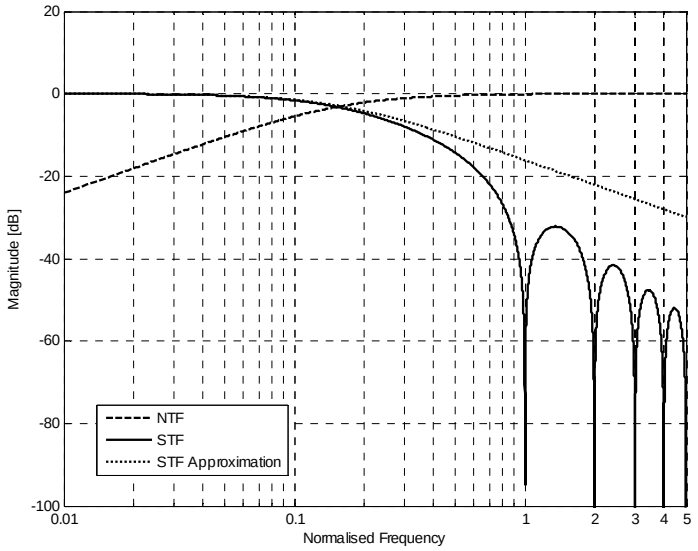


Figure 4-16 STF and NTF of the first-order CT-ΔΣ modulator

4.5.5 Excess Loop Delay

The delay between the quantizer clock and the output pulse of the DAC due to the asynchronous transistor switching time is called Excess Loop Delay (ELD) [Che99]. ELD is a severe problem in high-speed CT modulators employing NRZ-DAC as it may shift the DAC pulse into the next clock cycle, as illustrated in Figure 4-17. CT modulators with RZ feedback pulse are much less susceptible to ELD since RZ pulse has a safety margin before it shifts to the next clock cycle. The effects of ELD on the modulator's performance are analyzed in detail in [Che98] and it was concluded that ELD moves the NTF poles towards the unit circle, which increases the in-band quantization noise and lowers the maximum stable input amplitude. Additionally, the order of the modulator increases by one when the DAC pulse is shifted to the next clock cycle.

In high-speed CT-ΔΣ modulators, sampling and quantization is usually performed within the quantizer by latched comparators. A single-bit quantizer, in that case, consists of a pre-amplifier followed by a regeneration (or latching) stage [Yuk85], as illustrated in Figure 4-18.

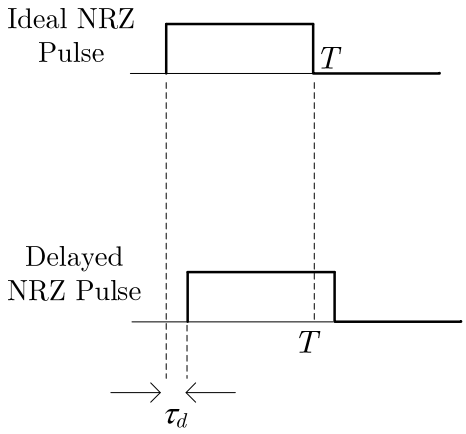


Figure 4-17 The effect of ELD on the NRZ-DAC pulse

When the switch is closed, the pre-amplifier amplifies the differential input voltage. This stage is called the tracking phase since the output "tracks" the input. When the switch is open, the positive feedback formed by the back-to-back inverting amplifiers pushes the output voltage to $\pm V_{\mathrm{REF}}$. Pre-amplification is necessary here for minimizing the kickback noise, which is due to the coupling of the large voltage variations on the regeneration nodes to the input of the comparator through the parasitic capacitances of the transistors in the amplifier [Fig06].

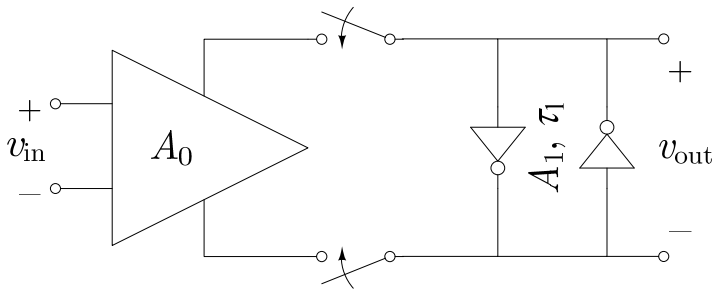


Figure 4-18 Latched comparator

The back-to-back inverting amplifiers represent a memory unit (i.e. a latch) which might entail to metastability when small voltages appear at the input of the comparator. It can be shown that the voltage difference between the output nodes of the regenerative circuit can be modelled as [Raz95], [Jon97]:

$$\Delta v = \Delta v_0 \, \mathrm{e}^{\left(A_1 - 1\right) t / \tau_1} \tag{4.31}$$

where Δv_0 is the initial voltage difference between the output nodes, A_1 is the voltage gain, and τ_1 is the characteristic time constant of the inverting amplifiers. Therefore, the voltage difference increases exponentially in time with the regeneration time constant:

$$\tau_R = \frac{\tau_1}{A_1 - 1} \tag{4.32}$$

The regeneration time necessary to push the input voltage to $\pm V_{\mathrm{REF}}$ can be written as:

$$t_R = \tau_R \ln\left(\frac{\Delta v}{\Delta v_0}\right) \tag{4.33}$$

As Δv_0 gets smaller, the regeneration time may become larger than the time allowed for the regeneration phase; and therefore, Δv might fail to be increased enough to reach one of the stable states ($\pm V_{\mathrm{REF}}$). This causes a random delay at the output of the quantizer along with quantizer's inherent latency. A common approach to minimize the occurrence of metastable states at the output of the quantizer is to utilize a cascade of latches to provide a more positive feedback gain for regeneration [Tha06]. Since each additional latch introduces $z^{-1/2}$ delay, the total delay in the feedback path due to inherent latency of quantizer and the DAC, as well as the random delay due to metastability should be accommodated in the DT-CT equivalence when finding the open loop transfer function of the CT modulator.

4.5.6 Loop-Filter Implementation

Loop filter of a CT modulator can be implemented with several structures including active-RC, transconductance-C, MOSFET-C, and LC filters [Ban83], [Tsi86], [Nau92], [Kuh95], [Pip96], [Hua97], [Pav02].

The Active-RC integrator, previously depicted in Figure 4-9(b), provides a good linearity but is not suitable for high-speed applications because of the closed-loop feedback and the limited bandwidth of the Op-Amp. Additionally, the relatively low accuracy of capacitors and resistors in standard CMOS processes create a necessity to tune of the filter structure [Gee05]. Active-RC

integrators are usually employed to implement the first stage of sub-megahertz low-pass modulators when a good linearity is required. The MOSFET-C structure replaces the resistor with a MOS transistor, which is biased in the linear region to create the necessary resistance value. The transfer function of the integrator can be written as:

$$H_{\text{MOS-C}}\left(s\right) = -\frac{g_m}{sC} = -\frac{\omega_0}{s} \tag{4.34}$$

where ω_0 is the angular centre frequency of the filter. The gate voltage of the transistor can be varied to change the transconductance value hence the structure is electrically tunable; however, the frequency range of filter is still limited by the bandwidth of the Op-Amp.

A transconductance-C filter consists of transconductance amplifier(s) with a capacitive load. A second-order band-pass transconductance-C filter is depicted in Figure 4-19(a) [Tha06]. The open loop, wide-band transconductance amplifier enables the structure to be utilized for high-speed applications up to frequencies in the hundreds of megahertz [Voo00]. The transfer function of the transconductance-C integrator is the same as that of the MOSFET-C integrator and, thus, it is electrically tunable. However, the lack of feedback translates into linearity problems; and therefore, transconductance-C integrators are preferred in the second and higher stages of the modulators [Zar08]. Another drawback of the structure is its sensitivity to parasitic capacitances, which alters the time constant of the integrator. Equation (4.35) suggests that in order to increase the cut-off frequency of the integrator, g_m must be increased or the capacitance must be decreased. Larger values of g_m increases power consumption and the minimum capacitance value is fundamentally limited by the intrinsic parasitic capacitances; therefore, transconductance-C structures are not suitable for RF applications in the gigahertz range.

The LC tank structure, depicted in Figure 4-19(b), has the advantage of being less sensitive to parasitic capacitances as they can actually be absorbed into the total reactance required for the design frequency [Gee05].

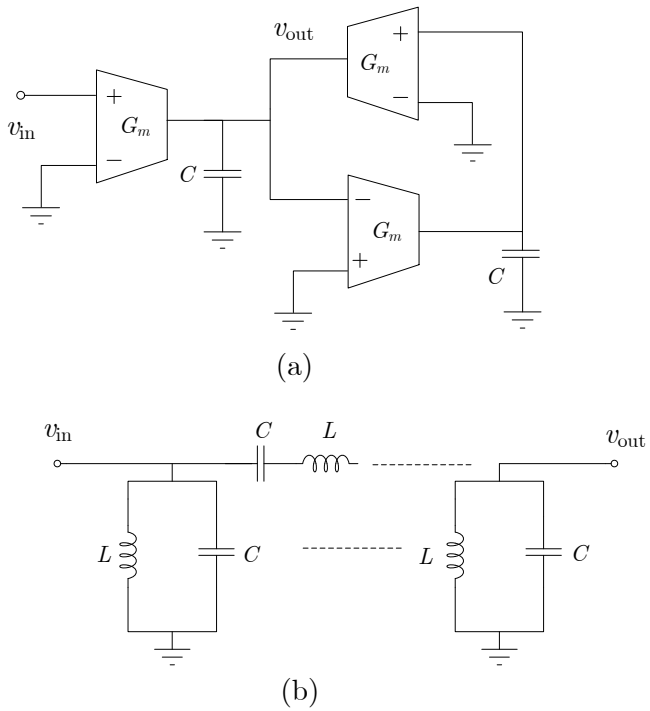


Figure 4-19 (a) Transconductance-C band-pass filter (b) Band-pass filter with LC tanks

This enables the structure to be utilized in gigahertz range applications. The transfer function of the ideal LC resonator,

$$R(s) = \frac{As}{s^2 + \omega_0^2} \tag{4.35}$$

has poles on $j\omega$-axis; and therefore, has an infinite Q-factor, as depicted in Figure 4-20.

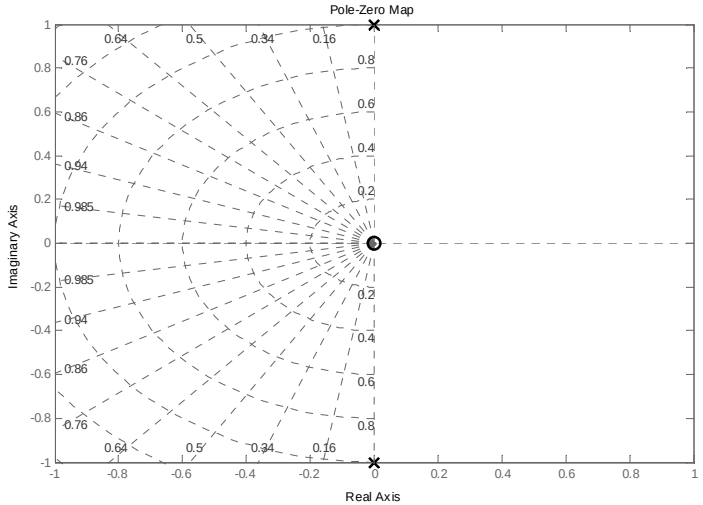


Figure 4-20 Pole-zero map of an infinite Q-factor resonator

In reality, parasitic resistances of the inductor and the capacitor limit Q-factor of the resonator. The base Q-factor of an LC tank can be written as:

$$\frac{1}{Q_0} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4.36}$$

where Q_L is the Q-factor of the inductor and Q_C is the Q-factor of the capacitor. The Q-factor of an on-chip LC tank is typically limited by the spiral inductor. On-chip spiral inductors, as illustrated in Figure 4-21, have Q-factors around 10 to 20 because of the ohmic losses in the metal contacts, the lossy substrate due to the bulk resistance, and the limited number of feasible turns [Dan05]. Increasing the number of turns beyond a certain value in an effort to increase the Q-factor does not help since the increased capacitance between the metal structures would self-resonate with the inductor [Pip96]. A Q-factor of 10 translates into 157.54MHz –3dB bandwidth when the centre frequency of the filter is set to GPS L1 band centre. Higher Q-factors are achievable in Silicon-Germanium (SiGe) BiCMOS and Silicon-On-Insulator (SOI) RF CMOS processes. Patterned ground shields have also been proposed to double the Q-factor of on-chip inductors in CMOS and BiCMOS processes [Yue98] [Che06].

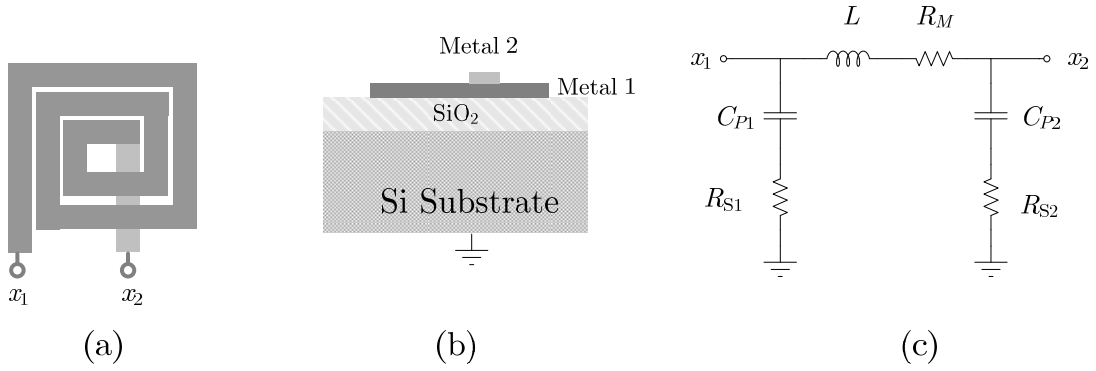


Figure 4-21 Spiral integrated inductor (a) Top view layout (b) Side view layout for a two-metal Si process (c) π-model equivalent circuit incorporating metal-to-substrate parasitic capacitance, substrate resistance, and ohmic loss in the metal contacts

The base Q-factor of an LC resonator can also be enhanced by utilizing an active device to generate a negative resistance that compensates for the resistive losses. Negative resistors can be implemented with single-ended or

differential schemes; however, negative resistance is inversely proportional with frequency-squared in single-ended schemes which poses problems for gigahertz range applications [Kar95]. Differential schemes are preferred since they are usually weakly dependent on frequency and less sensitive to noise and interference coupled through supply lines and the substrate [Dan05]. A simple way to generate negative resistance with a differential scheme is to cross-couple a matched transistor pair, as illustrated in Figure 4-22, where the positive feedback loop formed by the transistors results in a negative resistance of [Dun93]:

$$R_{\text{NEG}} = -\frac{2}{g_{m,\text{M1,2}}} \tag{4.37}$$

The negative resistance can be placed in series or parallel with the inductor. The simple lossy inductor model where the inductance is in series with a parasitic resistance, can be transformed into parallel mode, as illustrated in Figure 4-23, to simplify the analysis.

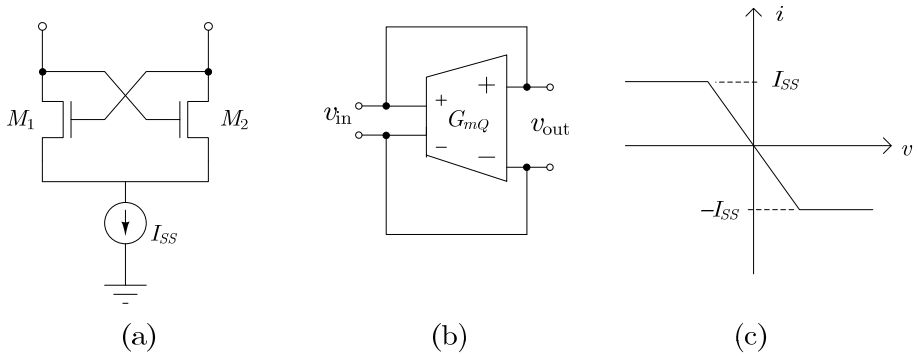


Figure 4-22 Cross-coupled MOSFET pair implementing negative resistance (a) Circuit schematic (b) Block diagram (c) I-V curve

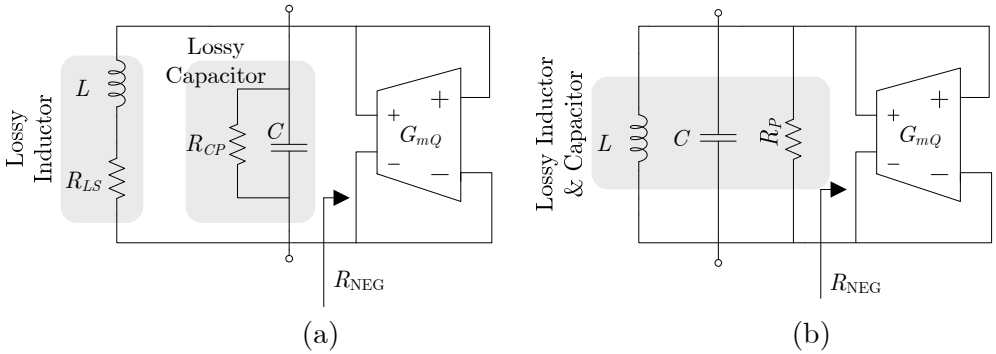


Figure 4-23 Series-to-parallel transformation for the Q-enhanced LC resonator

The transfer function of the Q-enhanced LC resonator can be written in the s-domain as [Nik07]:

$$R(s) = \frac{As}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} = \frac{As}{s^2 + \frac{s}{R_{EQ}C} + \frac{1}{LC}} \tag{4.38}$$

where

$$R_{EQ} = R_{NEG} \,||\, R_P \tag{4.39}$$

is the parallel equivalent resistance. At resonance, inductive and capacitive reactances are equal and the tank impedance is simply R_{EQ}:

$$Z(\omega_0) = \frac{1}{\underbrace{j\omega_0 C + \frac{1}{j\omega_0 L}}_{=0} + \frac{1}{R_{EQ}}} = R_{EQ} \tag{4.40}$$

Since the base Q-factor of a parallel RLC circuit is:

$$Q_0 = R\sqrt{\frac{C}{L}} \tag{4.41}$$

the enhanced Q-factor can be expressed as:

$$Q_E = \frac{Q_0}{1 + \frac{R_P}{R_{NEG}}} \tag{4.42}$$

Equation (4.42) shows that the Q-factor can be adjusted by the transconductance of the active device; hence, Q is electrically tunable. On the other hand, centre frequency tuning can be achieved with a variable capacitance since the angular centre frequency of the RLC circuit is

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{4.43}$$

PN-junction varactors [Bur96] or MOS varactors [Soo98] are preferred for realizing variable capacitances on-chip since they are relatively less noisy than other alternatives [Dan00]. MOS varactors generally have higher Q-factors and wider tuning range compared to PN-junction varactors. An NMOS varactor can be constructed by shorting the source and drain to apply a tuning voltage whilst the bulk is connected to ground. Voltage applied to gate determines the region of operation, as illustrated in Figure 4-24. It is desirable for the capacitance to be a monotonic function of gate voltage; therefore, the varactor to operate in the accumulation region. However, this cannot be guaranteed with an ordinary MOS varactor. Replacing the p+ source and drain diffusions of a PMOS varactor by n+ prevents the device to enter the inversion region regardless of the gate voltage. Such a device is called accumulation-mode (AMOS) varactor, which exhibits a lower series resistance as electrons have higher mobility than holes and typically have higher Q-factor than inversion-mode varactors [Soo02]. AMOS devices may not be available as standard cells for a given PDK.

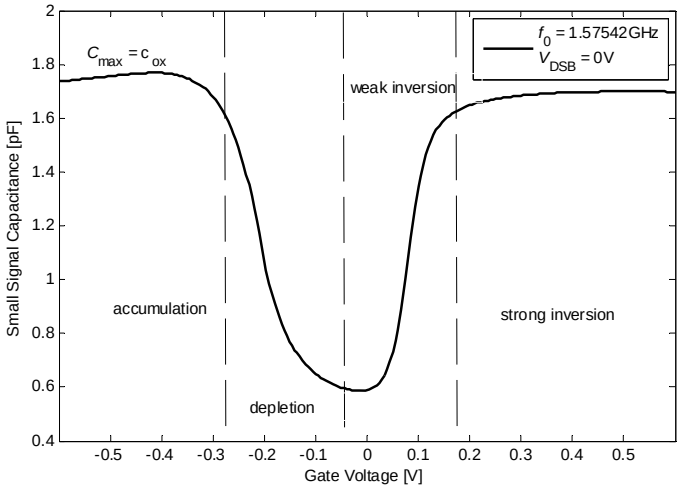


Figure 4-24 The variation of the small signal capacitance with gate voltage at 1.57542GHz for a 90nm NMOS varactor when tuning voltage (V_{DSB}) is set to 0V

Real-time automatic tuning of centre frequency and Q-factor is not only required for multi-band operation, but also for the deviation in the active and passive element values due to Process, Voltage, and Temperature (PVT) variations. Two common methods available for automatic tuning are master/slave tuning [Kho84], and self-tuning [Tsi81]. M/S tuning scheme

consumes more power, occupies larger chip area, and suffers from matching problems between the master and the slave filter. In self-tuning schemes, as illustrated in Figure 4-25, the filter is periodically removed from the circuit and tuned with the help of a tuning control circuitry that requires a frequency reference [Kuh95], [Gee05]. Therefore, it is more accurate as matching is not required. The disadvantages are the interruption of processing whilst the filter is being tuned and the need for a frequency reference. The self-tuning algorithm, proposed by Xin He and Kuhn eliminates the frequency reference requirement as the filter itself is used as a reference by turning it to an oscillator [Xin05]. A tuning circuit based on a modified version of this tuning method is proposed in Section 5.5.3.

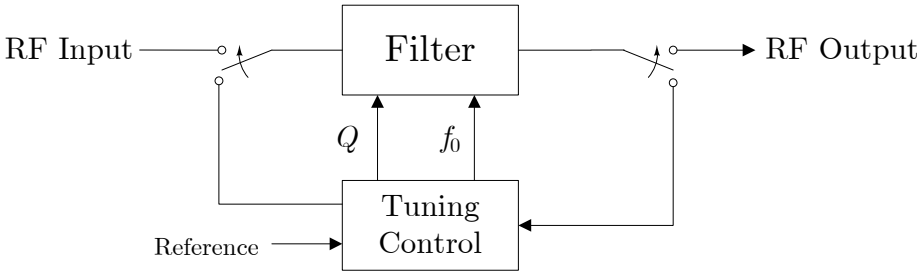


Figure 4-25 Block diagram of self-tuning scheme

Chapter 5

A Novel Subsampling Continuous-Time Delta-Sigma Modulator

As outlined in Chapter 1, conventional ΔΣ modulators are not suitable for subsampling A/D conversion due to two undesirable phenomena: Subsampling results in the attenuation of the RF alias in the sampled spectrum [Gou94] and in the reduction of the effective Q-factor of the loop filter [Yua05]. This chapter introduces a novel subsampling CT-ΔΣ architecture to mitigate the effects of subsampling. The proposed CT-ΔΣ modulator has significant improvements over previously published subsampling modulators [Gou94], [Hus00], [Kam06], [Bei07], [Her08], [Nad08] as it provides jitter and alias suppression and ELD compensation to improve the dynamic range, thus enabling the modulator to be utilized in subsampling receivers when a relatively low sampling rate is desired.

5.1 The Effects of Subsampling on ΔΣ Modulators

It is often a good practice to place the IF at the centre of the first Nyquist zone, as explained in Section 4.4. This can be achieved when the sampling rate is chosen as [Yuc04]:

$$f_S = \frac{4f_0}{2n+1},\ n = 0,1,2\ldots\ f_S = \frac{4f_0}{2n+1},\ n = 0,1,2\ldots \tag{5.1}$$

Defining the subsampling ratio as

$$M \triangleq \frac{4f_0}{f_S} = 2n+1 \tag{5.2}$$

is a convenient measure to characterize the effects of subsampling in so-called "$f_S/4$ modulators". When a conventional CT-ΔΣ modulator, as depicted in Figure 4-14(b), is utilized for subsampling A/D conversion, the RF alias of the feedback signal is severely attenuated since the S/H as well as any DAC with a rectangular pulse has sinc-shaped, low-pass frequency response, as illustrated in Figure 5-1. Larger values of the subsampling ratio, M, ensures lower sampling rates but at the expense of further attenuation of the feedback signal.

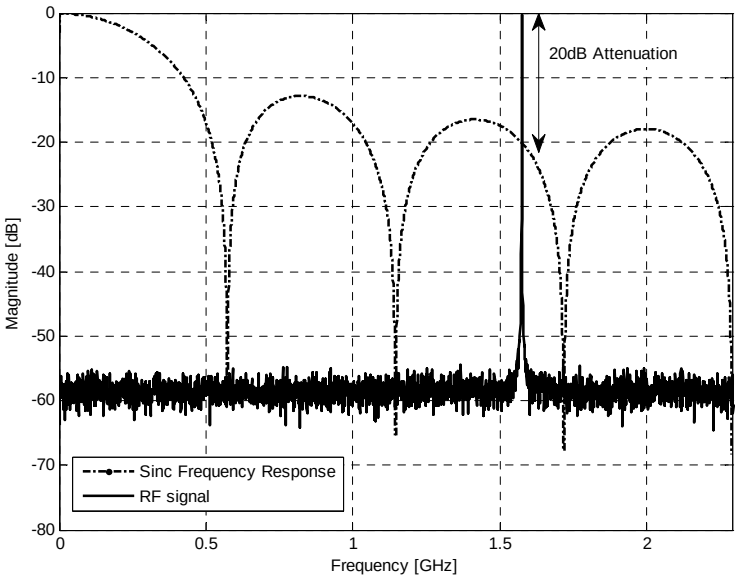


Figure 5-1 Attenuation of the GPS L1 signal by the sinc response for M=11

In addition to this, subsampling reduces the effective Q-factor of the loop filter; thereby, degrades the performance of the modulator. The IIT of the second-order resonator with a NRZ DAC is:

$$\hat{R}(z) = \mathrm{IIT}_{\mathrm{NRZ}}\left\{\frac{As}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}\right\} = Z\left\{L^{-1}\left\{\frac{As}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}\cdot\frac{1-e^{-sT}}{s}\right\}\right\}$$

$$= \frac{-AQ\left(e^{xT/Q}-1\right)(z-1)}{x\left(e^{T(x-\omega_0)/2Q}-z\right)\left(ze^{T(x+\omega_0)/2Q}-1\right)} \tag{5.3}$$

$$= \frac{AQ}{x}\cdot\frac{z\left(e^{xT/Q}-1\right)-e^{xT/Q}+1}{z^2e^{T(x+\omega_0)/2Q}+z\left(e^{xT/Q}+1\right)-e^{T(x-\omega_0)/2Q}}$$

where

$$x \triangleq \omega_0\sqrt{\left(4Q^2-1\right)} \tag{5.4}$$

Since $Q \gg 1$ and M is an odd number, the poles of $\hat{R}(z)$ can be approximated as:

$$p_{1,2} \approx \exp\left\{\pm jT\omega_0 - \frac{T\omega_0}{2Q}\right\} = \exp\left\{\pm\frac{1}{2}j\pi M - \frac{\pi M}{4Q}\right\} = \pm j\exp\left\{-\frac{\pi M}{4Q}\right\} \tag{5.5}$$

When the Q-factor is infinite, a DT resonator has its poles on the unit circle. For a conventional CT modulator employing sampling at a rate of f_S=$4f_0$, M equals to unity. As M increases, the pole radii get shorter resulting in lower effective Q-values, as illustrated in Figure 5-2. The poles of the loop filter correspond to the zeros of the NTF; therefore, larger values of M move the zeros of the NTF away from the unit circle. This will reduce the sharpness of the notch at the centre frequency of the filter leading to degraded noise shaping. To compensate for this effect, the Q-factor of the resonator must be enhanced at least by a factor of M.

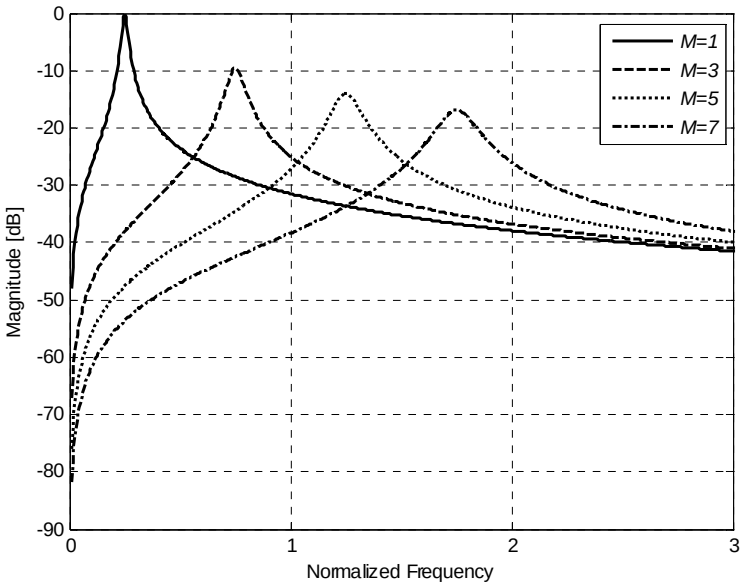


Figure 5-2 The effect of subsampling on the effective Q-factor of the loop filter

In order to compensate for the attenuation of the RF alias, Gourgue et al. [Gou94] proposed to utilize an analog mixer at the output of the feedback DAC to frequency translate the alias that falls in the first Nyquist region up to the frequency of the input signal, as illustrated Figure 5-3. An SNR analysis for the subsampling modulator with post-DAC mixing was later presented in [Hus00]. It was concluded that when the Q-factor of the loop filter is infinite, a phase difference of $\pi/4$ between the IF and Local Oscillator (LO) frequency provides the highest SNR. There are certain issues associated with the post-DAC mixing modulator:

- The $\pi/4$ phase difference is difficult to maintain due to the phase error caused by the analog mixer [Nad08]
- Since the phase noise of the LO is mixed with the IF signal, it is shaped by the STF of the modulator, which is flat in the band-of-interest
- The intermodulation of IF and LO signals may corrupt the feedback signal
- A finite Q-factor loop filter would amplify the effects of imperfections outlined above

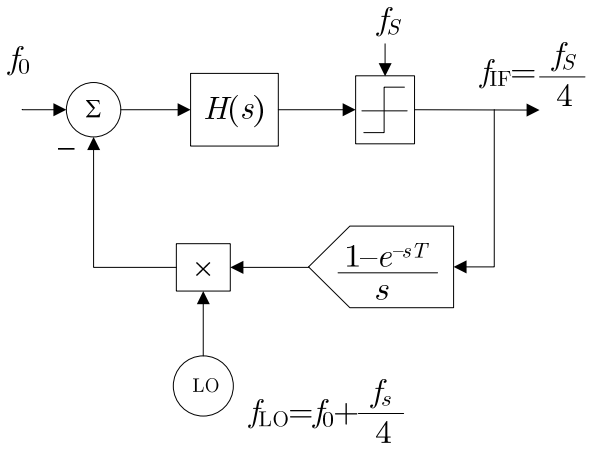


Figure 5-3 Subsampling modulator with post-DAC mixing

Kammoun et al. [Kam06] proposed to utilize FIR filters in the feedback path along with post-DAC mixing to compensate for the attenuation of the RF alias. While the FIR filters reduce the jitter sensitivity, this design still suffers from the same issues associated with [Gou94] and [Hus00].

Beilleau et al. [Bei07] proposed to utilize the raised-cosine DAC in the feedback since any SINDAC provides a band-pass frequency response. The RF alias of the signal is attenuated by the sinc response during both subsampling and D/A conversion; hence, a SINDAC with a unity gain at the desired frequency band would not provide any compensation. Therefore, M was chosen as low as 3 to keep the power consumption low; however, this led to a high sampling rate of 3.2 Gsps. SINDACs are generally less susceptible to clock jitter compared to the NRZ-DAC; however, they are difficult to realize and suffer from linearity problems, high power consumption and noise [Zar08].

Hernandez and Prefasi proposed to utilize two resonators with different technologies, as depicted in Figure 5-4, to enhance the modulator performance against both issues associated with subsampling modulators [Her08]. Since a typical low-loss transmission line has a Q-factor of 500 [Pre08], a transmission line filter is utilized in the feed-forward path to minimize the effective Q-factor reduction. A passive LC filter tuned to centre frequency of the input signal is utilized in the feedback to attenuate the aliases other than the RF alias. Some of the issues associated with this modulator are:

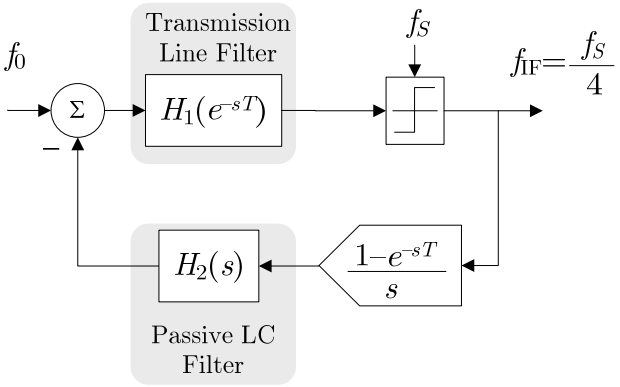


Figure 5-4 Subsampling modulator with two resonators

- Passive LC resonator in the feedback path cannot boost the attenuated RF alias; therefore, the modulator has a poor dynamic range
- An additional resonator as well as Q and frequency tuning of the additional resonator increases hardware complexity
- Silicon integrated transmission lines are constrained to values above tens of gigahertz, which makes them incompatible with GNSS frequencies, due to the chip dimensions and the dielectric constant of silicon [Pre08]

Naderi et al. [Nad08] proposed an all-digital solution to compensate for the signal attenuation by upsampling the digital signal at the output of the quantizer, as illustrated in Figure 5-5.

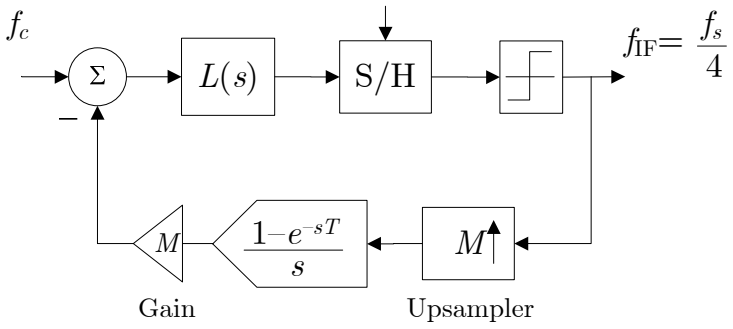


Figure 5-5 Subsampling modulator with zero-insertion upsampler

Upsampling by a factor of M is performed by inserting M–1 zeros between consecutive samples (i.e. zero-insertion method) rather than creating new samples from the original ones (i.e. zero-order hold method). The difference between the two methods is illustrated in Figure 5-6 and Figure 5-7.

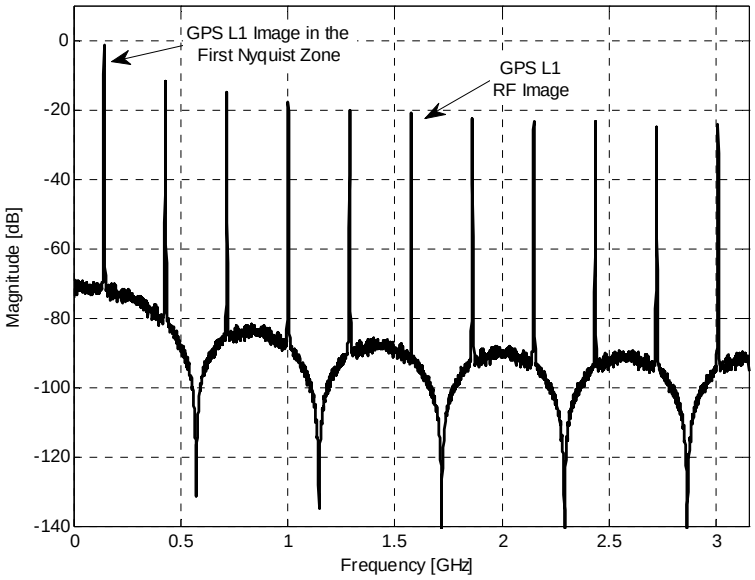


Figure 5-6 Upsampling by K=11 with a zero-order hold

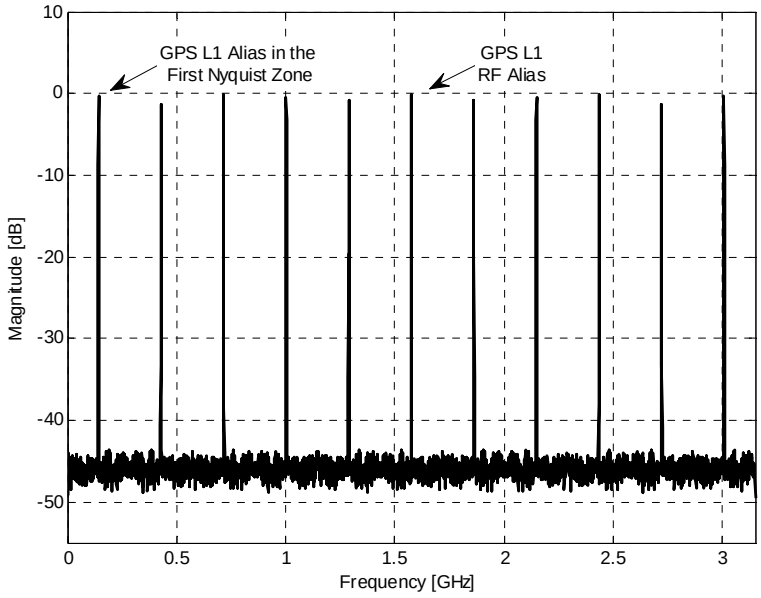


Figure 5-7 Upsampling by K=11 with zero-insertion

As can be observed from the figures, upsampling with a zero-order hold attenuates the RF alias whilst upsampling with zero-insertion replicates the signal in the first Nyquist zone, which is attenuated only by a few dBs. Nevertheless, increasing the bandwidth of the NRZ-DAC without attenuating the harmonics would increase the Total Harmonic Distortion (THD). Furthermore, the clock jitter at the output of the DAC would be a significant problem especially for higher values of the subsampling ratio. This design also

suffers from contrability issues, as will be explained in Section 5.2. These drawbacks hinder the approach to be utilized efficiently when a relatively low sampling rate is required.

5.2 Proposed Subsampling CT-ΔΣ Modulator

The topology and the circuit architecture of the generalised $(k–1)^{th}$ order configuration for the proposed modulator are illustrated in Figure 5-8 and Figure 5-9, respectively. Differential circuit architecture is preferred to reduce the input noise level caused by power supply fluctuations and substrate noise coupled from digital circuits; thereby, to improve the sensitivity of the loop filter [Gee05]. The distortion caused by the even-order harmonics in MOSFET circuits is reduced in balanced differential inputs and outputs [Rof96]. In addition, differential switches reduce the effects of clock feedthrough[†]. Current-steering DACs are opted to obtain high-speed operation and to reduce the complexity since it is easy to sum, weight, and switch currents [Wik99b].

A cascade of second-order Q-enhanced LC filters is opted for the loop filter realization in order to compensate for the reduction in the effective Q-factor. The feedback loop of the proposed modulator is optimized to minimize the effects of subsampling and to enhance the dynamic range. The analog RF signal at the output of the last LC filter is sampled with a subsampling rate chosen according to Equation (5.1). The sampled spectrum contains aliases located at $f_i = (i \pm 1/4)f_S$, where i is the alias index. Therefore, the centre frequency of the digital IF signal at the output of the modulator is at $f_S/4$. The desired RF alias (located at $M \times f_S/4$) would be attenuated as a result of subsampling, as illustrated in Figure 5-1.

[†] Clock feedthrough is a glitch caused by dispersing the charge due to the capacitive path between the control signals on the analog switch and analog signal passing through the switch

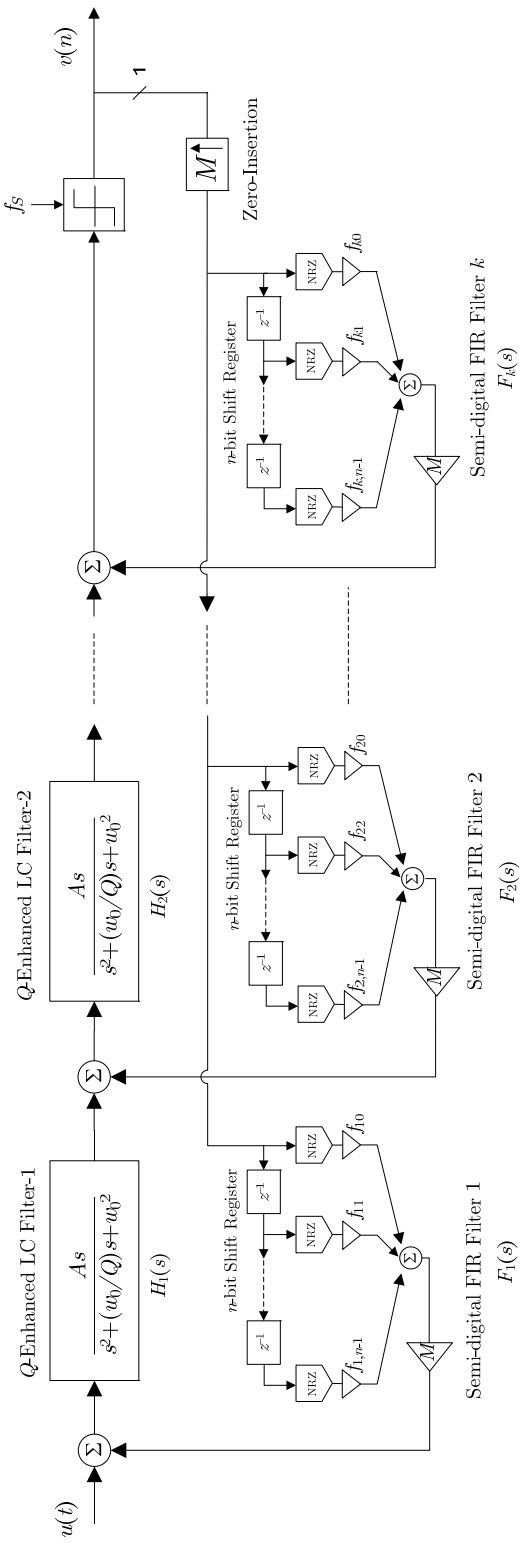


Figure 5-8 Topology of the proposed (k-1)$^{\text{th}}$ order subsampling modulator

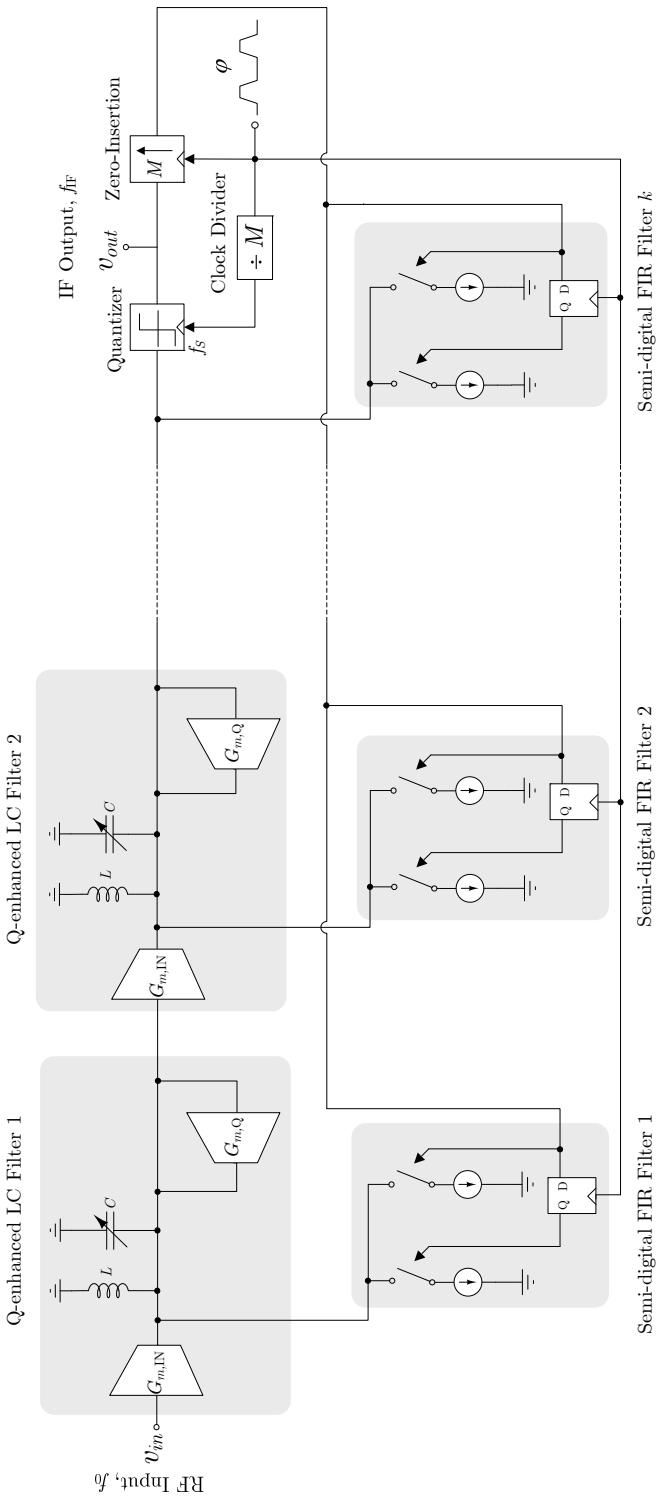


Figure 5-9 Circuit architecture of the proposed (k-1)$^{\text{th}}$ order subsampling modulator (Single-ended version shown for a clear illustration)

To compensate for this, the digital IF signal at the output of the single-bit quantizer is passed through a zero-insertion circuit to insert M–1 zeros between consecutive samples [Nad08]. This generates replicas of the alias located in the first Nyquist zone, which is only attenuated by a few dBs. The desired replica located at $M \times f_S/4$ would now have the same amplitude as the one in first Nyquist zone. In order to provide enough bandwidth for the RF alias, DAC current switches operate at $f_S \times M$, as shown in Figure 5-10. This implies that lowering sampling rate would result in amplified clock jitter at the output of the DAC. The use of NRZ feedback pulse for the DAC is desired here as it is easy to implement and have better jitter suppression than that of RZ and HRZ pulse shapes.

An LC resonator has a transfer function with a numerator having only band-pass terms as given in Equation (4.35). The lack of the s^0 term in the numerator hinders the matching of the modulator with its DT prototype since the set of linear equations used for matching is an overdetermined system[†] [Sho95b].

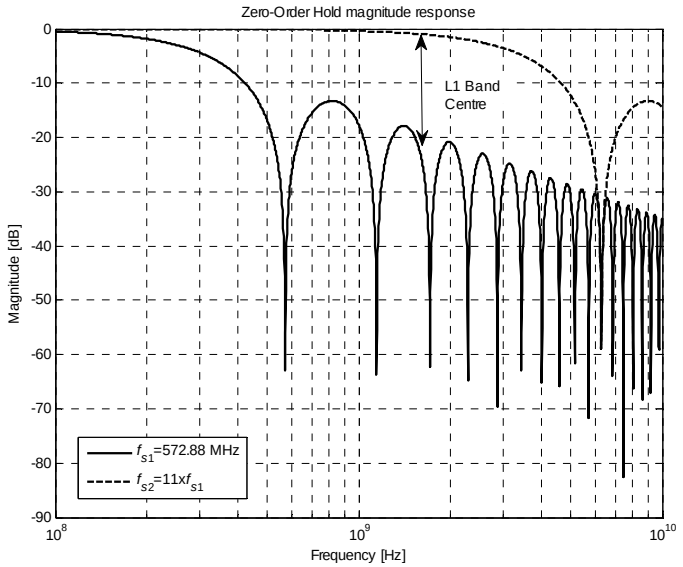


Figure 5-10 Extension of the DAC bandwidth by M=11

[†] A set of linear equations is overdetermined if there are more equations than unknowns. It is underdetermined if there are more unknowns than equations. Each unknown can be thought of as a degree of freedom while each equation can be thought as a constraint that restricts one degree of freedom.

Therefore, such a modulator, as illustrated in Figure 5-11, suffers from controllability issues. The s^0 (constant) term can be introduced in the numerator of the open-loop transfer function by adding damping resistors to the LC tank [Thu91]. However, this would further reduce the Q-factor of the loop filter. Therefore, it is avoided since the base Q-factor of the LC tank should be as high as possible in order to minimize the power consumption and the noise contribution of the negative resistance generation circuit. Shoaei and Snelgrove proposed a multi-feedback DAC approach to add more degrees of freedom to the system by utilizing a combination of feedback RZ/HRZ-DAC [Sho95b]. While the multi-feedback design provides a unique solution for the set of linear equations, the RZ/HRZ-DAC combination is more susceptible to clock jitter than the NRZ-DAC and degrades the SNR by more than 12dB [Tha06]. To enable the use of NRZ only feedback pulse, the signal at the output of the zero–insertion circuit is shifted in time as it is weighed and converted to analog at each stage by single-bit NRZ–DACs. The use of semi-digital FIR filters introduce sufficient degrees of freedom into the system to provide a unique solution for the set of linear equations. Additional clock jitter suppression is provided as semi–digital FIR filters give multi-level CT output. Furthermore, FIR filters act as a reconstruction filter and help attenuate the aliases located in the sampled spectrum between DC and $f_S \times M/2$, thus reducing the harmonic distortion at the output of the modulator. One disadvantage of the NRZ DAC pulse is its poor ELD performance; however, this is compensated by inserting an additional feedback path after the last LC filter [Ben97]. The semi–digital FIR filters have a gain factor of M since, spectrally, the upsampled signal is an M–fold compressed version of the original signal.

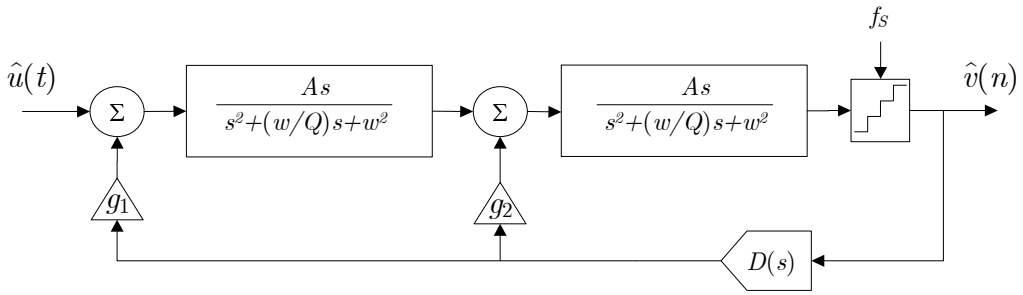


Figure 5-11 Topology of the fourth-order band-pass modulator lacking enough degrees of freedom for DT-CT equivalence

5.3 System-Level Design

The first step in the design of ΔΣ modulators is to establish the input dynamic range, bandwidth and maximum clock frequency requirements for the target application. Once these requirements are established, OSR, loop filter order, $|\mathrm{NTF}|_\infty$, and the target process technology can be determined.

For verification and performance evaluation purposes, the proposed modulator is designed with a fourth-order loop filter centred at GPS L1 band centre (1.57542GHz) and with $|\mathrm{NTF}|_\infty$=1.5. The transfer function of the prototype fourth-order, $f_s/4$ DT loop filter is obtained by frequency translating the second-order low-pass filter:

$$\begin{aligned} H_{LP2}(z)\Big|_{z^{-1}\to -z^{-2}} &= H(z) = \left.\frac{0.7749z^{-1} - 0.5585z^{-2}}{\left(1 - z^{-1}\right)^2}\right|_{z^{-1}\to -z^{-2}} \\ &= \frac{-0.7749z^{-2} - 0.5585z^{-4}}{\left(1 + z^{-2}\right)^2} \end{aligned} \tag{5.6}$$

NTF zeros of the DT prototype are put together at $f_S/4$, which constructs Butterworth filter. Although this is not desirable for wideband applications, realizing Chebyshev type-II or elliptic zeros require local feedback paths, which increase the hardware complexity of the modulator.

5.3.1 Modulator Topology

The fourth-order band-pass modulator is generally considered as the a good trade-off between dynamic range and stability as higher-order modulators have a tendency towards instability. The generalized fourth-order order topology for the proposed modulator is depicted in Figure 5-12(a) and some special cases of the generalized topology are introduced in Figure 5-12(b), (c), and (d). Here, LC filters are assumed identical and the number of taps for each FIR filter is assumed equal in order to limit the design parameters. The next step in the design procedure is to calculate the coefficients of the FIR

filter that satisfy the DT-CT equivalence. The DT-CT equivalence for the generalized fourth-order topology in Figure 5-12 can be written as:

$$H(z) = \hat{H}(z) \triangleq \text{IIT}\left\{\left[H_1(s)H_2(s)F_1(s) + H_2(s)F_2(s) + F_3(s)\right]e^{-sT}\right\} \quad (5.7)$$

In Equation (5.7), the term e^{-sT} represents the intentional full-cycle delay introduced before the feedback DAC to compensate for the signal-dependent ELD. To simplify the mathematical analysis, LC filters are assumed to have infinite Q-factor:†

$$H_1(s) = H_2(s) = \frac{As}{s^2 + \omega_0^2} \quad (5.8)$$

A comparison for the number of equations vs. unknowns (FIR filter coefficients) is given in Table 5-1. Clearly, the number of equations for the DT-CT equivalence depends on the number of taps in each FIR filter. As can be observed from Table 5-1, a unique solution set is available for Special Case–III and the generalized fourth-order topology whilst the rest of the configurations are underdetermined or overdetermined. Once the DT-CT equivalence is formulated, the unique solution set, as given in Table 5-2, can be obtained with the help of the MATHEMATICA function "SolveAlways".

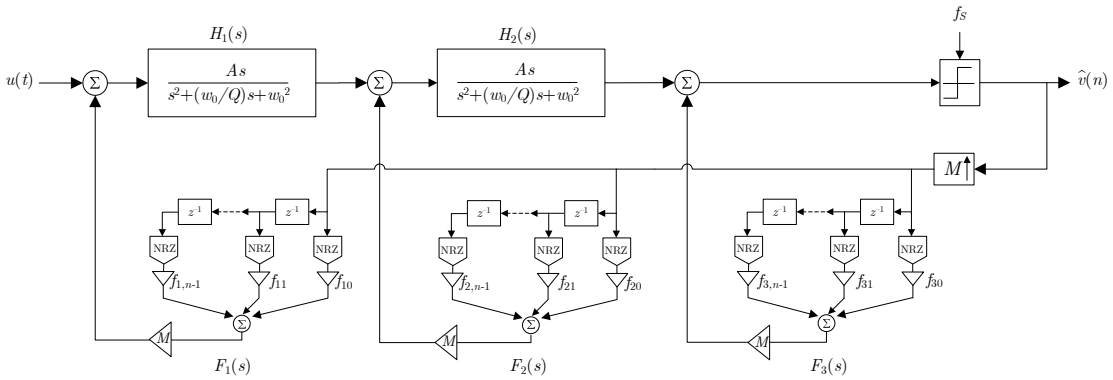
Table 5-1 The number of unknowns vs. equations for the DT-CT equivalence

Modulator	(# of Coefficients → # of Equations)			
Special Case-I	(2→5)	(3→6)	(4→7)	(5→8)
Special Case-II	(4→5)	(6→6)‡	(8→7)	(10→8)
Special Case-III	(4→6)	(6→7)	(8→8)†	(10→9)
Generalized	(6→6)*	(9→7)	(12→8)	(15→9)

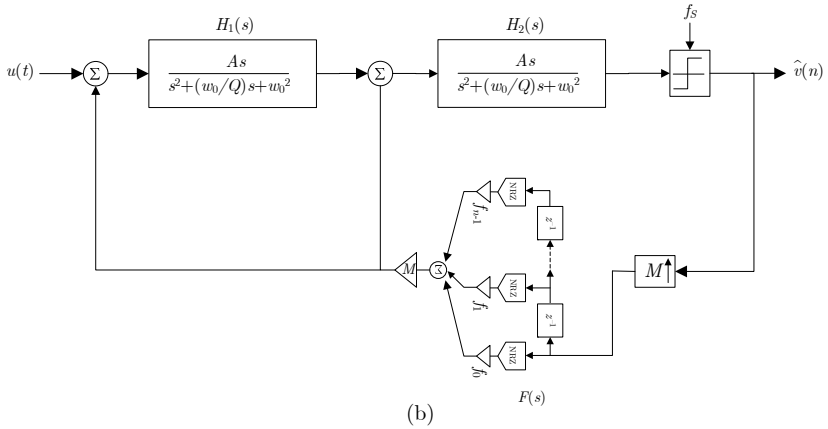
† Once the coefficients of the FIR filters are calculated, a finite Q-factor can be introduced in behavioural simulations

‡ Equations are not linearly independent therefore there is no unique solution for the set of linear equations

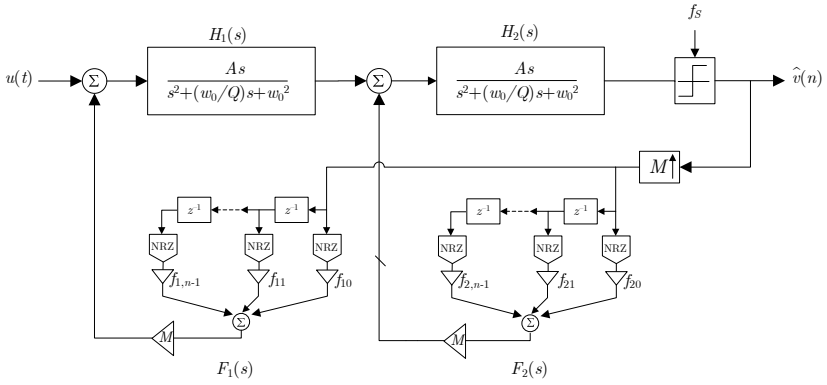
† Unique solution



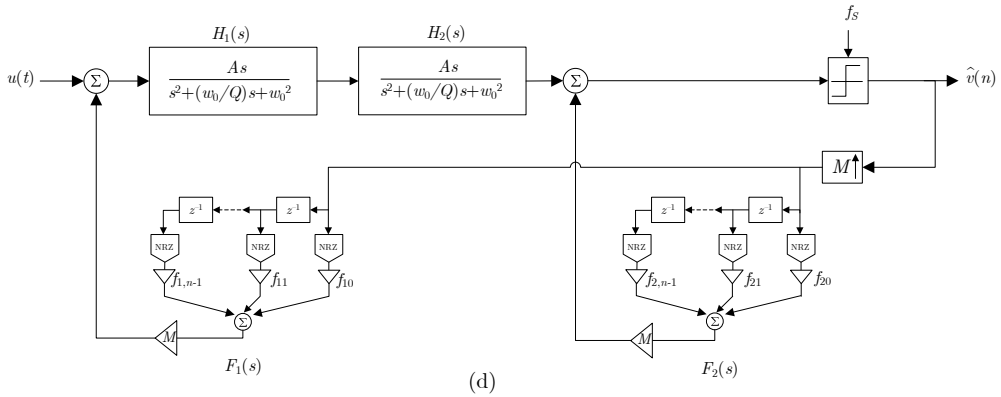
(a)



(b)



(c)



(d)

Figure 5-12 (a) Generalized fourth-order topology of the proposed modulator (a) Special Case-I (b) Special Case-II (c) Special Case-III

Table 5-2 Unique solution set

Coefficients	Special Case-III	Generalized
f_{10}	$-\frac{0.7785}{A^2T^2}$	$-\frac{0.1699}{A^2T^2}$
f_{11}	$-\frac{0.7785}{A^2T^2}$	$-\frac{0.1699}{A^2T^2}$
f_{12}	$-\frac{0.6086}{A^2T^2}$	–
f_{13}	$-\frac{0.6086}{A^2T^2}$	–
f_{20}	0	$-\frac{0.6086}{AT}$
f_{21}	–0.5270	$-\frac{0.6086}{AT}$
f_{22}	0	–
f_{23}	0.1937	–
f_{30}	–	0
f_{31}	–	–0.3333

When SolveAlways function does not return any solutions, linear programming techniques can be used [Lue08] in order to find a best-fit solution set that minimizes a certain cost function. Furthermore, additional equations can be introduced to find solutions to satisfy certain design constraints in underdetermined systems. One design constraint for the $f_s/4$ modulator could be to avoid the attenuation of the feedback signal centred at:

$$\omega_c = 2\pi f_c = \frac{\pi}{2T} \tag{5.9}$$

by the FIR filters. In the z-domain this constraint translates to:

$$\begin{aligned} \left|F(z)\right|_{z=j} &= \left(f_0 - f_2 + f_4 - \ldots + f_{n-1}\right) + j\left(-f_1 + f_3 - f_5 + \ldots - f_{n-2}\right) = 1 \\ &\rightarrow \begin{cases} f_0 - f_2 + f_4 - \ldots + f_{n-1} = 1 \\ -f_1 + f_3 - f_5 + \ldots - f_{n-2} = 0 \end{cases} \end{aligned} \tag{5.10}$$

However, finding approximate solutions with linear programming techniques is not necessary when unique solutions are available for Special Case-III and the generalized fourth-order topology. Therefore, we will focus our attention on these modulators with the coefficient sets that provide the full control on the CT modulator.

5.3.2 Aperture and Clock Jitter Model

As time-domain simulations with jittered clock edges are painfully slow especially in high-speed modulators, a behavioural model for the effect of aperture and clock jitter would be a useful tool. The dominant contributor of timing error in a sampler is the aperture jitter. For a sinusoidal signal, $x(\mathrm{t})=A\cdot\sin(2\pi f_0 t)$, the error at the output of a sampler can be approximated as [Mal03]:

$$x\left(t+\Delta T_{\mathrm{AJ}}(n)\right)-x(t)\approx 2\pi f_0\cdot\Delta T_{\mathrm{AJ}}(n)\cdot A\left(\cos 2\pi f_0\right)=\Delta T_{\mathrm{AJ}}(n)\frac{dx(t)}{dt} \quad (5.11)$$

where $\triangle T_{\mathrm{AJ}}(n)$ is the i.i.d. aperture jitter random variable for the n^{th} sampling instant with a standard deviation σ_{AJ}. Equation (5.11) can be used to model the effects of aperture jitter in a CT-ΔΣ modulator as illustrated in Figure 5-13.

On the other hand, the error sequence at the output of the DAC due to clock jitter, as illustrated in Figure 5-14(a), can be related to the modulator output signal as [Dun92]:

$$\varepsilon_J(n)=\frac{\Delta A(n)}{T}=\left[v(n)-v(n-1)\right]\frac{\Delta T_{\mathrm{CJ}}(n)}{T} \quad (5.12)$$

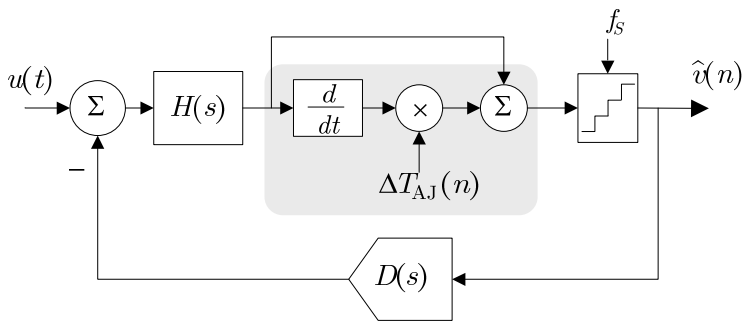


Figure 5-13 Fast aperture jitter error model for behavioural simulations

where $\Delta T_{\mathrm{CJ}}(n)$ is the i.i.d. clock jitter random variable for the n^{th} sampling instant with a standard deviation σ_{CJ}. Jitter error power is the variance of $\varepsilon_J(n)$, which can be written as:

$$\sigma_{\varepsilon_J}^2 = \sigma_{\Delta v}^2 \frac{\sigma_{\mathrm{CJ}}^2}{T^2} \tag{5.13}$$

In the z-domain Equation (5.14) is written as:

$$E_J(z) = \frac{\Delta T(z)}{T} \otimes \left(V(z)\left(1 - z^{-1}\right)\right) \tag{5.14}$$

where $\otimes$ is the convolution operator. Equation (5.14) leads to the fast and accurate jitter error model for the modulator as illustrated in Figure 5-14(b).

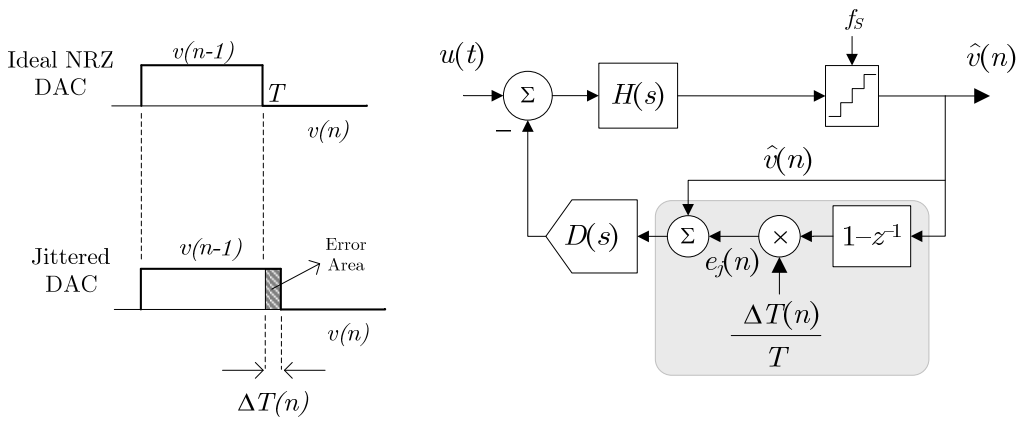


Figure 5-14 (a) Jittered single-bit NRZ-DAC (b) Fast clock jitter error model for behavioural simulations

5.3.3 Comparator Metastability

Metastability introduces a random delay in the feedback path, which randomizes DAC switching time [Dag04]. Therefore, comparator metastability in a ΔΣ modulator can be modelled in a similar manner to that of the clock jitter. Let the i.i.d. random variable for the delay caused by metastability for the n^{th} sampling instant be $\Delta T_M(n)$ and the standard deviation σ_M be a Gaussian distribution with zero mean. SNR degradation due to metastability can then be estimated by replacing $\Delta T_{\mathrm{AJ}}(n)$ with $\Delta T_M(n)$ in the clock jitter error model given in Figure 5-14(b). It should be noted that metastability

error at the output of the FIR filter whose output is directly fed into the quantizer is negligible since, in this case, this "noise" shaped by the NTF of the modulator. The combined error power due to clock jitter and comparator metastability can be written as:

$$\sigma_{JM}^2 = \sigma_{\Delta v}^2 \frac{\sigma_{\mathrm{CJ}}^2 + \sigma_M^2}{T^2} \tag{5.15}$$

assuming jitter and metastability random variables are uncorrelated.

5.4 Simulation Method

In order to determine the dynamic range of ΔΣ modulators, we follow the method introduced in [Sch93]. The smallest input applied to the modulator that gives 0dB SNR is called the In-Band Noise (IBN) [Che98]. Once the IBN is determined, the magnitude of the input tone can be slowly increased to find the Maximum Stable Amplitude (MSA). Once these two points are established, the dynamic range of the modulator can be calculated as:

$$\mathrm{DR}\,[\mathrm{dB}] \triangleq 20 \log 10 \left(\frac{\mathrm{MSA}}{\mathrm{IBN}} \right) \tag{5.16}$$

Time-domain behavioural simulations were performed with MATLAB/SIMULINK [Mat10] in order to evaluate the estimated performance of the proposed modulators. The frequency of the input tone is set to L1-E1 centre frequency, 1.57542GHz, and subsampling ratio is set to M=11, which gives a sampling rate of 572.88MHz. The ode8 (Dormant-Prince) solver is utilized with a fixed step size of 1.57542×10^{-9}s. For each simulation, 8192-point FFT is calculated to determine the SNR of the modulator. The dynamic range of the ideal fourth-order modulator with the transfer function given in Equation (5.6) when the OSR is varied between 128, 64, and 32 is 97dB, 78dB, and 61dB, respectively. Dynamic range of the modulators for OSR=64 (4.47MHz bandwidth) under the following testing conditions are illustrated in Figure 5-15 and Figure 5-16:

- 0.1% (1.7456ps) RMS aperture jitter on the sampler
- 0.5% (0.7934ps), 1% (1.5860ps), and 1.5% (2.380ps) RMS clock jitter on the NRZ-DACs
- $k_B T_K / C$ thermal noise (C_S=1.5pF, T_0=300°K)
- An enhanced Q-factor of Q_E=200

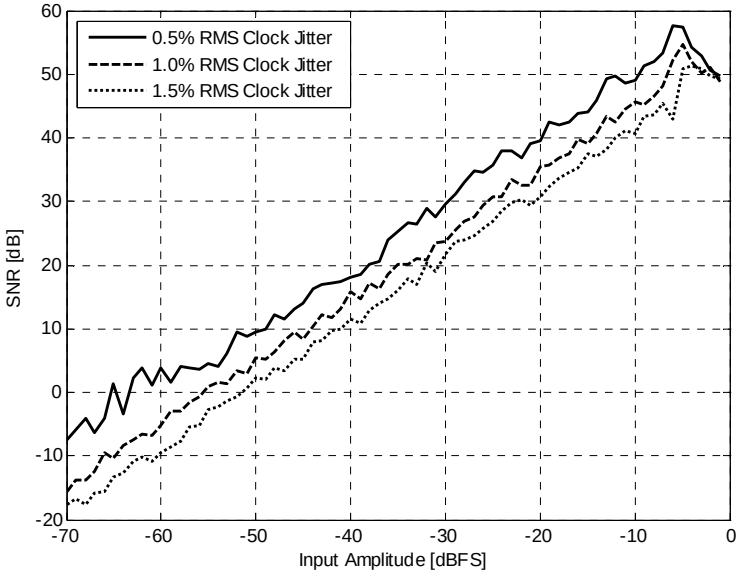


Figure 5-15 Input Amplitude vs. SNR for Special Case-III
(M=11, OSR=64, 4.47MHz Bandwidth)

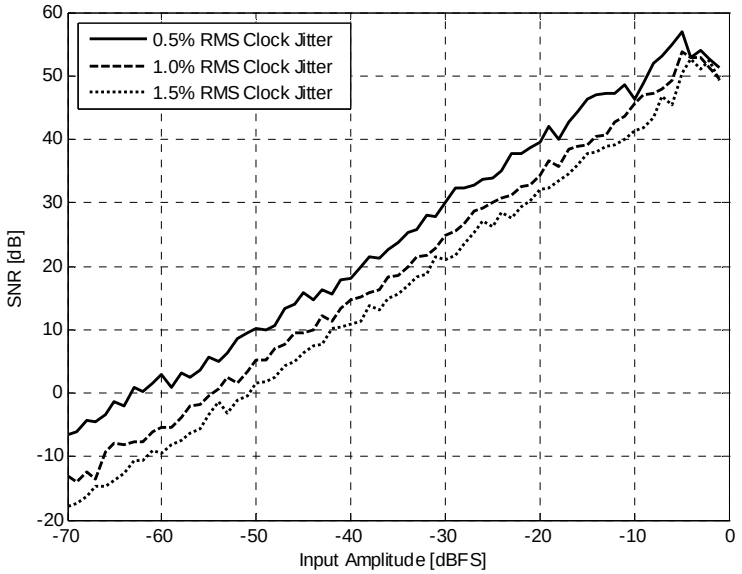


Figure 5-16 Input Amplitude vs. SNR for the generalized fourth-order topology
(M=11, OSR=64, 4.47MHz Bandwidth)

The total number of analog levels at the output of the FIR filters is shown in Table 5-3. As the dynamic range and the peak SNR for both modulators are almost identical, the generalized fourth-order topology is favourable to Special Case-III, which has two less filter taps.

In order to test inherent AA filtering characteristic, a CW interferer with –3dBFS amplitude centred at 1.52542GHz is placed at the input of the generalized fourth-order modulator [‡] along with the desired RF signal at 1575.42MHz having the same amplitude. The interferer at 1.52542GHz aliases back to 93.22 and 193.22MHz as a result of subsampling. The amount of suppression on the interferer is illustrated in Figure 5-17 for different values of the enhanced Q-factor. The effect of Q-factor enhancement on noise shaping can also be clearly observed in Figure 5-18. As the subsampling ratio increases, the effective Q-factor of the modulator is reduces, which degrades the sharpness of the notch at the centre frequency, eventually causing instability in the modulator. Therefore, Q-enhancement is essential in the proposed subsampling modulator.

Table 5-3 The number of analog levels at the output of the semi-digital FIR filter

Modulator	# of Taps	# of Levels
Special Case-III	8	10
Generalized	6	9

[‡] Simulations are performed with 0.1% (1.7456ps) RMS aperture jitter on the sampler and 1% (1.5860ps) RMS clock jitter on the NRZ-DACs

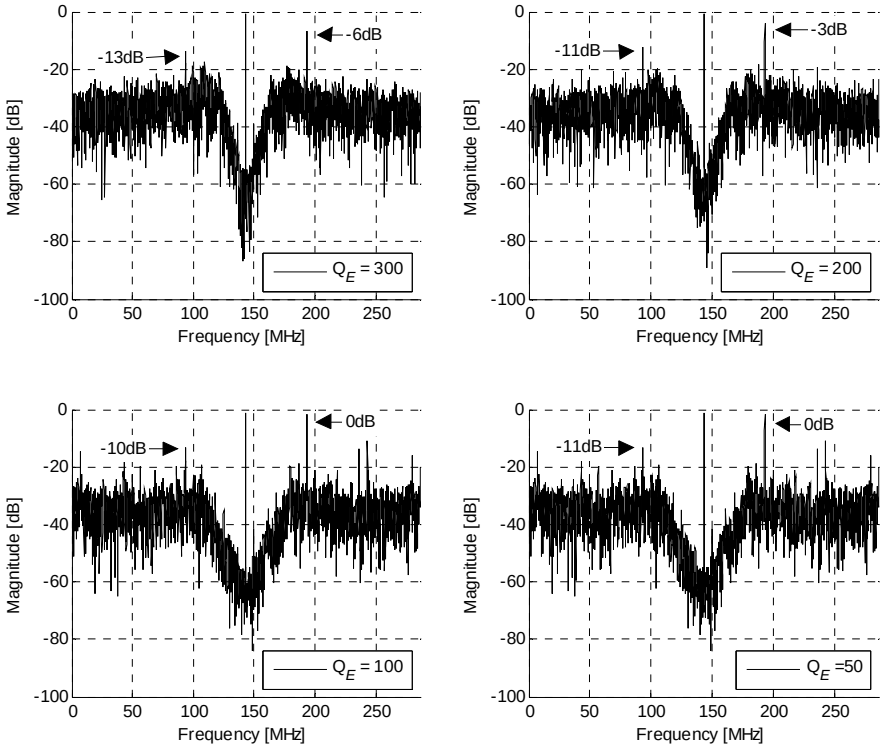


Figure 5-17 CW interferer suppression using inherent AA filtering (M=11)

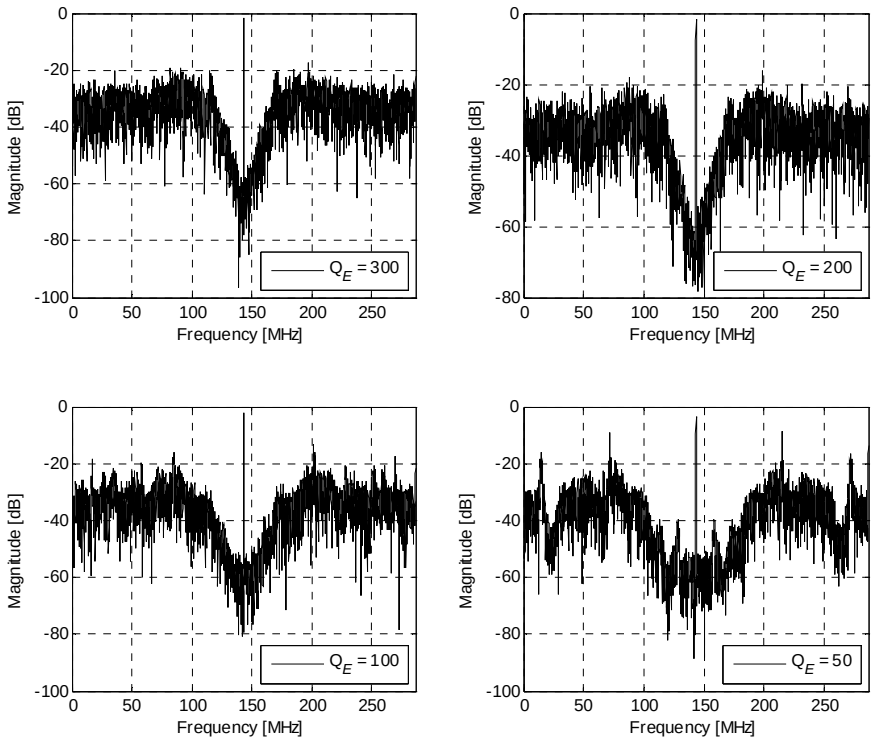


Figure 5-18 The effect of Q-factor enhancement on noise shaping (M=11)

5.5 Circuit-Level Design

As demonstrated in Section 5.4, the generalized fourth-order topology has almost equal dynamic range as with the added benefit of requiring two less filter taps. This section presents the circuit-level design for the generalized fourth-order topology.

5.5.1 Process Technology

The maximum clock frequency required for the proposed CT-ΔΣ modulator is determined from the clock rate of the DACs as the bandwidth of the DACs must be high enough not to attenuate the RF alias in the feedback path of the modulator. The highest frequency component belongs to the L1-E1 band; therefore, the maximum clock rate is $f_{\mathrm{L1}}\times 4 = 6.30168\mathrm{GHz}$ for the $f_S/4$ modulator. This suggests that the target technology must have transistors with $f_{\mathrm{T}} \geq 32\mathrm{GHz}$ as explained in Section 4.5.

Gallium Arsenide (GaAs) process technology dominates the RFIC market since it offers superior RF performance such as low-noise, high f_{T}'s, and high inductor Q's. However, GaAs comes at a cost of high power dissipation and low-yield. Low-cost and low-power consumption are essential for mobile, mass-market GNSS applications. Fortunately, there has been a trend towards integrating RF circuitry in CMOS and BiCMOS technologies. Considering that $f_{\mathrm{T}} \geq 32\mathrm{GHz}$; 0.35$\mu$m or down SiGe BiCMOS and 0.18μm or down RF CMOS processes would meet the requirements [Sch95], [Hen01]. SiGe BiCMOS is better suited for RF/analog IC designs than RF CMOS and is generally preferred when the target application predominantly comprises RF/analog circuitry [Paw06]. BiCMOS also offers better noise immunity; however, noise requirements are relaxed when a CT-ΔΣ modulator is utilized for A/D conversion. In a GNSS receiver, the digital circuitry would occupy larger chip area, which makes the mature CMOS technology more attractive due to the smaller die sizes and lower manufacturing costs.

The circuit-level simulations in this section are performed using the CADENCE SPECTRE [Spe10] simulator with TSMC 90nm RF CMOS PDK,

which are available to University of Westminster through the Europractice IC Service [url11]. TSMC PDK provides both mixed-signal and RF models for SPECTRE simulations. RF device models ("nmos_rf"/"pmos_rf" for NMOS/PMOS) are preferred in *Q*-enhanced LC filter simulations as they are based on physical measurements taken for a range of frequencies. Mixed-signal device models ("nch"/"pch" for NMOS/PMOS) are based on BSIM [url12] and do not accurately model the parasitic elements introduced at high frequencies. As RF device models are based on actual measurements, the Width (W) and Length (L) of devices are limited to a certain range. Hence, W/L ratio for MOSFET RF models cannot be greater than 50 assuming a minimum length of L=100nm. The user has the option of modifying the poly Finger Count (FC) to increase the total area of the device.

5.5.2 *Q*-Enhanced LC Filter

A typical differential *Q*-enhanced LC filter is depicted in Figure 5-19. The filter incorporates an input transconductance with inductive source degeneration, NMOS-PMOS cross-coupled pair, and an LC tank. Symmetrical inductors and varactors may be employed in the tank to obtain a fully-differential structure. Inductive degeneration enabled by L_S improves the linearity of the input stage and provides a good input impedance matching. The NMOS-PMOS cross-coupled pair is opted for the positive feedback as it provides a higher negative resistance than that of the NMOS-only pair introduced in Section 4.5.6 for a given bias current at the expense of reduced output swing and increased parasitic capacitance. The negative resistance provided for the LC tank can be written as:

$$R_{\mathrm{NEG}} = R_{\mathrm{NMOS}} + R_{\mathrm{PMOS}} = -\frac{2}{g_{m,\mathrm{M3}}} - \frac{2}{g_{m,\mathrm{M5}}} \tag{5.17}$$

and the transfer function of the filter can be expressed as [Gee05]:

$$H(s) = \frac{s\dfrac{G_{m,\mathrm{IN}}}{C}}{s^2 + s\left(\dfrac{1}{R_P} - G_{m,Q}\right) + \dfrac{1}{LC}} \tag{5.18}$$

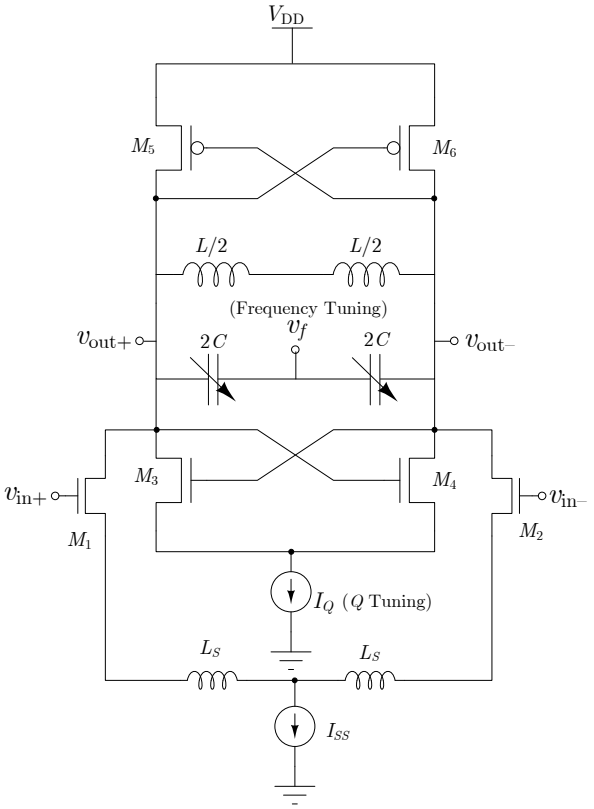


Figure 5-19 Q-enhanced LC filter with NMOS-PMOS cross-coupled pair and source degeneration inductors

where $G_{m,\mathrm{IN}}$ is the input transconductance that generates an output current to drive the LC tank. The input stage of the modulator is the most critical part of the circuit design since the dynamic range of the modulator cannot be better than the input stage [Che00]. In [Kuh95], the dynamic range of the Q-enhanced LC filter is derived as:

$$\mathrm{DR} \triangleq \frac{V_{\max}^2}{V_{\mathrm{noise}}^2} \approx \frac{V_{\max}^2 C}{k_B T\left(\xi+1\right)} \frac{Q_0}{Q_E} \tag{5.19}$$

where $V_{\max}$ is the maximum RMS signal voltage, V_{noise} is the RMS noise voltage, and ξ is the transconductor excess noise factor, typically ranging between 1 to 2. Equation (5.19) indicates that Q-enhancement actually lowers filter's dynamic range; therefore, base Q-factor should be as high as possible to minimize the reduction of the dynamic range by Q-enhancement. TSMC 90nm RF PDK has built in spiral inductors having Q-factors up 16.91 at L1-E1 frequency when L=3.146nH, as shown in Figure 5-20. Using the 3.146nH inductor, the total equivalent capacitance of the LC tank should be

C=3.243pF for the filter's centre frequency to be at 1.57542GHz. At this frequency, the Q-factor of the NMOS varactor is measured as Q_C=36.74, as shown in Figure 5-21.

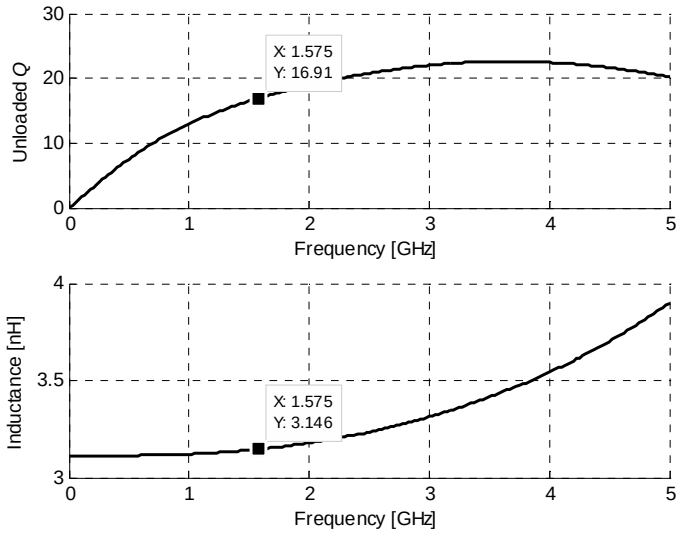


Figure 5-20 The variation of (a) Q-factor (b) Inductance with frequency for the 3.146nH spiral inductor (W=15μm, Inner Radius: 89μm, Turns: 3)

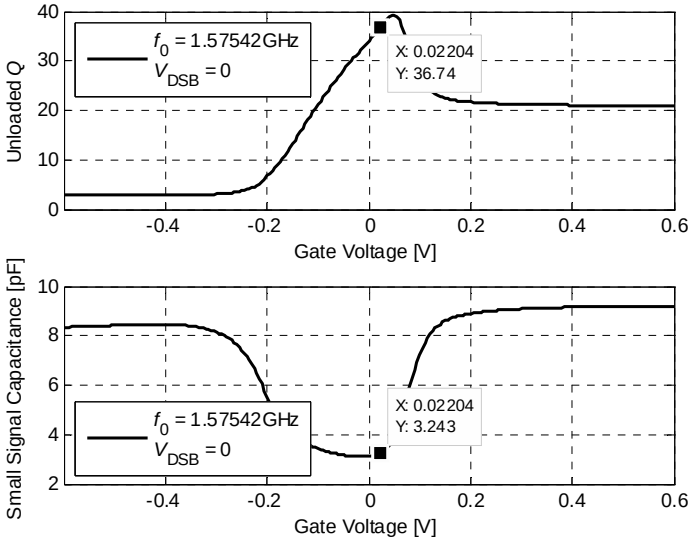


Figure 5-21 The variation of (a) Q-factor (b) Small signal capacitance with gate voltage at 1.57542GHz for the NMOS varactor (W=5μm, L=240nm, FC=50, Multiplier: 12)

Therefore, if the full frequency tuning were to be realized with an NMOS varactor, the base Q-factor of the LC tank would be Q_0=11.58. The maximum achievable dynamic range for the filter is then:

$$\mathrm{DR}_{\max} \approx 10 \times \log 10 \left(\frac{0.6^2 \times 3.24368 \times 10^{-12}}{2 \times 4.11 \times 10^{-21} \times 2.5} \frac{11.58}{200} \right) = 65.17\,\mathrm{dB} \qquad (5.20)$$

provided that ξ=1.5 and $V_{\max}$=0.6V. System-level behavioural simulations indicate the proposed fourth-order modulator has approximately 60dB dynamic range in 4.47MHz bandwidth (OSR=64) when subsampling ratio is M=11, as illustrated in Figure 5-16. Therefore, a Q-enhancement of 200 is possible without compromising modulator's dynamic rangeUsing SPECRE S-parameter analysis, the parallel equivalent resistance of the LC tank is having the 3.146nH inductor and C=3.243pF NMOS varactor is measured as R_P=351Ω at resonance. Based on this measurement, for the filter to have a Q-factor of Q_E=200, the negative resistance generated by the positive feedback should be R_{NEG}=–372Ω as can be calculated from Equation (4.42). At 27^{0}C, this can be reached by setting the bias current I_Q to 1.238mA, as shown in Figure 5-22.

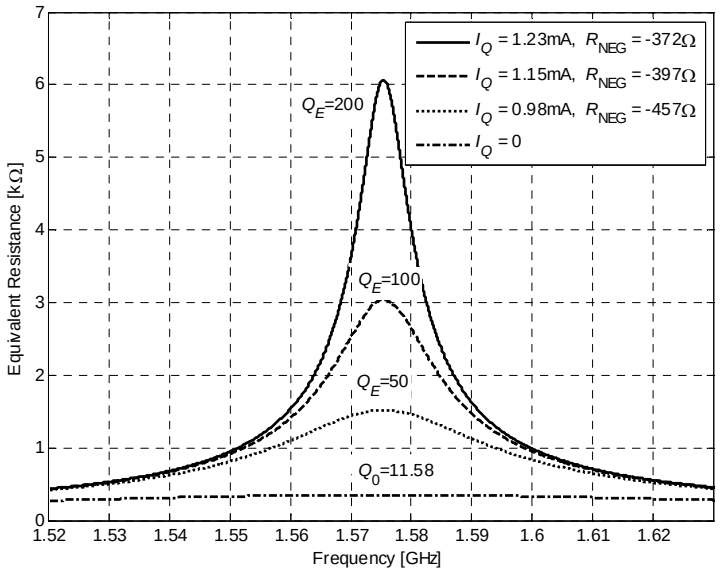


Figure 5-22 Required bias current I_Q for different values of Q

In reality, frequency/voltage dependent device parasitics will change the equivalent resistance and capacitance of the filter [Her99]. Therefore, the bias current required for a certain Q-factor will be more than what is shown in Figure 5-22, as given in Table 5-4.

Q and the centre frequency drift are unavoidable as both active and passive components of the filter are susceptible to PVT variations. In the LC tank, the drift is mostly due to varactors as the inductance value is primarily controlled by the spiral inductors dimensions, which is relatively unaffected by PVT variations [Kuh96]. As the capacitance and Q-factor of MOS varactors depend on both gate and drain-source to bulk voltage, it is more reliable to employ fixed Metal-Insulator-Metal (MiM) capacitors for coarse frequency tuning and a small MOS varactor for fine frequency tuning. This keeps the Q and frequency drift within a smaller range, as illustrated in Figure 5-23. On the other hand, when a high Q-enhancement is applied by the active circuitry, PVT variations may cause the filter to oscillate and hence to introduce instability in the CT-ΔΣ modulator. Monte Carlo simulations confirm there is no such risk with a nominal Q_E of 200, as illustrated in Figure 5-23. Nevertheless, an automatic tuning scheme is essential to keep Q and the centre frequency within the desired range.

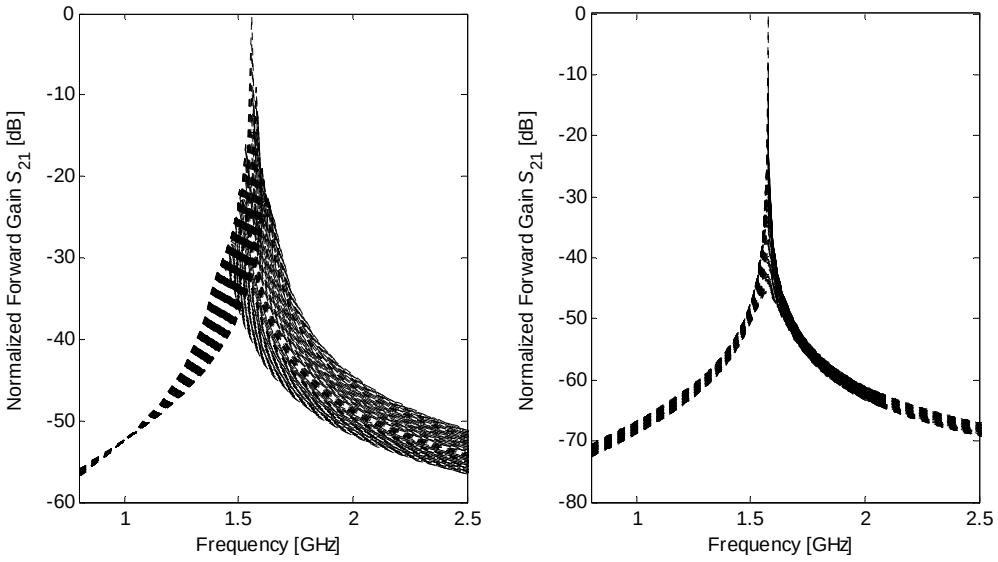


Figure 5-23 Q-factor and centre frequency variation in the filter (Q_E= 200, f_0=1.57542GHz) when (a) an NMOS varactor (b) an MIM capacitor with a small NMOS varactor is employed for frequency tuning

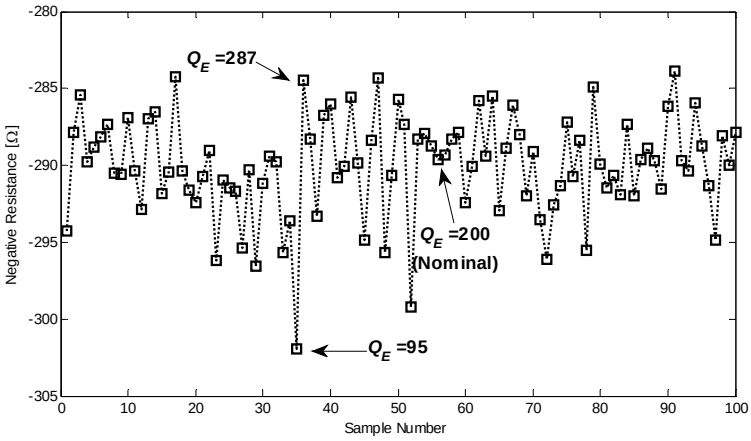


Figure 5-24 The effect of device mismatch on negative resistance (100 point Monte Carlo sampling)

5.5.3 Filter Tuning

The tuning circuit, as illustrated in Figure 5-25, realizes a modified version of the self-tuning procedure proposed in [Xin05]. The tuning circuit is a reduced-complexity alternative to Voltage-Controlled Filter (VCF) and VCO-based master/slave tuning methods [Kho84] [Tan78], as it does not require a slave filter or a PLL.

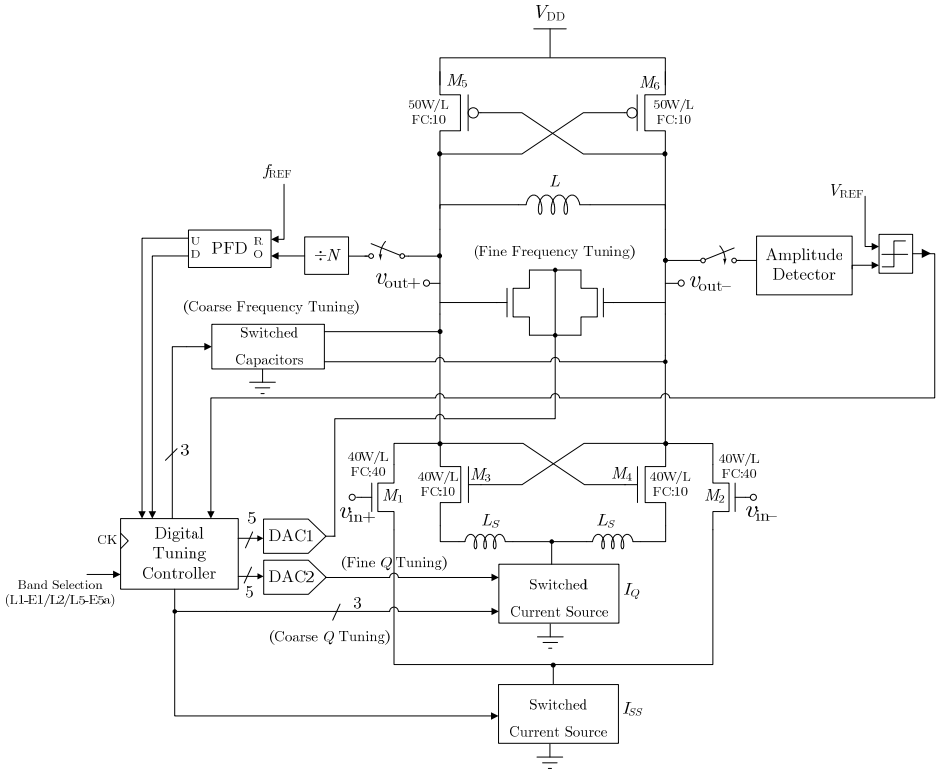


Figure 5-25 Q-enhanced LC filter with the proposed tuning circuit

As the CT-ΔΣ modulator is required to operate on three bands (L1-E1, L2, L5-E5a), the switched-capacitor network has three MiM capacitors for coarse frequency tuning, as illustrated in Figure 5-26(b). The nominal values for MiM capacitors, as given in Table 5-4, are calculated with taking device parasitics at relevant frequencies into account. Similarly, coarse Q-tuning is performed with a switched current source employing a regulated drain current mirror [Bak10], as illustrated in Figure 5-26(a). A similar structure is also used for the implementation of modulator's feedback DAC as explained in Section 5.5.6. A switched current source is also required for the input transconductance to match the transfer function of the filter given in Equation (5.18) with the one given in Equation (4.38). In Equation (4.38), A is taken as ω_0 and the input-refereed 1dB compression point (P1dB) for each case is measured using SPECTRE's Periodic Steady State (PSS) analysis, which is also given in Table 5-4. Figure 5-27 illustrates the input-refereed 1dB compression point measurement when the filter is operating on L2 band.

Table 5-4 Design Parameters for the Filter

Band	C_{MiM} [pF]	C_{MiM} W&L [µm]	I_Q [mA]	I_{SS} [mA]	P1dB [dBm]
L1-E1	2.6587	36.09	1.83	1.92	–11.75
L2	4.7578	48.34	2.61	6.09	–4.41
L5-E5a	5.2587	50.83	2.82	6.45	–4.17

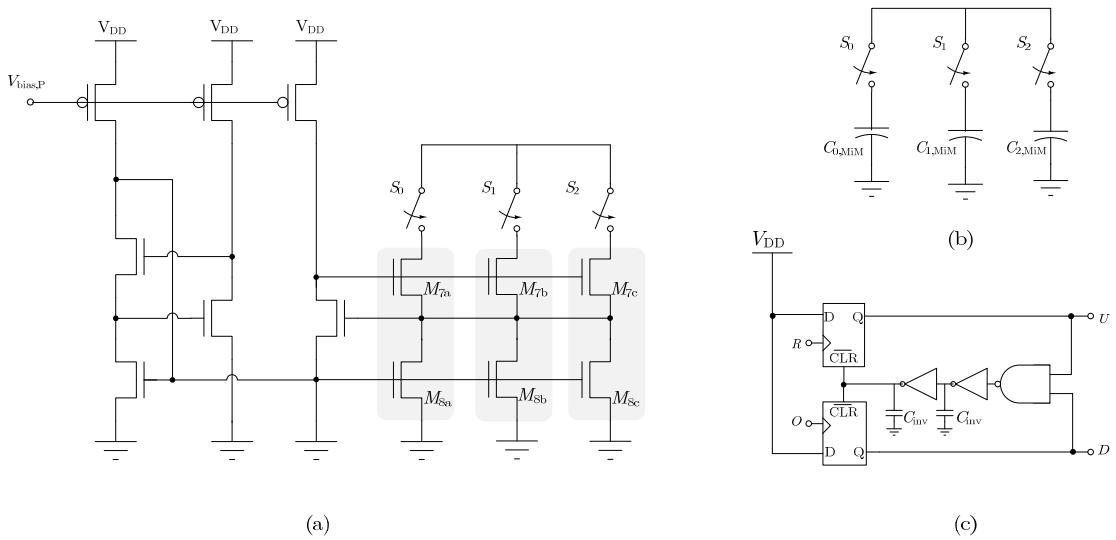


Figure 5-26 (a) Switched current source for coarse Q tuning (b) Switched-capacitor network for coarse frequency tuning (c) Phase-frequency detector

Fine frequency and Q-tuning, on the other hand, is realized with the help of a simple digital controller. The feedback from the comparator and Phase-Frequency Detector (PFD) [Gar79], as shown in Figure 5-26(c), can be used to gradually adjust the fine Q and frequency with the help of two voltage-mode SI DACs. The tuning procedure can be summarized as follows:

- Switch to the band of interest by turning on S_0 (L1-E1), S_1 (L2), or S_2 (L5-E5a) for coarse frequency and Q-tuning
- Increase the bias voltage $V_{\text{bias,P}}$ of the switched current source until the filter turns into an oscillator
- Fine-tune oscillation frequency
  - If the oscillation frequency after divide-by-N (f_{OSC}/N) is lower than the desired centre frequency ($f_{\text{REF}}\times N$), PFD's U-port output (up) starts generating pulses whilst D-port output (down) remains low. The outputs from U- and D-ports can be sampled within the digital controller in order to adjust the tuning voltage for the NMOS varactor with the help of a DAC. Since a DAC is used for updating the oscillation frequency, there may never be a phase/frequency lock. Therefore, the adjustment is terminated either when both outputs are low (lock indicator) or when D-port output starts generating pulses whilst U-port output remains low (nearest frequency after lock).

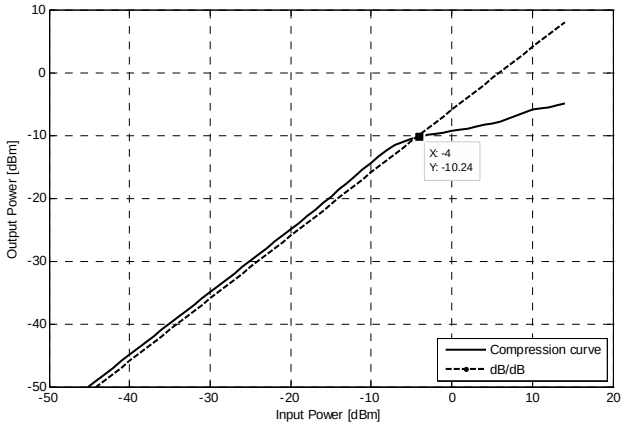


Figure 5-27 Input-referred 1-dB compression point of the filter (L2 band)

- Set V_{REF} for desired Q-factor after frequency adjustment is complete
  - As the filter is still in oscillation, the comparator output is low as V_{REF} is lower than the voltage level at the output of the amplitude detector. The DAC connected to the $V_{\mathrm{bias,P}}$ in Figure 5-26(a) is utilized to reduce the bias voltage until the comparator output goes high. The accuracy of the adjustment depends on comparator resolution as well as the number of bits used in the DAC. A discussion on comparator resolution is provided in Section 5.5.4.

As the oscillation frequency approaches to the desired frequency, the widths of the pulses generated by the PFD get narrower, making it difficult to sample PFD's outputs. Using a 62.5Msps sampler and sampling both at the rising and the falling edge, it takes approximately 325ns to detect the up pulse when the frequency mismatch is approximately 1%, as illustrated in Figure 5-28. The frequency resolution and detection time can be improved by increasing the sampling rate.

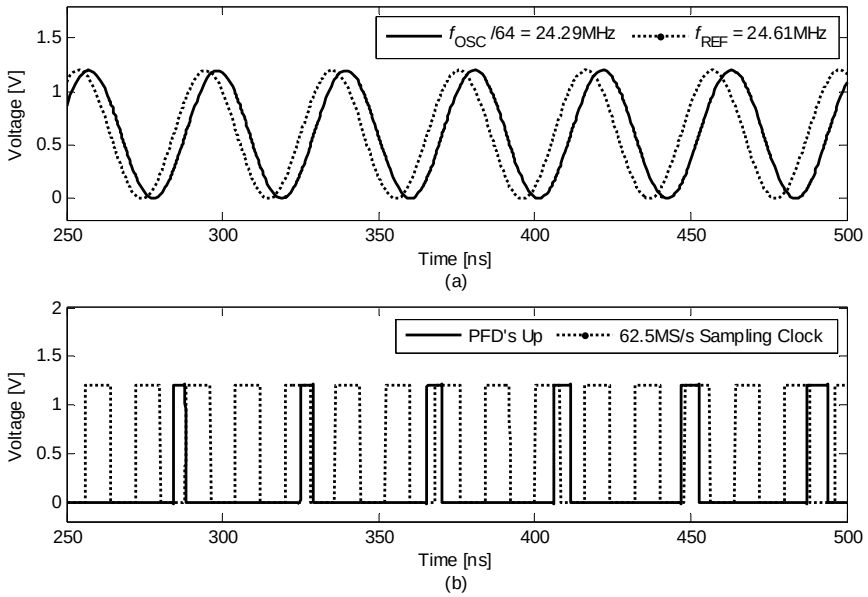


Figure 5-28 Transient simulation of the PFD (a) Reference signal and the output of divide-by-64 when filter is in oscillation (b) The pulse at the output of U-port and the sampling clock

A behavioural model of the digital controller is written in Verilog and integrated with the transistor-level design of the tuning circuit and the filter on VIRTUOSO in order to test the tuning procedure. Figure 5-29 illustrates filter's response when 5-bit DACs are used for fine-tuning with an average accuracy of 97% for frequency tuning and 90% for Q tuning.

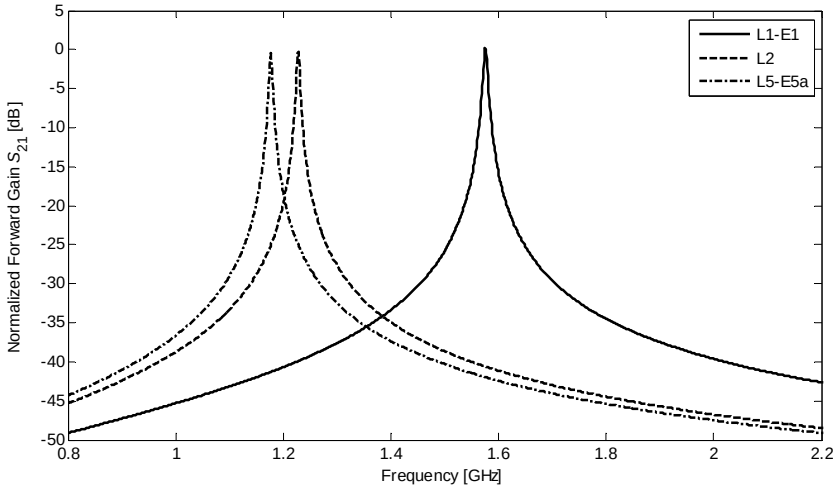


Figure 5-29 Filter's response to the tuning procedure (nominal $Q_E = 200$)

5.5.4 Quantizer

The single-bit quantizer employed in the proposed CT-ΔΣ modulator and the tuning circuit is a latched comparator as illustrated in Figure 5-30 [Bak10]. The quantizer incorporates a pre-amplifier to reduce the kick-back noise, a positive feedback for decision making, an output buffer, and an Set/Reset (SR) latch in order for the outputs change at the rising edge of the clock.

The input stage is a complementary differential pair for wide input swing, which is biased by M_1 and M_5. As explained in Section 4.5.5, when the sampling clock is high, the input stage amplifies the differential input and the voltage difference between v_{in+} and v_{in-} creates an imbalance between drain currents of M_{12} and M_{13}. When it is low, the positive feedback pushes the decision made to VDD or GND.

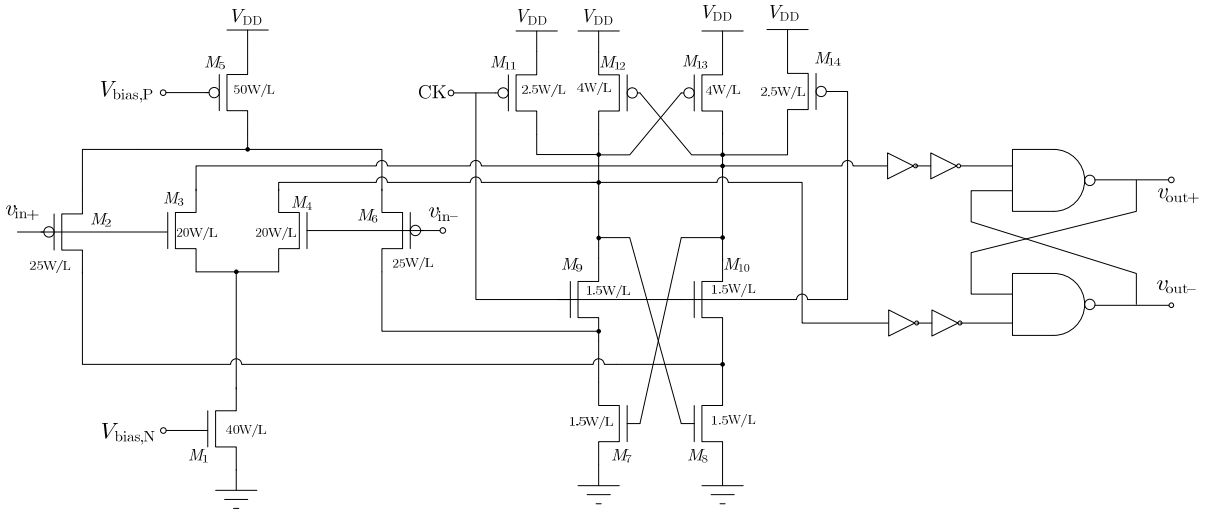


Figure 5-30 Single-bit latched comparator

Quantizer's sensitivity is proportional with pre-amplifier's power consumption. When 47.5μA is drawn from the supply, the smallest difference that can be discriminated is approximately 3mV, as shown in Figure 5-31(a). Figure 5-31(a) illustrates quantizer output going from low to high when v_{in+} is gradually increased with a step size of 1μV whilst v_{in-} is held at 600mV. The derivative of the transfer curve gives the quantizer gain, as shown in Figure 5-31(b). The propagation delay of the quantizer is measured as 870ps, as illustrated in Figure 5-32.

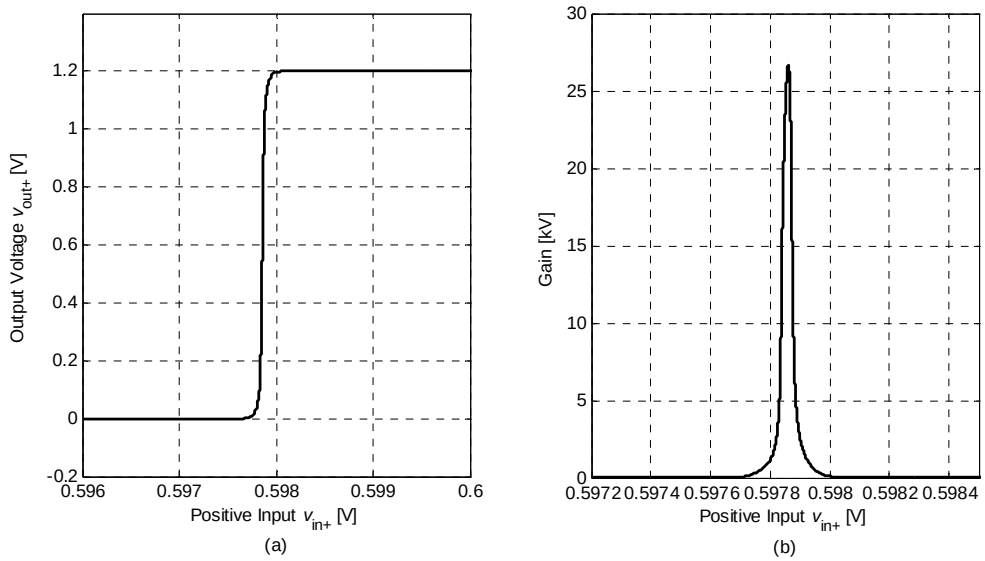


Figure 5-31 DC analysis of the quantizer

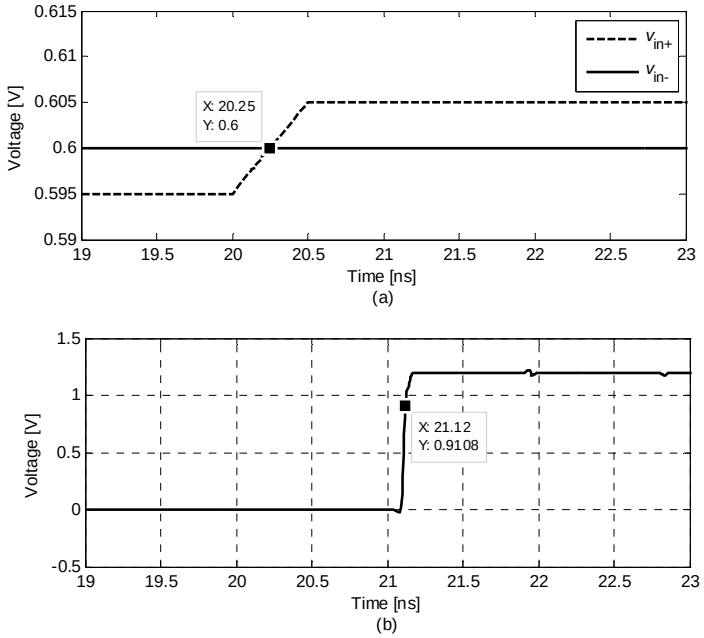


Figure 5-32 Transient simulation of the quantizer demonstrating the propagation delay (a) Voltage applied to the differential input (b) Quantizer output voltage

5.5.5 Zero-Insertion Upsampler

The zero-insertion upsampler is a simple digital circuit, which incorporates an modulo-M–1 counter and a multiplexer, as illustrated in Figure 5-33. The circuit inserts M–1 zeros between consecutive samples before the signal is transmitted to the semi-digital FIR filter. In a multi-band receiver, it would be feasible to operate the ADC with a variable sampling rate, as will be explained in Chapter 6. When this is the case, the upsampling factor M should to be programmable.

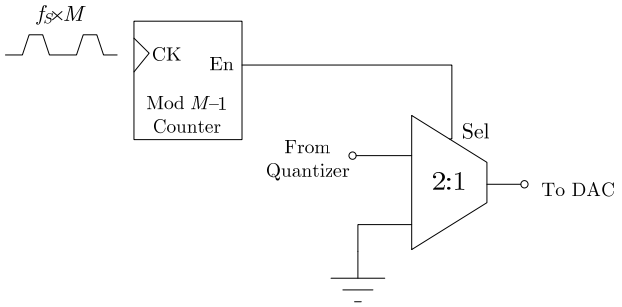


Figure 5-33 Block diagram of the single-ended zero-insertion upsampler

5.5.6 Semi-Digital FIR Filter

The generalized fourth-order topology for the proposed ΔΣ modulator comprises three two-tap semi-digital FIR filters in the feedback path for D/A conversion. The architecture of the two-tap differential semi-digital FIR filter is given in Figure 5-34. The current cell, which implements one tap of the FIR filter, incorporates a cascode current source and differential transmission gate switches, as illustrated in Figure 5-35.

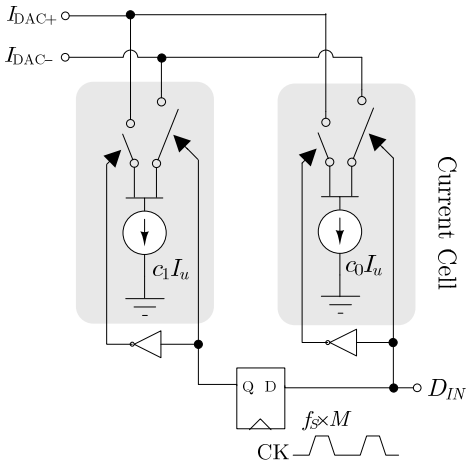


Figure 5-34 Two-tap semi-digital FIR filter with switched-current DACs

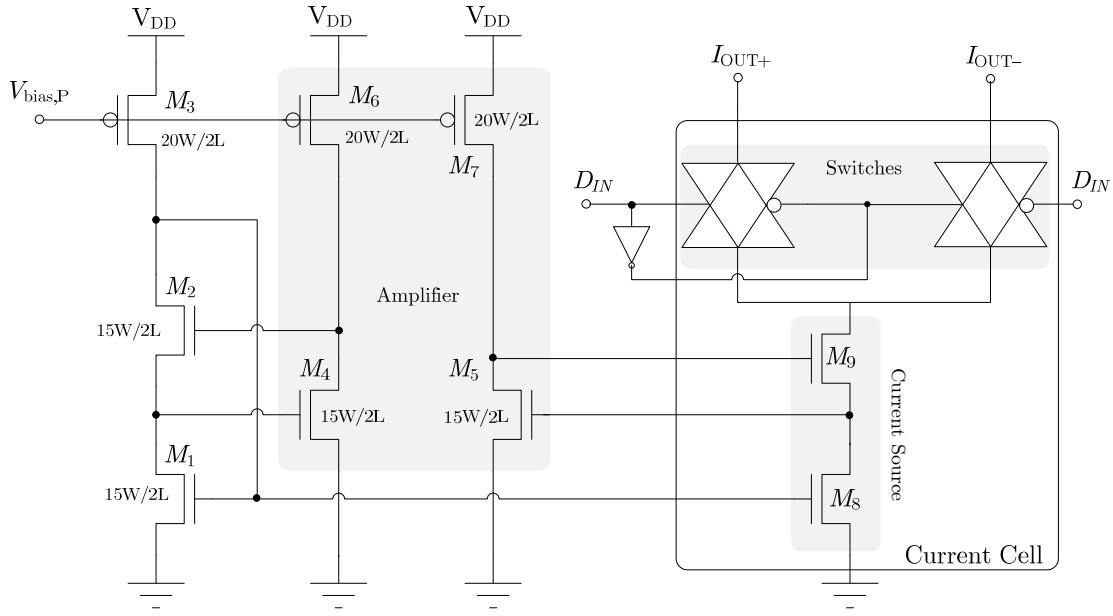


Figure 5-35 Current source driver and the current cell

A current source requires high output resistance to maintain near-ideal behaviour. Therefore, cascode current sources are used to reduce the effect of channel length modulation. Additionally, the wide-swing current mirror configuration improves the linearity of the current source [Bak10]. As M_3's drain-to-source voltage (V_{DS}) decreases, M_5's V_{DS} also decreases causing M_9's gate voltage to increase and restore the V_{DS} for M_3. Ideally, this would provide infinite output resistance for the current source as the M_3's drain current remains fixed. In practice, the output resistance is limited by the gain of amplifier employed with the current driver. The I-V curve for the current source is given in Figure 5-36 when it is designed to sink 4.961mA.

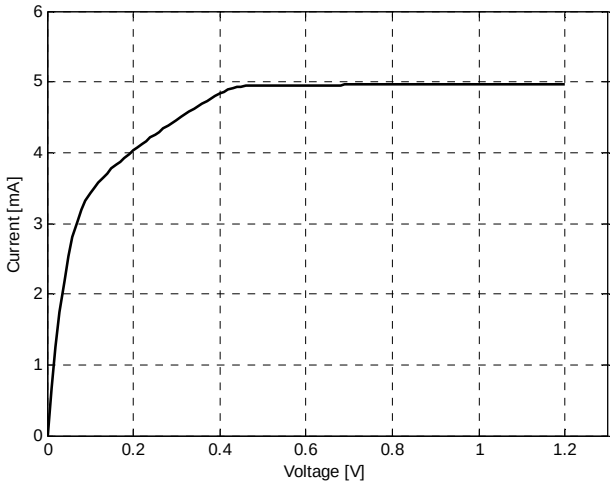


Figure 5-36 The I-V curve for the current source

The scaled and normalized coefficients of the semi-digital FIR filter is given in Table 5-5. When the unit current source, I_U, is taken as 10μA, the maximum current output required will be 4.961mA since the variation in the FIR filter coefficients to match the open-loop transfer function of the CT modulator with its DT prototype is quite large. The dimensions of M_8 and M_9 to implement the taps of the FIR filter are also provided in Table 5-5.

The on-resistance of the switches should be as low as possible to minimize the voltage drop over the switches. This requires long length devices, which results in large glitches as a result of increased gate capacitance. Differential transmission gate switches are used to minimize the size of the devices as well as the glitches caused by clock feedthrough. Figure 5-37 illustrates the switching performance of the transmission gates at 6.30168GHz.

Table 5-5 Scaled coefficients of the semi-digital FIR filter

F_1(s)	Normalized Value	Current Source [mA]	M_8 & M_9
f_{10}	1	4.961	4460W/2L
f_{11}	1	4.961	
F_2(s)			
f_{20}	9.594×10^{-3}	0.403	362W/2L
f_{21}	9.594×10^{-3}	0.403	
F_3(s)			
f_{30}	0	–	–
f_{31}	237.73×10^{-3}	0.010	10W/2L

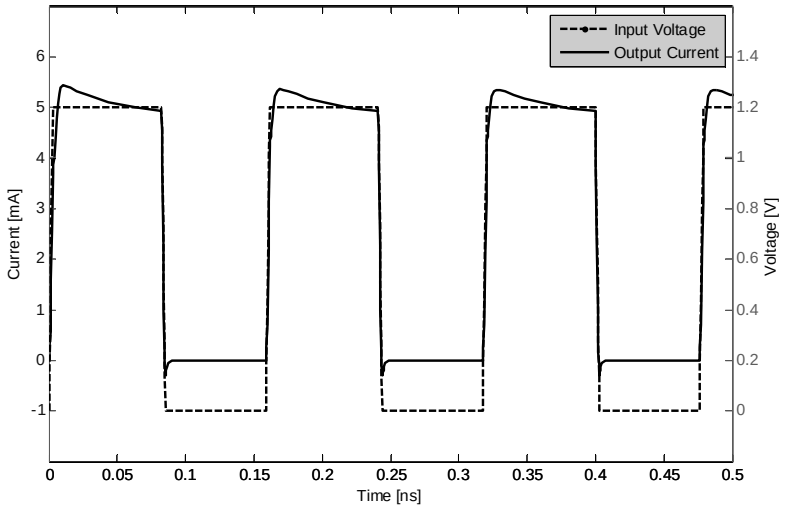


Figure 5-37 Transmission gates switching the 4.96mA current at 6.30168GHz

Variations in the nominal values of the current due to PVT variations as well as clock feedthrough will affect the open-loop transfer function of the modulator, but without introducing any distortion. Figure 5-38 shows the deviation in 0.403mA current source due PVT variations, which is used to implement the taps of the second FIR filter. Figure 5-39 illustrates the effect of current source PVT variations on the proposed modulator.

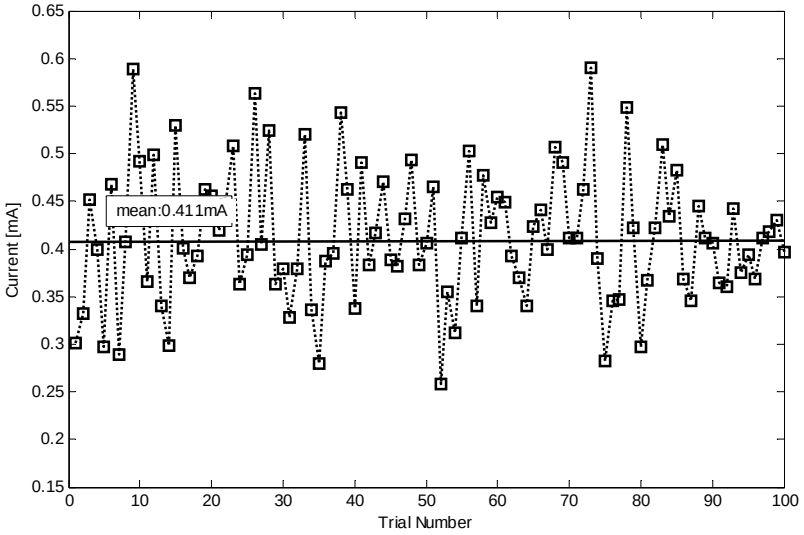


Figure 5-38 The effect of device mismatch on 0.403mA current source (100 point Monte Carlo sampling)

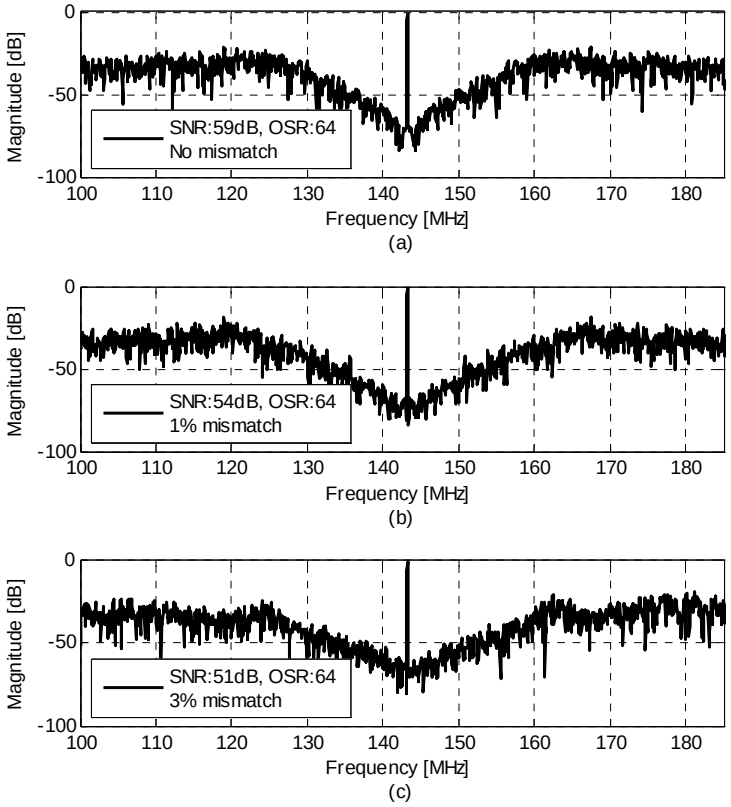


Figure 5-39 The effect of current source PVT variations on the proposed modulator (OSR=64, input tone: –3dBFS) (a) No mismatch results in 59dB SNR (b) 1% mismatch results in 54dB SNR (c) 3% mismatch results in 51dB SNR

Chapter 6

On the Design of a Novel Subsampling Receiver for Multi-Constellation GNSS

This chapter proposes a novel subsampling receiver architecture for multi-constellation GNSS applications. The proposed receiver replaces the commonly used Flash ADC with the novel subsampling CT-ΔΣ modulator introduced in Chapter 5. The use of the novel CT-ΔΣ modulator results in a reduced complexity solution for multi-constellation GNSS receivers as the amount RF components used in the front-end is minimized. A GNSS Toolbox for performing MATLAB/SIMULINK – CADENCE co-simulations for the proposed receiver is introduced in this chapter. It is demonstrated that the proposed receiver successfully acquires and tracks the civilian GPS/Galileo signals with high C/N_0.

6.1 System-Level Design Considerations

The proposed subsampling receiver architecture is given in Figure 6-1. System-level design considerations such as the noise budget, gain plan, and component selection are discussed in this section.

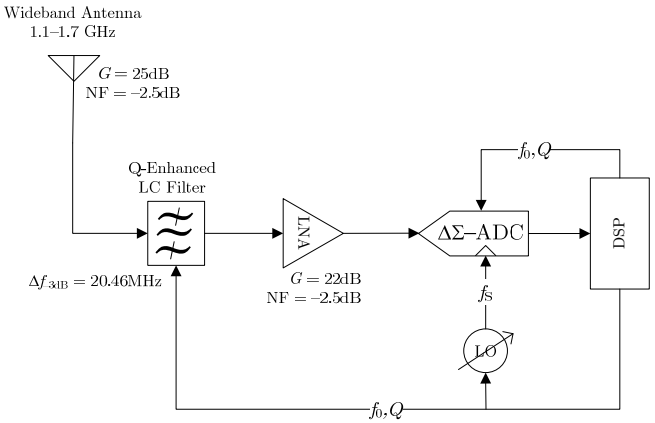


Figure 6-1 Proposed subsampling receiver architecture

6.1.1 Band Selection

The proposed receiver architecture employs the subsampling CT-ΔΣ modulator introduced in Chapter 5 for A/D conversion. The first step in the design of the modulator for a multi-constellation receiver is to establish how the radionavigation signals will be delivered to the DSP. The simultaneous processing of multi-carrier radionavigation signals is desirable, as this would enable estimating ionospheric delay. However, this is not possible with a single ΔΣ modulator. Instead of utilizing multiple modulators for this purpose, subsampling one signal at a time and adjusting the sampling rate of the modulator for tuning into another band as and when desired is favourable to reduce to cost and power consumption of the receiver.

In order to achieve a low NF, the first component after the antenna should be an amplifier. When an active antenna is used, two or three additional gain blocks are required to bring the thermal noise floor to the FSR of the ADC. While the CT-ΔΣ ADC incorporates a high-Q loop filter that also acts as an AAF, an RF filter after the antenna is still required to suppress the

out-of-band signals and to relax the linearity requirements of the LNA following the filter. Instead of employing an off-chip RF filter for each band, the Q-enhanced LC filter introduced in Section 5.5.3 is opted for the RF filter.

All civilian signals except for Galileo E5a are located at the centre of wider bandwidth military or restricted access signals. Therefore, the –3dB bandwidth of the RF filter can be extended beyond the null-to-null bandwidth of the civilian signals at the cost of increasing the thermal noise floor. As the noise budget of the receiver would be relaxed with the use of the novel CT-ΔΣ modulator, the bandwidth of the RF filter and is chosen as 20.46MHz for all signals. Therefore, the highest Q-factor required for the RF filter is Q_E=1575.42/20.46=77, as illustrated in Figure 6-2.

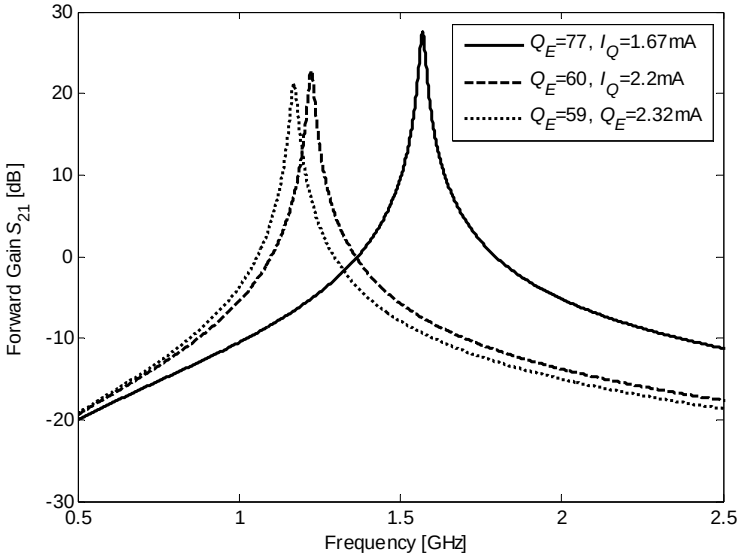


Figure 6-2 The Q-enhanced LC filter with a 20.46MHz bandwidth tuned for each band

6.1.2 Noise Figure

The required NF for each signal is calculated from Equation (3.3) and (3.4) and assuming that the minimum required post-correlation SNR is 10dB. As can be observed from Table 6-1, NF requirement for L5 and E5a are relaxed due to the relatively high processing gain. The most stringent noise figure requirement is for E1 OS and L1.

Table 6-1 Noise budget of the multi-constellation receiver

	GPS			Galileo	
	L1 C/A	L2C	L5	E1 OS	E5a
Carrier [MHz]	1575.42	1227.60	1176.45	1575.42	1176.45
Signal Bandwidth [MHz]	2.046	2.046	20.46	16.386	20.46
RF Filter Bandwidth [MHz]	20.46				
Thermal Noise Floor@290°K [dBm]	–100.86				
Min. Received Power [dBm]	–128.5	–130	–124	–124	–124
Input SNR [dB]	–27.64	–29.14	–23.14	–23.14	–23.14
Code Rate [Mcps]	1.023	1.023	10.23	1.023	10.23
Processing Gain [dB]	43.10	46.11	53.10	36.11	53.10
Min. Required NF [dB]	5.46	6.96	19.96	2.97	19.96

6.1.3 Gain Plan

When planning the gain of the GNSS receiver chain, one must be a careful not to raise the thermal noise floor above ADC's FSR. The FSR of the proposed CT-ΔΣ modulator can be found by dividing the current from the feedback DAC to the input transconductance of the first filter [Che98]. This gives 305mV peak-to-peak (V_{PP}) FSR for L1-E1, 120mV for L2, and 115mV for L5-E5a. With an ADC input impedance of R_{IN}=50Ω, the maximum allowable full-scale power that can be applied to the ADC is calculated from [Kes05]:

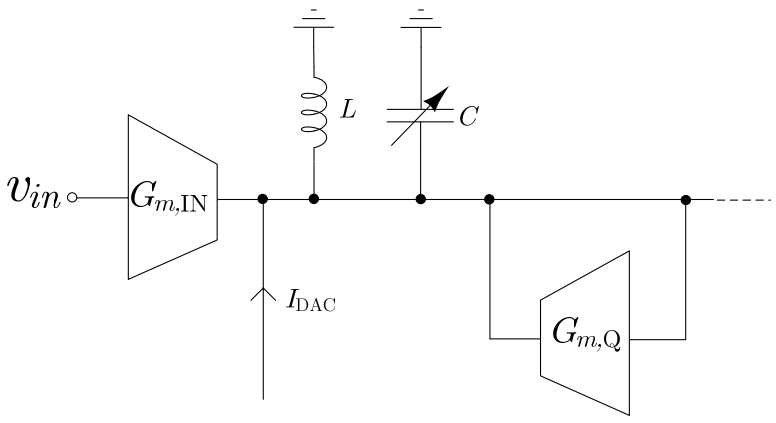


Figure 6-3 Input stage of the CT-ΔΣ modulator

$$P_{\text{FSR}}[\text{dBm}] = 10 \times \log_{10} \left(\frac{\left(\frac{V_{\text{PP}}}{2} \Big/ \sqrt{2} \right)^2}{R_{\text{IN}}} \right) + 30 \tag{6.1}$$

which gives –6.33dBm for L1-E1, –17.43dBm for L2, and –17.80dBm for L5-E5a.

A typical patch or helix antenna with a pre-amplifier has a gain of 20 to 30dB and a noise figure of –2.5dB [Bau02], [Tsu05]. The gain and the NF of the Q-enhanced LC filter employed after the antenna are measured using SPECTRE SP and Noise analysis and shown in Figure 6-4. Gain and NF of a LNA in 90nm RF CMOS process is typically 20 to 25dB and 2 to 2.5dB, respectively. With these considerations in mind, the RF front-end gain, as given in Table 6-2, is planned to leave a few dBs of headroom to accommodate for the interferers. The total gain provided by the RF front-end raises the thermal noise floor from –100.86 to around –13dBm. The cascaded noise figure of the antenna and the RF front-end can be calculated using Friis formula as [Fri45]:

$$\text{NF} = 10 \times \log_{10} \left(F_{\text{ANT}} + \frac{F_{\text{FILTER}} - 1}{G_{\text{ANT}}} + \frac{F_{\text{LNA1}} - 1}{G_{\text{ANT}} G_{\text{FILTER}}} + \frac{F_{\text{LNA2}} - 1}{G_{\text{ANT}} G_{\text{FILTER}} G_{\text{LNA1}}} \right) \tag{6.2}$$

where F is the non-log noise factor and G is the non-log gain of the components as given in Table 6-2.

Table 6-2 Gain plan of the RF front-end

	Antenna	RF Filter			LNA			ADC		
		L1	L2	L5	L1	L2	L5	L1	L2	L5
Gain [dB]	25	27.3	22.7	21.2	22					
NF [dB]	2.5	11.9	12.4	12.6	2.5					
Cascaded NF [dB]		~2.5								
Cascaded Gain [dBm]		25			52.3	47.7	46.2	74.3	69.7	68.2
Noise Power [dBm]	–100.86	–73.36			–34	–38	–39	–9.5	–13	–15

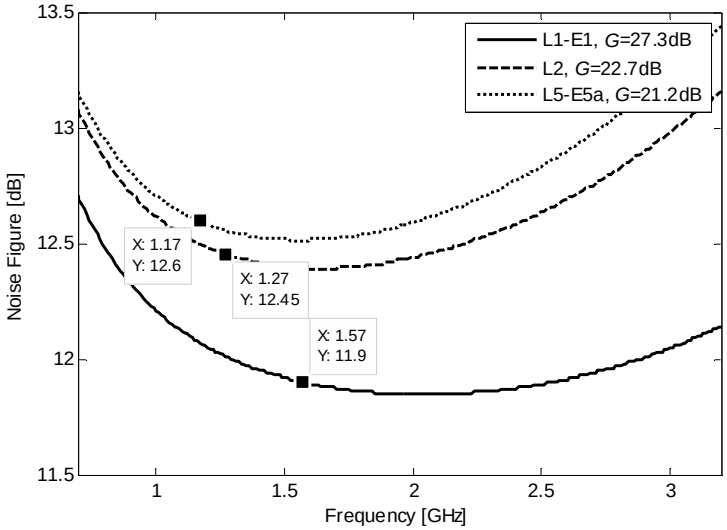


Figure 6-4 Noise figure of the Q-enhanced LC filter after the antenna

6.2 GNSS Toolbox

During this Ph.D. study, next-generation GNSS signals had been transmitted by a few satellites in orbit or they only existed on paper. In order to analyze and evaluate the performance of the proposed GNSS receiver architecture, a GNSS signal generator for GPS L1/L2/L5 and Galileo E1/E5/E6 bands as well as the signal processing blocks for the digital receiver is developed at behavioural level in MATLAB/SIMULINK. The toolbox can be divided into three blocksets: Signal transmission, wireless channel, and the DSP, as depicted in Figure 6-5 .

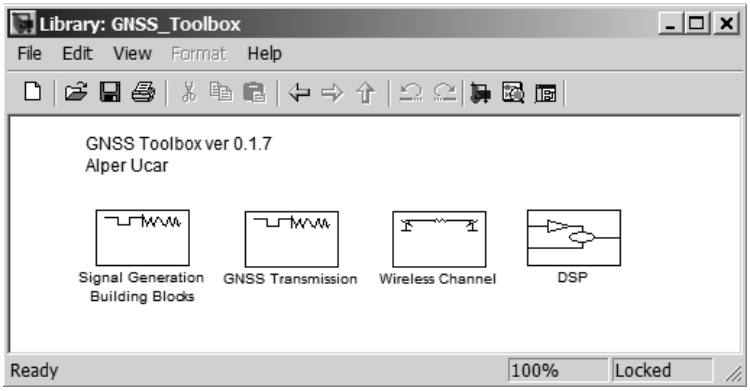


Figure 6-5 Snapshot of the GNSS Toolbox in SIMULINK

6.2.1 Signal Transmission

Signal transmission blockset, as illustrated in Figure 6-6, generates civilian GPS L1/L2C/L5 and Galileo E1/E5/E6 signals according to the latest signal specification [Nav06], [Esa10]. A set of building blocks for code generation and signal modulation are also available as shown in Figure 6-7, which enables the end-user to modify the code and modulation parameters. As an example, the parameters available for AltBOC modulation are shown in Figure 6-8.

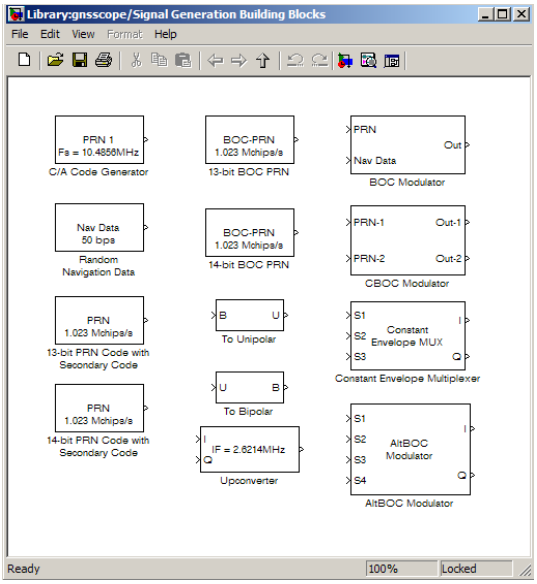


Figure 6-6 Building blocks for signal generation

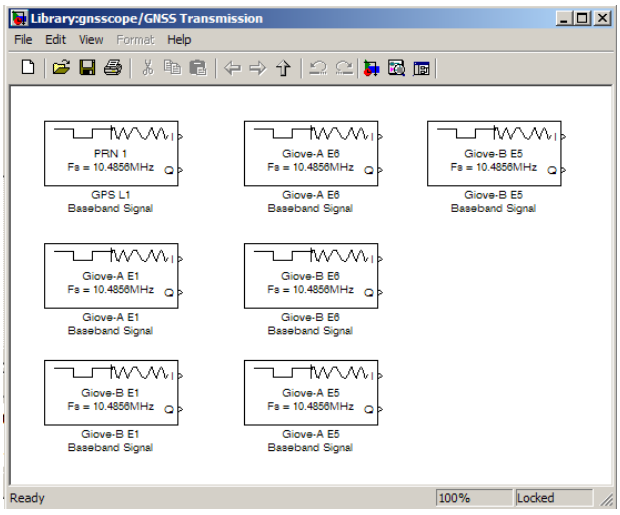


Figure 6-7 GNSS transmission

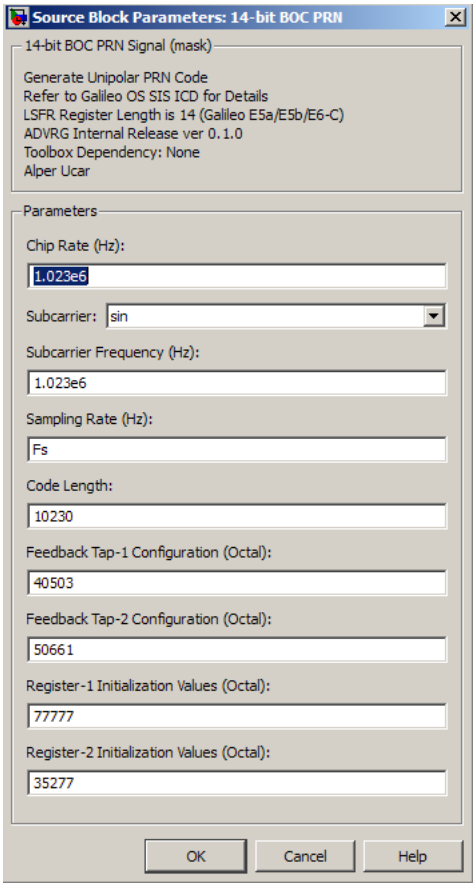


Figure 6-8 Design parameters available to end-user for "14-bit BOC-PRN generator"

6.2.2 Wireless Channel

The wireless channel is characterized as a fading channel, which caters for ionospheric delay, Doppler frequency shift on the carrier and multipath effects [Kaz08]. Doppler shift is applied to the signal in order to achieve the appropriate frequency offset. An RF model for the multipath Rician fading channel is developed since, in most of the cases, the radionavigation signals travel to the receiver along a Line-of-Sight (LoS) path.

6.2.3 DSP

The DSP block consists of programmable FIR down-sampler, serial and parallel code phase search acquisition, and signal tracking modules. All DSP modules are implemented in 4-bit fixed-point arithmetic. They are also parametrizable to give the user control over important variables such as the number of correlators, correlator spacing, code/carrier loop filter bandwidth,

and code/carrier discriminator functions. Figure 6-9 depicts the parallel code phase search acquisition module.

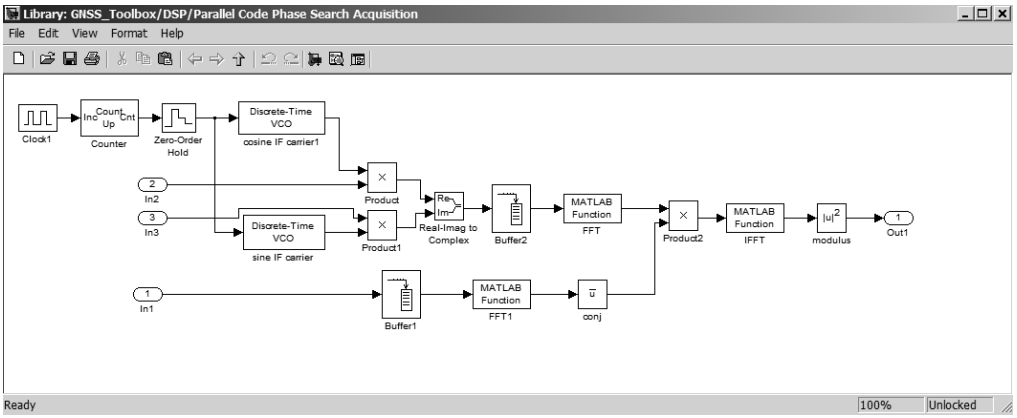


Figure 6-9 Parallel code phase search acquisition module

6.3 Simulation of the Receiver Chain

In order to analyze the performance of the proposed receiver, MATLAB/SIMULINK – CADENCE co-simulations are performed with the setup illustrated in Figure 6-10.

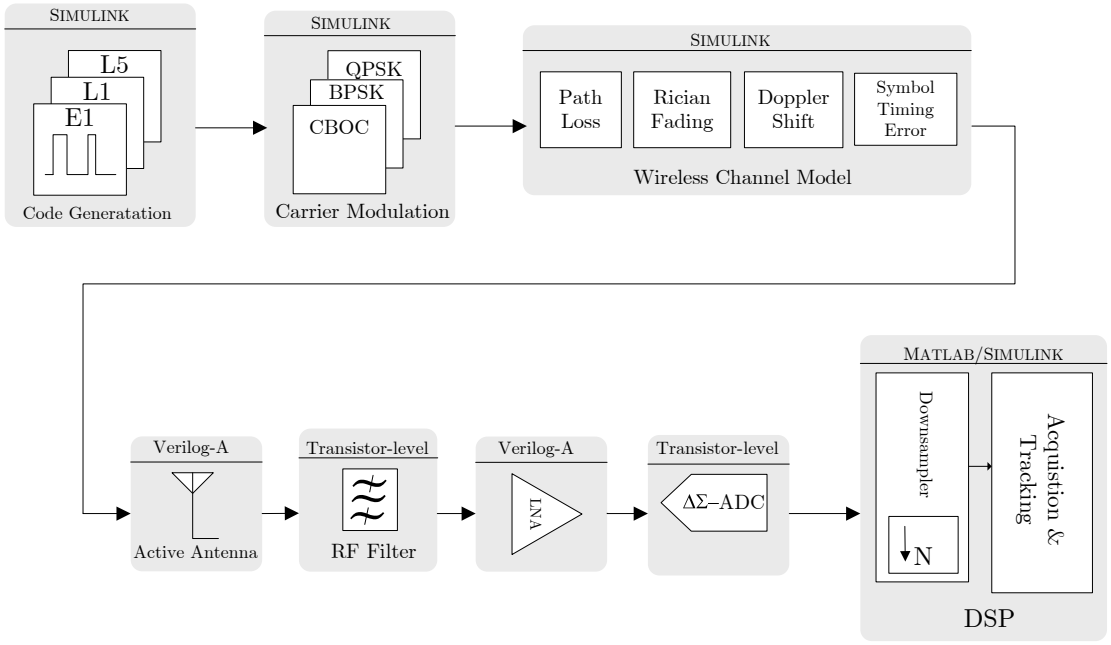


Figure 6-10 MATLAB/SIMULINK– CADENCE simulation setup for the receiver chain

GNSS signals are generated and passed through the wireless channel model in MATLAB/SIMULINK, as depicted in Figure 6-11. The raw data obtained from the behavioural simulation is imported into the CADENCE VIRTUOSO Analog Design Environment where a Verilog-A model for the amplifiers and transistor-level design for the Q-enhanced LC filter and the proposed CT-ΔΣ modulator are employed, as depicted in Figure 6-12. The proposed subsampling receiver architecture is set up in VIRTUOSO with the gain plan given in Table 6-2. The sampling rates for each band are chosen so that the SNR of the ADC does not vary much from one band to another. The sampling rates also satisfy Equation (5.1) in order to place the IF signal (f_{IF}) at $f_S/4$.

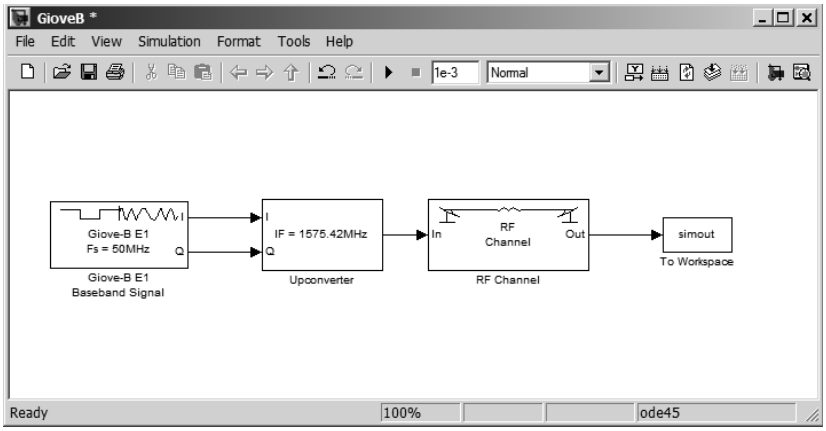


Figure 6-11 GIOVE-B raw data preparation in SIMULINK

It was previously demonstrated that the bandwidth of the L5/E5a signal can be reduced down to 9MHz with only 1.15dB power loss [Det08]. The bandwidth of the E1 OS signal can also be reduced to 4.092MHz at the cost of a less sharp correlation function for the E1 signal. The novel CT-ΔΣ modulator with the parameters given in Table 6-3 is employed for A/D conversion. The clock signal utilized for modulator's quantizer and DACs is set to have 0.5% RMS clock jitter. The data collected after transient simulations with are imported back to MATLAB workspace. The digitized signals are band-pass filtered over their relevant bandwidths (Δf) to filter out the noise and then down-sampled with a down-sampling factor as given in Table 6-3. Once filtered and down-sampled all civilian signals are successfully acquired and tracked. The C/N0 is estimated with the variance summation method using prompt in-phase and quadrature correlation values [Psi03] and is found to be ranging from 36 to 41dB-Hz, as given in Table 6-3.

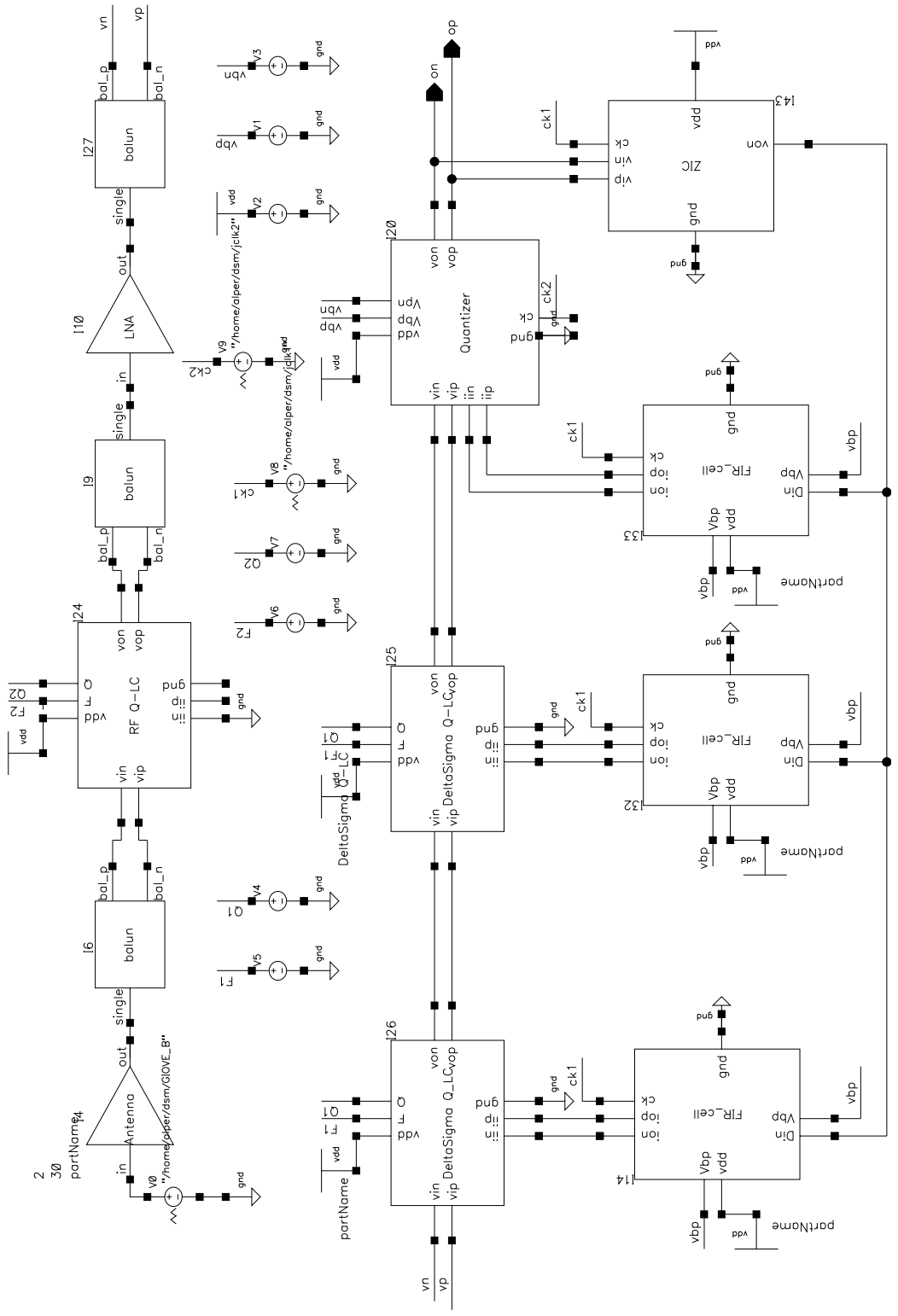


Figure 6-12 RF front-end testbench in Cadence Virtuoso

Table 6-3 Simulation Parameters of the Receiver Chain

Band	CT-ΔΣ ADC						DSP		
	f_S [Msps]	Δf [MHz]	M	Q_E	OSR	SNR[§] [dB]	f_{IF} [MHz]	D^{**}	C/N_0 [dBHz]
L1-E1	484.74	4.092	13	200	70	53	121.18	32	36[††]
L2	288.47	2.046	17	300	70	55	72.21	64	41
L5-E5a	672.25	9	7	100	52	46	168.06	32	39[‡‡]

The journey of the generated GIOVE-B signal through the RF front-end is plotted in Figure 6-13. Figure 6-13(d) clearly shows how the proposed ΔΣ modulator shapes the noise away from the desired signal to make the BOC-modulated signal's main lobes visible at the output of the ADC. This concept is also illustrated in Figure 6-14. Acquired Galileo E1-C signal, using the parallel code phase search acquisition module, is plotted in Figure 6-15. Figure 6-16 illustrates the prompt in-phase correlator output and navigation data sent from the signal generator. Consequently, it is demonstrated that the receiver architecture can acquire the civilian GPS and Galileo radionavigation signals with high C/N_0.

[§] For –3dBFS amplitude

[**] Down-sampling factor

[††] For Galileo E1-C

[‡‡] For GPS L5

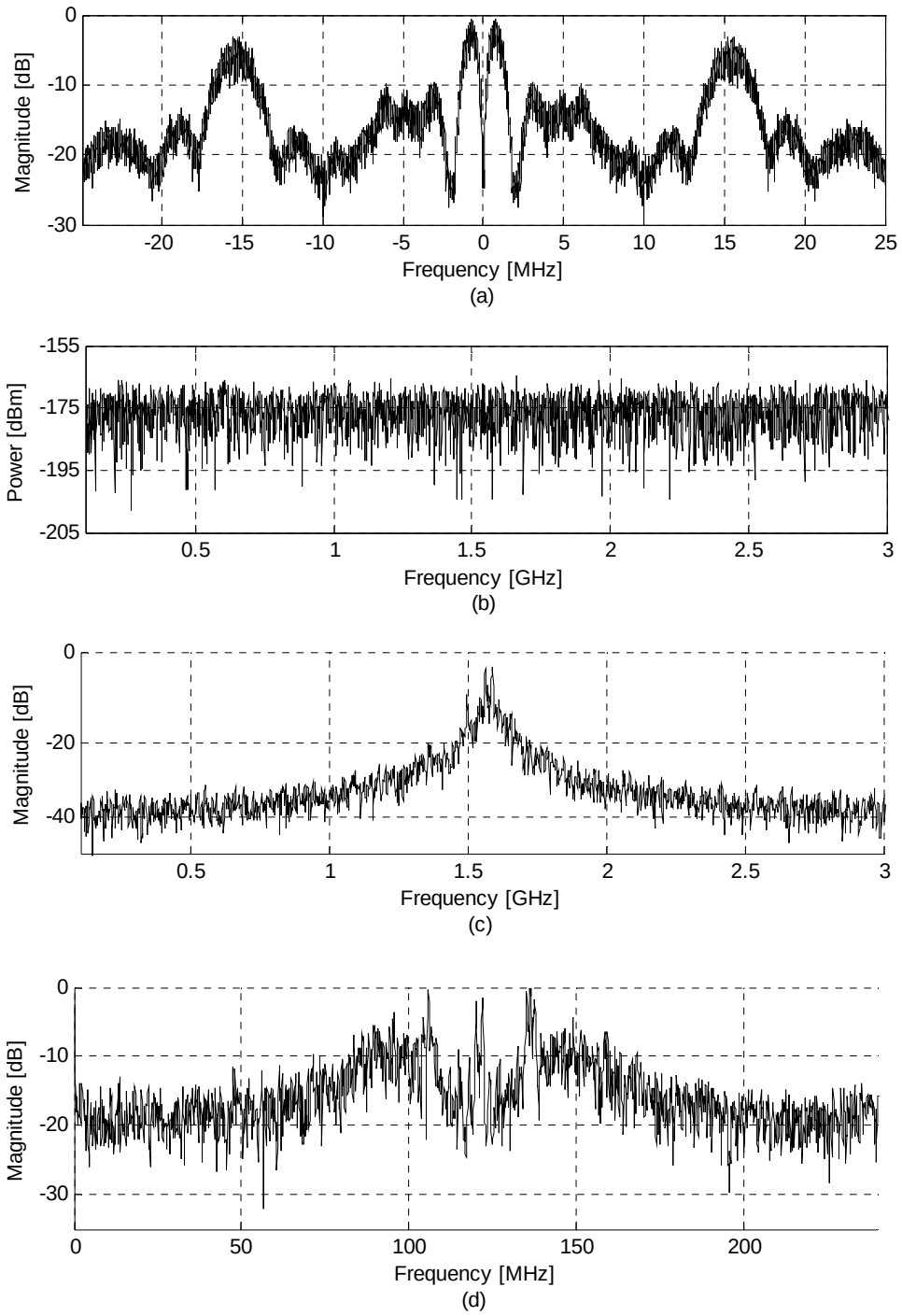


Figure 6-13 Generated GIOVE-B signal through the receiver chain (a) Baseband signal at the output of the signal generator (b) RF signal at the input of the antenna (c) RF signal at the output of the RF Filter (d) IF signal at the output of the CT-ΔΣ ADC

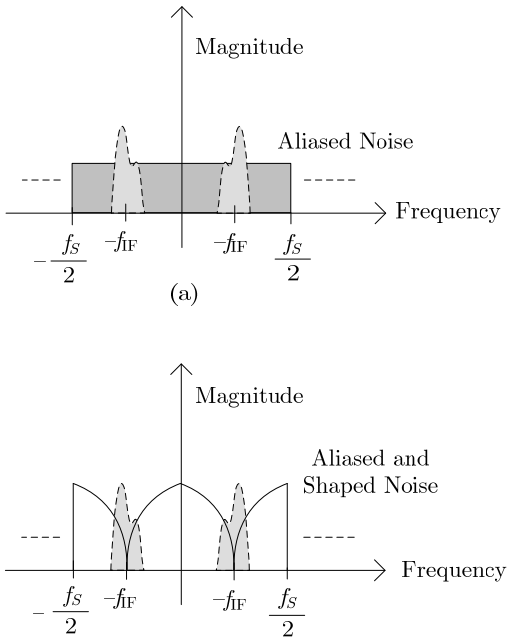


Figure 6-14 Aliased noise from a (a) Flash ADC (b) Proposed CT-ΔΣ ADC

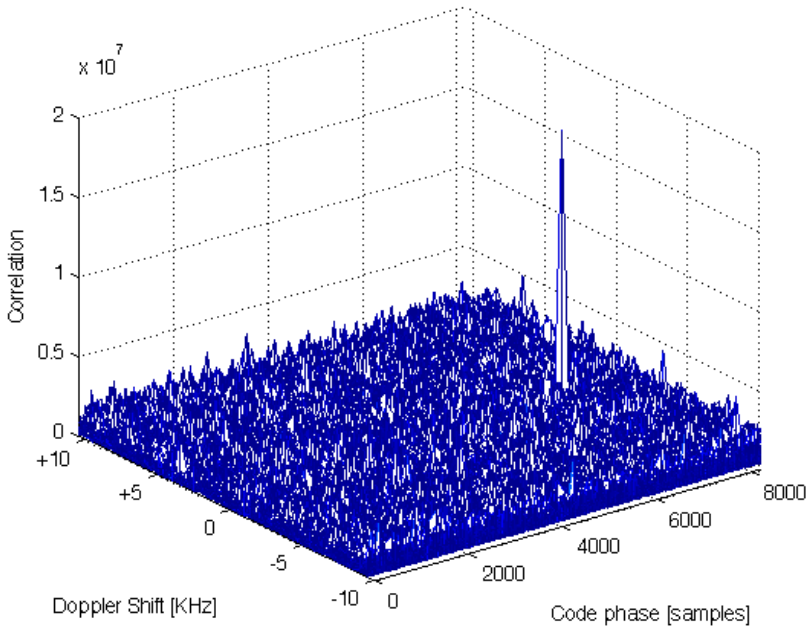


Figure 6-15 Acquired Galileo E1-C signal

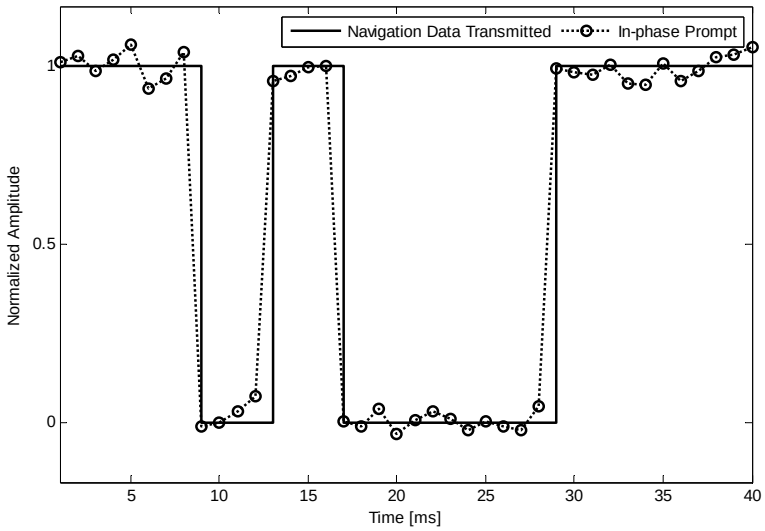


Figure 6-16 Decoded navigation data for Galileo E1-B signal

Chapter 7

Concluding Remarks

The main motivation of this doctoral work was to investigate the optimal receiver architecture for multi-constellation GNSS applications. The work reported in the thesis deploys a novel subsampling $\Delta\Sigma$ noise-shaping technique, which subsequently enables to propose a novel receiver architecture in an effort to reduce the number of analog components and to eliminate undesirable off-chip devices such as the expensive SAW filters. The main accomplishments of the thesis on a chapter-by-chapter basis can be summarized as follows.

Chapter 1 is dedicated to setting the scene for the problem in hand and looking at the state-of-art together with the novel contributions to the state-of-art by the author.

In Chapter 2, signal characteristics of GPS and Galileo are presented to give the reader an idea about how a multi-constellation receiver would deliver enhanced positioning accuracy to the end-user.

In Chapter 3, various receiver topologies are reviewed and compared. It is shown that while the subsampling receiver is an attractive candidate for multi-frequency applications, noise aliasing as a result of subsampling degrades the SNR of the sampled signal spectrum. It is concluded that a subsampling receiver employing A/D conversion with CT-ΔΣ modulators may be a feasible option for a multi-constellation receiver as it offers noise-shaping and inherent AA filtering.

Chapter 4 gives an introduction to ΔΣ modulators with an emphasis on design and implementation of high-speed CT modulators. Q-enhancement circuits and the Q and frequency tuning algorithms are introduced which make it feasible to implement multi-band resonators in BiCMOS and CMOS process technologies.

In Chapter 5, issues associate with subsampling CT-ΔΣ modulator are outlined and a novel CT-ΔΣ modulator, which is capable of compensating for the attenuation of the RF alias in the feedback path is proposed. It is also shown that the novel modulator enables the utilization of NRZ feedback pulse when the loop filter is implemented with LC resonators, which is not possible with a conventional CT-ΔΣ modulator. The utilization of NRZ feedback offers enhanced SNR compared to NRZ/RZ and RZ/HRZ feedback pulse combinations. Additional clock jitter suppression at the output of the feedback path is accomplished thanks to the novel feedback path. A low-complexity filter tuning circuit for modulator's loop filter is also proposed in this Chapter.

In Chapter 6, a multi-constellation GNSS receiver architecture is proposed in which the novel subsampling CT-ΔΣ modulator is the core component to deliver a high performance. The proposed receiver architecture can handle multi-constellation GPS/Galileo signal acquisition with minimal number of analog components thereby eliminating and circumventing the cost and impairments associated with them. Exploiting the noise-shaping characteristics of the CT-ΣΔ modulator makes subsampling a viable option for

GNSS applications. Time-domain behavioural and transistor-level simulations indicate that the proposed receiver is capable of tracking the civilian GPS/Galileo signals with high C/N_0. Elements of a highly parametrizable toolbox for the behavioural simulation of GNSS transmission and reception was developed to evaluate the performance of the novel receiver architecture. Considering that the GNSS signal specification is continuously updated, the toolbox might serve as a handy platform to develop and test new concepts and designs for GNSS applications.

In final conclusion, it is anticipated that the work presented in this thesis will enable to monolithically integrate low-power, next generation GNSS receivers on a single chip, to tune into the radionavigation band of interest as and when desired, and to adapt to the dynamic communication environment to achieve a high positioning accuracy.

7.1 Future Work

System and circuit-level design for a novel subsampling CT-ΔΣ modulator was presented in this study. Time-domain, behavioural and transistor-level simulations were performed using MATLAB/SIMULINK and CADENCE VIRTUOSO to evaluate the performance of the proposed modulator and the subsampling receiver. Although key non-idealities were considered for the behavioural-level models, they should be replaced with more realistic low-level models in future simulations. The raw data obtained from the signal generator should also be replaced with the ones obtained from satellites. Moreover, post-layout simulations need to be performed on the proposed ΔΣ modulator and the receiver to obtain more accurate performance metrics. If post-layout simulation results are satisfactory, an implementation in 90nm or down RF CMOS technology may be considered.

The proposed CT-ΔΣ modulator can be utilized to enable integrating wireless standards such as GSM, UMTS, IEEE 802.11, and GNSS onto a single universal radio platform. Fast and efficient Q and frequency tuning of the loop filter is the key challenge for such integration. Another future

research direction is to improve the accuracy of the proposed tuning circuit whilst keeping the complexity and the power consumption low.

Finally, the GNSS toolbox developed for GPS and Galileo can be extended to incorporate modules for GLONASS and Compass signal generation, optimized BOC-modulated signal acquisition and tracking, and position calculation.

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