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# Achieving Rail-to-Rail Input Operation Using Level-Shift Multiplexing Technique for All CMOS Op-Amps

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**Abstract**— This paper presents a new design approach which can convert any CMOS operational amplifiers to have rail-to-rail common-mode input capability by utilizing few additional hardware elements. The proposed circuit can operate over a wide range of supply voltages from 1-volt to the maximum allowed for the CMOS process, without degrading the ac and dc performances of the amplifier in question over the rail-to-rail operation.

## I. INTRODUCTION

The demand for portable electronics which can operate at very low supply voltages has been known as an established fact for the last few decades, as it helps improve the operation lifetime as well as minimizing the density of the battery. In analog amplifier applications, rail-to-rail operations are increasingly becoming popular in obtaining maximum dynamic range at limited supply voltages.

An operational amplifier (op-amp) in non-inverting unity-gain configuration requires a rail-to-rail input stage to fully accomplish the rail-to-rail output stage. When designing a rail-to-rail input stage, one must ensure to keep the transconductance ( $g_m$ ) constant over the rail-to-rail Common-Mode (CM) voltage and hence to minimize signal distortion [2]-[4]. The traditional technique using complementary differential pairs with 1:3 current mirrors [1] is commonly introduced by in the literature [2]-[4]. Recently, the trend of novel techniques have proposed other performances to be also independent of the input CM voltage, such as large-signal behavior, Common-Mode Rejection Ratio (CMRR) and so on [5]-[6].

When using complementary input pairs, on the other hand, designers must deal with the mobility ratio of the pairs ( $\mu_n/\mu_p$ ), which is process- and temperature-dependent and may deviate by approximately 12% [7]. To avoid investigating this in the first place, there are some available techniques that only use a single type of differential pair, such as level-shifting [7], floating-gate [8], and bulk-driven [9]. Each of these techniques, however, possesses several drawbacks. The level-shifting technique proposed in [7] utilizes two identical differential pairs, each biased with the same amount of the tail current, and the input of one of the

differential pairs is level-shifted using source followers. The FeedForward (FF) cancelling section is used to ensure only one differential pair contributes to the effective  $g_m$  over the rail-to-rail CM input. However, the cutting-off of the other tail current of the differential pair introduces degradation in the input-referred noise, due to the minimized  $g_m$  of the cut-off differential pair. The differential pair using floating-gate MOSFETs, which can be implemented with a standard double poly-silicon process, couples only the ac part of the input whilst the dc is biased at the required level so that the rail-to-rail operation can be achieved, however the output resistance is significantly reduced [10] which causes degradation in the open-loop ac gain of the op-amp. For the bulk-driven technique, there are some recent papers proposing to overcome many of the concerns. To overcome the reduced transconductance of a bulk-driven MOSFET, Carrillo *et al* proposed the partial positive feedback technique in [11], and we proposed the technique of forward-biasing of the bulk for the cascode transistors in [12] to improve the output resistance of the folded-cascode op-amp. Furthermore, we also proposed a technique to diminish the latch-up likelihood in [13] to achieve robust operation over the wide range of supply voltages from sub 1-volt to the maximum allowed of the CMOS process. The remaining concern with a bulk-driven MOSFET is the input capacitance which is caused by the capacitance of the substrate.

The proposed design techniques mentioned above, however, may not always be suitable in some applications. There are many different circuit topologies of op-amps, and designers choose a suitable topology depending on the performance improvement they care for in their particular application. Replacing a proposed rail-to-rail input stage to their chosen op-amp topology may sometimes lead to difficulties and consume a lot of time in the implementation. Rather, an ideal solution for achieving rail-to-rail input operation should be one that incurs a small circuit overhead for any chosen op-amp topology, whilst maintaining all the ac and the dc performances of the op-amp to the same level over the rail-to-rail operation.

In summary, this paper presents a new design approach for achieving rail-to-rail input operation which can be

applied to any CMOS op-amp structures at the expense of a small hardware overhead. The proposed circuit can operate over a wide range of supply voltages from 1-volt to the maximum allowed for the CMOS process, whilst maintaining the ac and dc performance of the chosen amplifier the same over the rail-to-rail operation.

## II. THE LEVEL-SHIFT MULTIPLEXING TECHNIQUE

### A. Topology

An n-bit analog multiplexer as depicted in Figure 1 is a well-known block [14].

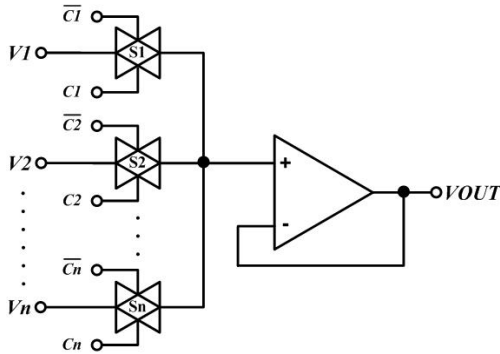


Figure 1. An n-bit analog multiplexer using CMOS transmission gates

It is worth noting that analog multiplexers with CMOS transmission gates are still commonly used today in the field of biochemical sensors, image processing, face recognition, military and satellite electronics [15]-[16]. Indeed, our proposal utilizes 2-bit multiplexer for each inputs of the op-amp. Figure 2 illustrates the topology of our proposal, which we call the Level-Shift Multiplexing (LSM) technique.

The LSM block illustrated in Figure 2(a), is for use with CMOS op-amps having nMOS input pairs, whereas Figure 2(b) is for the op-amps having pMOS input pairs. As can be seen from Figure 2, the LSM block consists of source followers, 2-bit multiplexers and a comparator. The operation principle of this block is very simple. The source followers are used to shift the DC-level of the input voltage, the multiplexers are used to propagate either the shifted or non-shifted DC-level of the input voltage, and the comparator is used to sense the input CM voltage and select between the two accordingly. In the next section, we describe a very simple comparator which we propose for use with this LSM block.

### B. Comparator

For the LSM block we propose to deploy a comparator that has input hysteresis (also known as Schmitt trigger) to give the input stage noise immunity [2]-[4]. Figure 3 illustrates a very simple Schmitt trigger proposed by Pedroni [17], which has turned out to be an essential part of our solution in our proposal.

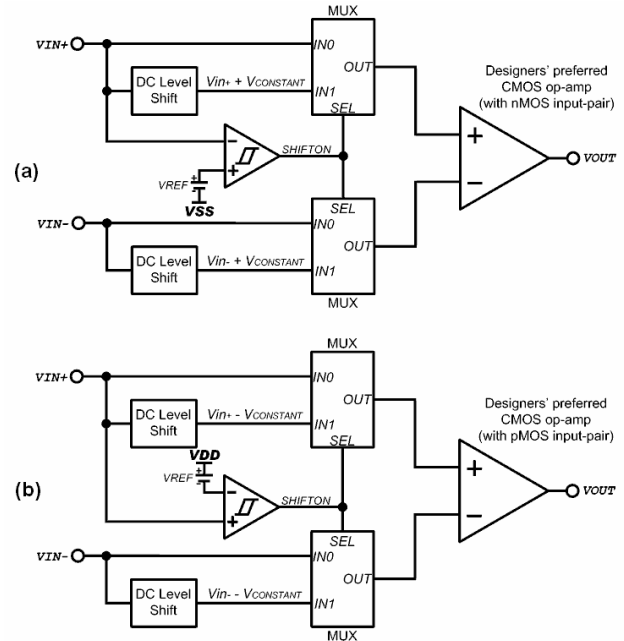


Figure 2. Topology of the LSM input stage for CMOS op-amp with (a) nMOS input pair and (b) pMOS input pair

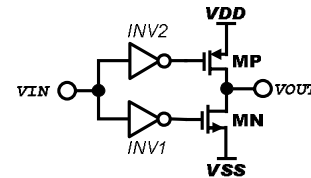


Figure 3. Schmitt trigger proposed by Pedroni [10]

The beauty of this Schmitt trigger circuit is that no bias circuitry is needed for the reference voltage  $V_{REF}$ , as it is determined by the transition stage of the two inverters  $INV1$  and  $INV2$ . To make the transition stage independent of the supply-voltage, we have modified the Schmitt trigger circuit of Figure 3 as detailed in Figure 4 for use with our LSM block.

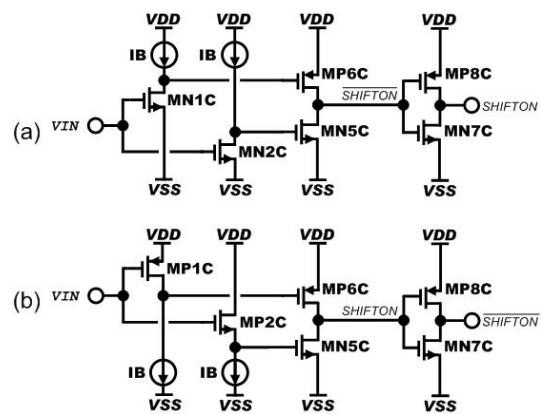


Figure 4. Proposed Schmitt trigger for CMOS op-amp with (a) nMOS input pair and (b) pMOS input pair

Figure 5 shows the simulation results for the circuit of Figure 4(a), which is designed to activate the level-shift when  $V_{IN} < 0.5V$  and release it when  $V_{IN} > 0.55V$ , hence allowing an input hysteresis of 50mV.

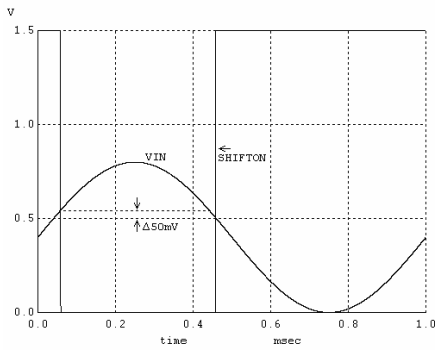


Figure 5. Simulation results of Figure 4(a)

To verify the design of the comparator, we recommend checking it with the CMOS transmission gate switch to ensure no charge injection occurs by the transition of the comparator. As recommended in [18], slow transition of the gate input of the switch results in diminished charge injection. In our proposed LMS block, this can be accomplished by reducing the slew-rate of the comparator, increasing the gate capacitance of the transmission switch, or having a capacitive load at the output of the comparator. An example of the charge injection is given in Figure 6.

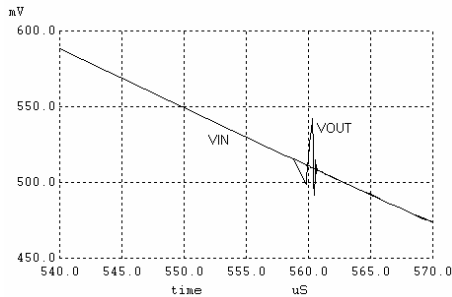


Figure 6. An example of the charge injection caused by the transition of the comparator output

### III. VERIFICATION

To verify the performance of the LSM block, we transformed it into the transistor-level circuit as shown in Figure 9, and chose to apply it with the conventional two-stage op-amp as illustrated in Figure 7.

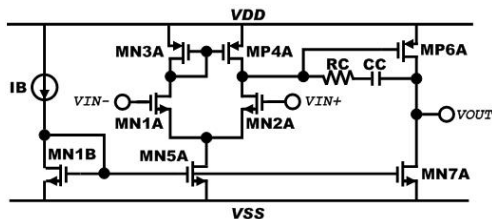


Figure 7. A two-stage op-amp

Using the BSIM3 MOSFET models for a 0.18μm CMOS process, we simulated our proposal with a supply voltage of 1.5-volts and a load resistance and capacitance of 1MΩ and 5pF, respectively. Figure 8 gives the simulation results in the form of a Bode plot for the input CM voltage  $V_{ICM}$  varying from 0.1V to 1.3V with a 0.2V step.

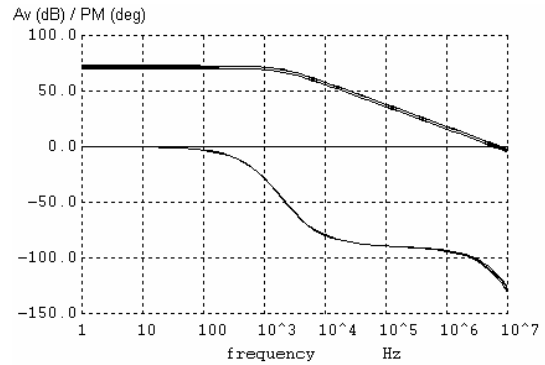


Figure 8. Simulated frequency response of the LSM input stage for  $V_{ICM}$  varying from 0.1V to 1.3V with a 0.2V step

Table I shows the summary of the simulation results of the overall performance of the op-amp.

TABLE I. SIMULATION RESULTS OF THE OVERALL PERFORMANCE OF THE OP-AMP

| Characteristics  | Simulated Results  |
|--|--|
| Open-loop DC gain  | 70.6dB ( $V_{ICM} < 0.5V$ , i.e. when propagated through source followers.)<br>72.6dB ( $V_{ICM} > 0.5V$ ) |
| Unity-gain frequency   | 6.0MHz ( $V_{ICM} < 0.5V$ , i.e. when propagated through source followers.)<br>7.5MHz ( $V_{ICM} > 0.5V$ ) |
| Phase margin   | 64°  |
| ICMR   | 1.3V   |
| Total current consumption  | 64~109μA   |
| SR   | SR+ = SR- = 2.0V/μs  |
| Output voltage swing   | 1.3V   |
| Common-mode rejection ratio  | 79~85dB  |
| Power Supply Rejection Ratio   | PSRR+ = 75~78dB<br>PSRR- = 82~103dB  |
| Input referred noise voltage   | 15.9~24.5nV/√Hz (white noise only)   |
| Total harmonic distortion, $A_{VCL} = +1V/V$                                       | 0.006% for 1.3Vp-p, 1kHz sine wave   |
| Measurement condition: $V_{DD} = 1.5V$ , $V_{SS} = 0V$ , $C_L = 5pF$ , $R_L = 1MΩ$ |  |

### IV. OBSERVATIONS

The simulation results indicate that the open-loop DC gain drops by 2dB when the signals are propagated through the source followers. The cause of this 2dB drop is the gain of the source followers, as it is always less than one due to the body-effect. To avoid this, the circuit designers may wish to short the bulk-terminals of the input transistors to the source terminals, which are technically feasible if an n-well process is used. However, the practical challenge of this approach is that the layout matching of the input transistors, using the conventional common-centroid configuration cannot be utilized when the bodies need to be isolated. Hence, the offset may become an issue.

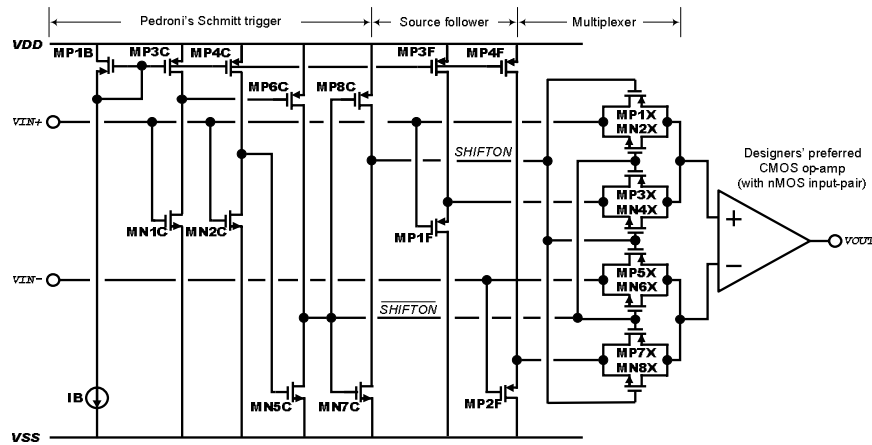


Figure 9. Transistor realization of the LSM technique for CMOS op-amp with nMOS input-pair

As can be seen in Table I, the important practical advantage of the LVS input stage is that almost all of the op-amp performance parameters are independent of the  $V_{ICM}$ . However, the drawback is that the noise immunity of the ground significantly relies on the  $V_{ICM}$  level. The simulation results indicate that the PSRR- differs by 21dB depending on the  $V_{ICM}$ . This degradation is observed when the signals are propagated through the source followers, and currently ongoing work is in the area of new DC level-shifters to solve this problem.

## V. CONCLUSION

A new design approach for achieving rail-to-rail input operation called the LVS technique has been presented. This technique utilizes only digital multiplexers, source followers and a simple Schmitt trigger, and transforms any CMOS op-amp to one having rail-to-rail input capability. SPICE simulation results presented in this paper confirm that almost all of the op-amp's performance measures are independent of the  $V_{ICM}$ . The LVS technique has been shown to be a serious contender for CMOS op-amps in unity-gain buffer applications.

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