**Design and implementation of generalized topologies of time-interleaved variable bandpass Σ−Δ modulators**

**Kalafat Kizilkaya, I.**

# DESIGN AND IMPLEMENTATION OF GENERALIZED TOPOLOGIES OF TIME-INTERLEAVED VARIABLE BANDPASS Σ−Δ MODULATORS

A Thesis/A Dissertation

By

Işıl KALAFAT KIZILKAYA

Department of Engineering

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## ABSTRACT

In this thesis, novel analog-to-digital and digital-to-analog generalized time-interleaved variable bandpass sigma-delta modulators are designed, analysed, evaluated and implemented that are suitable for high performance data conversion for a broad-spectrum of applications. These generalized time-interleaved variable bandpass sigma-delta modulators can perform noise-shaping for any centre frequency from DC to Nyquist. The proposed topologies are well-suited for Butterworth, Chebyshev, inverse-Chebyshev and elliptical filters, where designers have the flexibility of specifying the centre frequency, bandwidth as well as the passband and stopband attenuation parameters. The application of the time-interleaving approach, in combination with these bandpass loop-filters, not only overcomes the limitations that are associated with conventional and mid-band resonator-based bandpass sigma-delta modulators, but also offers an elegant means to increase the conversion bandwidth, thereby relaxing the need to use faster or higher-order sigma-delta modulators.

A step-by-step design technique has been developed for the design of time-interleaved variable bandpass sigma-delta modulators. Using this technique, an assortment of lower- and higher-order single- and multi-path generalized A/D variable bandpass sigma-delta modulators were designed, evaluated and compared in terms of their signal-to-noise ratios, hardware complexity, stability, tonality and sensitivity for ideal and non-ideal topologies. Extensive behavioural-level simulations verified that one of the proposed topologies not only used fewer coefficients but also exhibited greater robustness to non-idealties.

Furthermore, second-, fourth- and sixth-order single- and multi-path digital variable bandpass digital sigma-delta modulators are designed using this technique. The mathematical modelling and evaluation of tones caused by the finite wordlengths of these digital multi-path sigma-delta modulators, when excited by sinusoidal input signals, are also derived from first-principles and verified using simulation and experimental results. The fourth-order digital variable-band sigma-delta modulator topologies are implemented in VHDL and synthesized on Xilinx® Spartan™-3 Development Kit using fixed-point arithmetic. Circuit outputs were taken via RS232 connection provided on the FPGA board and evaluated using MATLAB routines developed by the author. These routines included the decimation process as well. The experiments undertaken by the author further validated the design methodology presented in the work.

In addition, a novel tunable and reconfigurable second-order variable bandpass sigma-delta modulator has been designed and evaluated at the behavioural-level. This topology offers a flexible set of choices for designers and can operate either in single- or dual-mode enabling multi-band implementations on a single digital variable bandpass sigma-delta modulator.

This work is also supported by a novel user-friendly design and evaluation tool that has been developed in MATLAB/Simulink that can speed-up the design, evaluation and comparison of analog and digital single-stage and time-interleaved variable bandpass sigma-delta modulators. This tool enables the user to specify the conversion type, topology, loop-filter type, path number and oversampling ratio.

## ACKNOWLEDGMENTS

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Finally, I want to dedicate this thesis to my parents. To my impatience father and mother, Kahraman and Leyla, who everyday asked about the progress of my thesis. To my father- and mother-in-law, Turgut and Nurcan, who always showed respect to my dream of being a doctor and never complained that I took away their precious son and grandchild away from home to pursue this aim.

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## ABBREVIATIONS

The following project-specific and general technical abbreviations are used in the thesis:

**AAF** Anti Aliasing Filter

**ADC** Analog to Digital Converter

**AWGN** Additive White Gaussian Noise

**A/D** Analog to Digital

**BS** Band Stop

**BP** Bandpass

**BPF** Bandpass Filter

**BW** Bandwidth

**CCD** Charged Coupled Device

**CF** Centre Frequency

**CT** Continuous Time

**DAC** Digital to Analog Converter

**DECT** Digital Enhanced Cordless Telecommunications

**DEM** Dynamic Element Matching

**D/A** Digital to Analog

**ENOB** Effective Number of Bits

**EPS** Encapsulated Postscript

**FFT** Fast Fourier Transform

**GNSS** Global Navigation Satellite System

**GSM** Global System for Mobile Communication

**GUI** Graphical User Interface

**FSM** Finite State Machine

**HF** High Frequency

**IC** Integrated Circuit

**IF** Intermediate Frequency

**IIR** Infinite Impulse Response

**IMD** Intermodulation Distortion

**LFSR** Linear Feedback Shift Register

**LNA** Low Noise Amplifier

**LP** Lowpass

**LPF** Lowpass Filter

**NTF** Noise Transfer Function

**OSR** Oversampling Ratio

**PBA** Passband Attenuation

**PCM** Pulse Code Modulation

**PSD** Power Spectral Density

**RF** Radio Frequency

**SBA** Stopband Attenuation

**SC** Switched Capacitor

**SDR** Software Defined Radio

**SINAD** Signal-to-Noise and Distortion Ratio

**SNR** Signal to Noise Ratio

**SP** Single Path

**STF** Signal Transfer Function

**TI** Time Interleaved

**VBP** Variable Bandpass

**2P** Two Path

**4P** Four Path

**Σ-Δ** Sigma-Delta

I, Işıl Kalafat Kızılkaya, declare that all the material contained in this thesis is my own work.

# Chapter 1. Introduction

Pervasive technology emerges in people's daily life requiring multi-mode multi-channel circuitry. Therefore, data converters need to be highly integrated into the overall system due to low-power, small-size requirements [1-3]. Moreover, innovative technologies such as Global Navigation Satellite System (GNSS), Software Defined Radio (SDR), Global System for Mobile Communication (GSM), Digital Enhanced Cordless Telecommunications (DECT) require wideband, high-speed data conversion [4-6].

Sigma-Delta (Σ-Δ) modulators offer more benefits compared to Nyquist-rate converters such as high-speed data conversion whilst providing decreased hardware. They are able high resolution even with a one-bit quantizer, since they employ oversampling and noise-shaping. Although using fewer bits in the quantizer inevitably causes higher quantization noise, it also removes the Dynamic Element Matching (DEM) circuitry and the noise arising from it [7, 8].

The basic idea of Σ-Δ modulation is to shape the quantization noise using a loop-filter such that the noise in the band of interest is suppressed, whilst the out-of-band noise is amplified. In addition, Σ-Δ modulators utilize high OverSampling Ratios (OSR)s to decrease the overall noise from DC to Nyquist [7, 8]. However, these benefits of Σ-Δ modulation have their own limitations.

First of all, the loop-filter may cause instability [9]. The type and order of the loop-filter should be chosen carefully after iterative simulations [7]. Secondly, using a high OSR restricts the bandwidth of the conversion therefore limiting the Σ-Δ modulators mostly to narrow-band applications [10]. In Chapter 2, these problems will be defined and discussed with their positive and negative aspects.

## 1.1 Integration, Loop-filter and Stability

As mentioned, a high OSR limits the conversion bandwidth of the Σ-Δ modulators thus there has been a great amount of work and analysis on LowPass (LP) Σ-Δ modulators. On the one hand, the designed, implemented and mathematically analysed LP Σ-Δ modulators makes it easy to build stable, high-resolution LP Σ-Δ modulators. However, the integration of LP Σ-Δ modulators with high-frequency technologies requires complex building blocks such as mixers

and passive filters [11-13]. These extra blocks not only make the structure complex and increase the overall power dissipation but also introduce extra noise and limit linearity of these modulators.

Herein, BandPass (BP) Σ-Δ modulators that are capable of feedforwarding the signal through the data converter are really advantageous as they eliminate the downsampling process [12, 13]. However, the majority of the published papers on BP Σ-Δ modulators are confined to midband ($f_s/4$) [13-15]. In addition, resonator based Σ-Δ modulators result in unequal out-of-band gain levels of the Noise Transfer Function (NTF) especially for frequencies close to DC and Nyquist. Unequal shoulder gains may cause modulator instability and/or ear-detectable noise. Moreover, if channel selection is required within the system, tunable centre-frequency and/or bandwidth are needed [15].

As a result, Variable BandPass (VBP) Σ-Δ modulators are highly suitable candidates to employ for high-speed and high frequency data conversion applications. It should be pointed out that VBP terminology is used here when referring to the variable centre-frequency and variable bandwidth of the Σ-Δ modulator. There are a few published papers on multi-band Σ-Δ modulators but they are restricted to other fixed centre-frequencies [16-18]. As a solution, this study presents generalized VBP Σ-Δ modulators that can accomplish noise-shaping for any centre frequency and bandwidth from DC to Nyquist. Moreover with the help of various filters such as Butterworth, Chebyshev, Inverse Chebyshev and Elliptical, designers have the flexibility to specify the centre frequency, bandwidth and passband/stopband attenuations. With the help of these filters, stable VBP Σ-Δ modulators are designed, evaluated and implemented. As compared to LP and midband Σ-Δ modulators, the designed generalized VBP Σ-Δ modulators employ more feedback and feedforward coefficients. Furthermore, the complexity of these coefficients requires more hardware when implemented in Digital to Analog (D/A) converters. However, these VBP Σ-Δ modulators have superior ability to shape the quantization noise in the frequency of interest within the desired bandwidth.

### 1.2 High OSR, Speed and Bandwidth

The high sampling frequency places huge pressure on processor speed, thus constraining discrete-time Σ-Δ modulators to narrow-band signal applications. In order to overcome the

high-speed requirements, researchers have focused on several parallel structures such as frequency-band-decomposition, cascaded Hadamard, and Time-Interleaving (TI) based Σ-Δ modulator topologies [19]. The TI approach employs $P$ mutually cross-coupled Σ-Δ modulators, each operating at a sampling frequency $f_s$, which results in an equivalent sampling rate of $Pf_s$. Moreover, this approach offers an elegant means to increase the conversion bandwidth circumventing the need to use faster or higher-order Σ-Δ modulators [20]. Using the TI technique requires increased hardware and design complexity, but provides a powerful means to increase the conversion band. In this study, the TI method is utilized and applied to the designed Single Path (SP) VBP Σ-Δ modulators. The designed TI VBP Σ-Δ modulators will be discussed in Chapter 3 and Chapter 4.

To sum up, generalized VBP Σ-Δ modulators are designed and evaluated in this study to provide flexibility. By providing flexibility, these generalized VBP Σ-Δ modulators eliminate the mixer and passive filtering blocks of conventional receivers. Hence they overcome the integration requirements of data converters within the high frequency and high-speed technology as will be explained in Chapter 3. Moreover, these generalized VBP Σ-Δ modulator topologies help to determine those frequencies that are capable of obtaining high SNRs and/or less hardware and/or less tonality. The stability and performance of these VBP Σ-Δ modulators are enhanced with the help of different filters; Butterworth, Chebyshev, Inverse Chebyshev and Elliptical filters. However, these generalized VBP Σ-Δ modulators still suffer from relatively narrow bandwidths as a result of the high OSRs. Therefore, the TI methodology is applied to the designed VBP Σ-Δ modulators. Whilst applying the TI technique, the positive and negative attributes of these resulting multi-path Σ-Δ modulators will be investigated and presented.

## 1.3 Outline

In *Chapter 2,* the basics of data conversion are explained. The commonly used blocks are explained and their mathematical models are provided. Thereafter, the theory of Σ-Δ modulators as well as their characteristics are presented. Hence the motivations for the design of TI VBP Σ-Δ modulators are explained. Finally the contributions and novelties of the thesis are listed.

In *Chapter 3,* a step-by-step design technique is developed for TI VBP Σ-Δ modulators. This technique is an extension of the node-equation method that is also explained in Chapter 3.

A generalized NTF that can perform Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters, is chosen to build generalized Analog-to-Digital (A/D) VBP Σ-Δ modulators. Two discrete loop-filters of $2^{nd}$-, $4^{th}$-, $6^{th}$- and $8^{th}$-orders are designed by mapping the given generalized NTF. Thereafter the developed design technique is applied to these SP VBP Σ-Δ modulators in order to construct their 2-path and 4-path counterparts. The resulting topologies are analysed and compared in terms of their coefficients, Signal-to-Noise Ratio (SNR), Dynamic Range (DR) and immunity to non-idealities.

In *Chapter 4,* D/A TI VBP Σ-Δ modulators are designed using the design technique in Chapter 3. The Error Feedback (EF) and the Output Feedback (OF) topologies are built employing the same loop-filter of $2^{nd}$-, $4^{th}$- and $6^{th}$-orders. Once again, the EF and OF topologies are analysed and compared in terms of their coefficients, SNRs, DRs and immunity to non-idealities. Thereafter, they are implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit. These circuits not only validate the developed design technique but also ensure the accuracy of the simulation routines built spesifically for these modulators.

In *Chapter 5,* the developed Graphical User Interface (GUI) is presented. This GUI wraps up all the designed A/D and D/A simulink models and Matlab routines in a single environement. It enables the user to plot the output response or the SNR response of any chosen conversion type, topology, order and path number with the desired NTF provided in Chapter 3.

In *Chapter 6,* the concluding remarks of the overall thesis are reviewed. The recommendations for future work are also discussed.

## Chapter 2. Data Converters

Analog circuitry unavoidably suffers from non-ideality issues such as manufacturer errors, thermal noise and component mismatches [21]. Apart from a few non-idealities such as clock jittering, finite wordlength and propagation delays, circuit performance is more settled in the digital world. As long as the values of 1s and 0s do not change their states, the non-idealities in the digital world do not affect the overall circuit performance. Moreover, data storage in the digital domain is much more effective and easy. Thus, data conversion plays a vital role in a wide range of implementations from biomedical devices to communication technologies, as the real world is completely analog.

Data conversion is a dual-way street: A/D and D/A. In Figure 1, the data conversion block diagram is given. As seen, an analog signal is filtered, sampled and then converted to a digital word stream. After the processing of the digital signal, a D/A conversion block and an analog filter reconstruct the processed signal.

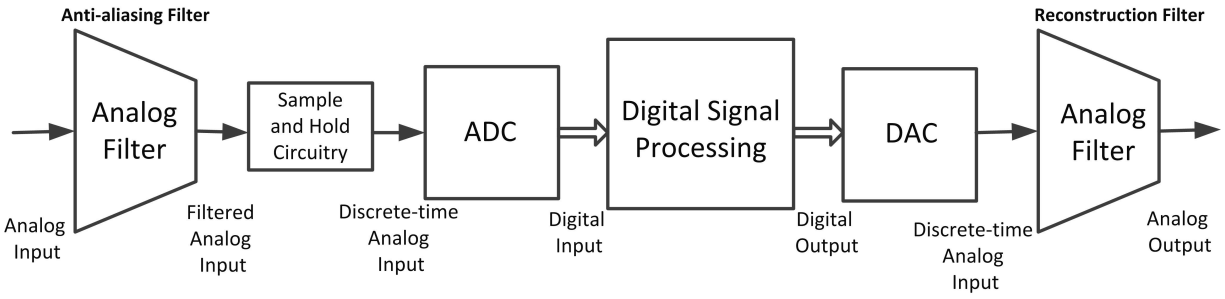



**Figure 1: Data Conversion Block Diagram**

This section firstly investigates the sampling and the quantization, as these are the vital blocks of data conversion in which the fundamental amount of noise is added to the signal. By simply utilizing these two blocks, one can build a conventional Pulse Code Modulation (PCM) data converter. It is important to go through the basics of PCM to have a better understanding of Σ-Δ modulation and how it achieves higher resolution in combination with simpler hardware.

Thereafter the principles of Σ-Δ modulation are explained. The limitations of its ability to fulfil the emerging technologies' requirements are identified and addressed. A comprehensive literature survey is also carried out to identify the state-of-the-art and any areas that are worthy

of further investigation in the field of Σ-Δ modulation. As a solution, the Time-Interleaving method and VBP Σ-Δ modulators are presented. Finally, performance parameters are defined in order to compare and evaluate the resolution of the designed Σ-Δ modulator topologies.

## 2.1 Sampling and Pre-Filtering

Sampling is the conversion of a continuous time analog signal $x(t)$, into a discrete time analog signal $x[n]$. The sampling frequency $f_s$ should be at least twice the signal bandwidth to meet the Nyquist criteria [22]. This is due to the fact that sampling results in signal images at the frequencies $kf_s$ as given in (1), where $T_s$ is the sampling interval. These images are also depicted in Figure 2 where $f_B$ is the signal band.

$$X_{samp}(f) = \frac{1}{T_s}\sum_{k=-\infty}^{\infty} X(f - kf_s) \tag{1}$$

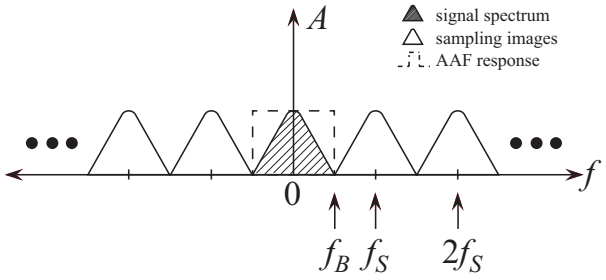



**Figure 2: Sampled Signal Spectrum**

However, in real life, signals are not band-limited and may have high frequency tones, which will result in aliasing after sampling. Therefore, pre-filtering is always required before the sampling process to ensure a band-limited signal. The pre-filter is called the Anti-Aliasing Filter (AAF). As seen in Figure 3, the higher the $f_s$ is chosen, the more relaxed an AAF is needed. Moreover, a high sampling frequency will result in higher resolution both for the A/D and D/A converters.

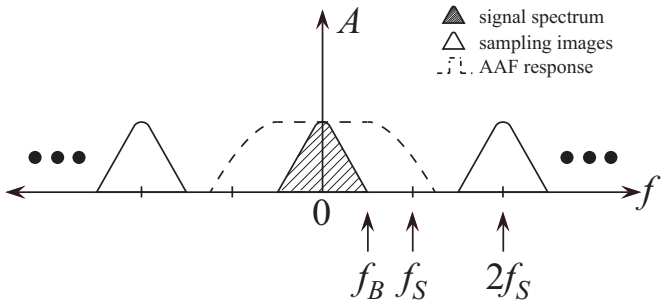



**Figure 3: AAF and Aliasing**

## 2.2 Quantization

The second step of signal processing is the A/D conversion in which sampled and band-limited data is converted to digital data. The conventional Analog to Digital Converter (ADC) can be constructed by using a quantizer after the sampling block as seen in Figure 4. Since the quantizer itself maps the sampled data to a digital quantization level, the output is purely digital. However, this ADC scheme, in other words PCM technique, demands multi-bit quantizers to achieve high resolution. Thereby it increases the overall hardware complexity [23].

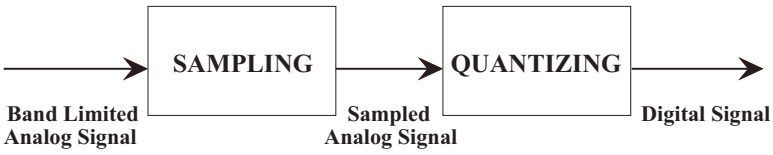



**Figure 4: PCM A/D Converter**

At this point it is rational to roughly inspect the quantization before getting into the Σ-Δ modulation technique. Hence the A/D and D/A conversion blocks are investigated in detail in Chapter 3 and Chapter 4.

Quantization is the process where discrete amplitude data are converted into a digital data stream. The basic concept is illustrated in Figure 5. Note that uniform sampling is employed within this study where the quantization steps, "$\Delta_Q$"s, are taken to be equal.

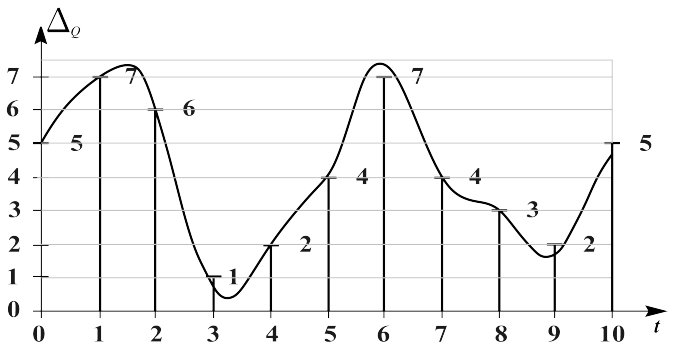



**Figure 5: Quantization of a Sampled Analog Signal**

The sampled input data $x[n]$ is rolled over to the nearest quantization level resulting in a discrete time and discrete amplitude data stream. This rolling process inevitably causes an error at the output, known as the quantization noise.

As depicted in Figure 5, quantization is a highly non-linear operation which is mathematically hard to model. The commonest approximation to define its behaviour is the Additive White Gaussian Noise (AWGN) approach. As seen in Figure 6, the AWGN equates the output of a quantizer, $y[n]$, to the sum of the input signal, $x[n]$, and the quantization noise, $e[n]$. Moreover, the probability density function of the quantization noise, $P_e(e)$, is assumed to have a uniform distribution between $\pm\ \Delta_Q/2$ as illustrated in Figure 7.

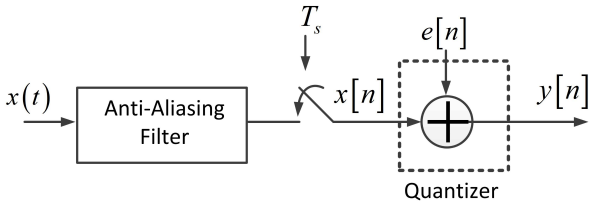



**Figure 6: AWGN Block Diagram**

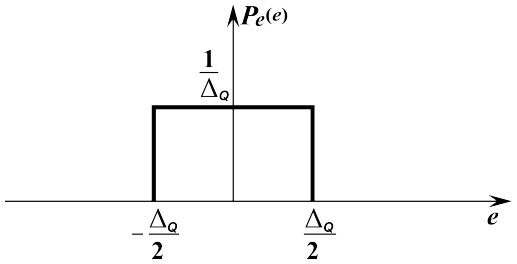



**Figure 7: White Quantization Noise**

In (2), the power of the white quantization noise is calculated where $\sigma_e$ is the quantization noise and $\Delta_Q$ is the quantization step. Assuming an N-bit quantizer with a maximum output level of $V$, the quantization step can be calculated as $2V/2^N$. So (2) is recalculated in (3) resulting in the SNR formula given in (4) where $\sigma_s^2$ is the input signal power. Note that for every *N* increment there is a corresponding 6 dB SNR increment. Equation (4) clearly depicts this for high resolution where a higher number of bits in the quantizer is required.

$$\sigma_e^2 = \int_{-\Delta_Q/2}^{\Delta_Q/2} \frac{1}{\Delta_Q} e^2 de = \frac{\Delta_Q^2}{12} \tag{2}$$

$$\sigma_e^2 = \frac{\left(\frac{2V}{2^N}\right)^2}{12} \tag{3}$$

$$SNR = 10\ log \frac{\sigma_s^2}{\sigma_e^2} = 10\ log \frac{\sigma_s^2}{V^2} + 4.77 + 6.02N\ dB \tag{4}$$

The SNR calculation in (4) is for an ideal PCM ADC. In real-life implementations, there occurs input referred noise such as thermal noise and flicker noise. Hence the obtained SNR is lower than the calculated SNR. Therefore, designers generally calculate the Effective Number Of Bits (ENOB) as a performance metric. The ENOB measures the actual resolution in bits of an operating ADC. The IEEE standard 1241-2000 defines the ENOB as a measure of the signal-to-noise and distortion ratio (SINAD) used to compare actual ADC performance to an ideal ADC [24]. The ENOB formula is given by the equation in (5) and the equivalent equation to calculate SINAD is given in (6). Note that the IEEE standard 1241-2000 calculates the ENOB assuming a sine wave input to the ADC. Therefore, *A* refers to the amplitude of the sine wave and $V$ represents the full-scale range of the ADC/DAC under test.

$$ENOB = log_2(SINAD) - \frac{1}{2} log_2(1.5) - log_2\left(\frac{A}{V/2}\right) \tag{5}$$

$$SINAD = \sqrt{1.5}\left(\frac{A}{V/2}\right) 2^{ENOB} \tag{6}$$

On the other hand, (4) assumes that the entire band from DC to the sampling frequency is required for the conversion. However, the conversion band is generally limited to the input signal band. If the in-band quantization noise is reduced, the SNR will increase. A common

way to decrease the in-band noise is to use oversampling. The idea of oversampling is that the uncorrelated quantization noise is averaged by a higher number of samples. As a result, the Power Spectral Density (PSD) of the quantization noise is distributed over a larger frequency band decreasing the in-band quantization noise as seen in Figure 8. Assuming a baseband signal, the reduced quantization noise by the use of oversampling can be further decreased with the help of a Low Pass Filter (LPF).

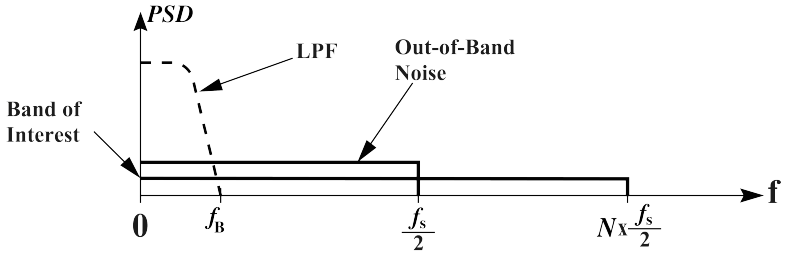



**Figure 8: Oversampling and Quantization Noise**

Consequently, oversampled converters can achieve the desired SNR with a fewer number of quantization bits. The attractiveness of fewer quantization bits is the drastically reduced Digital to Analog Converter (DAC) circuitry utilized in the feedback loop of the A/D converters [25]. Specifically, if a one-bit quantizer is employed, the resulting DAC circuitry is just a comparator. A one-bit quantizer not only reduces the DAC circuitry but also eliminates the DEM circuitry that is required to cancel the non-ideal behaviour of the DAC.

By the same token, D/A converters suffer from the problem of having a multi-bit input. As the digital data coming through the DAC is multi-bit, the resulting circuitry is complex [25]. Hence, modulation is required before the D/A conversion in which the multi-bit input data is converted to a coarse, lower-bit data in order to reduce the DAC circuitry and mitigate its non-ideal behaviour.

## 2.3 Σ-Δ Modulation

Σ-Δ modulators offer high resolution and relatively simpler hardware therefore they are widely chosen in many applications for data conversion. When they were first introduced in the market in the 1960s, they were mostly used for audio implementations due to their high OSR requirements [7], [8], [26]. However, as technologies developed and processors achieved

higher speeds, Intermediate Frequency (IF) applications, such as in frequency synthesizers [27], switched-mode power supplies [28] and software defined radios [29]; also used the Σ-Δ modulation technique. The fundamental concept underpinning Σ-Δ modulation is to combine noise-shaping and oversampling to achieve high resolution therefore decreasing the number of bits in the quantizer. This in return significantly reduces the hardware required for the DAC and relaxes the steepness of the AAF behaviour.

Σ-Δ modulators utilize a feedback loop and a loop-filter to shape the quantization noise arising from the quantizer itself. The basic structure of a Σ-Δ modulator for an A/D conversion is seen in Figure 9. A decimator is placed after the Σ-Δ modulator to filter the output data and down-convert it to the Nyquist rate. Note that for the D/A modulator the DAC in the feedback loop is removed, instead a DAC is placed after the decimator as seen in Figure 10.

To differentiate between A/D and D/A Σ-Δ modulation, N-bit and M-bit quantizers are put within the block diagrams respectively. Once again, an A/D Σ-Δ modulator converts a sampled input data to an N-bit digital data stream whilst a D/A Σ-Δ modulator converts an N-bit digital data to a coarse M-bit digital data where M<N. The D/A conversion is performed by the M-bit DAC placed after the decimator therefore saving both hardware and power consumption. This study utilizes 1-bit quantizers for both topologies resulting in a comparator for the DAC topology and eliminating the DEM circuitry required to amend the non-ideal behaviour of the DAC.

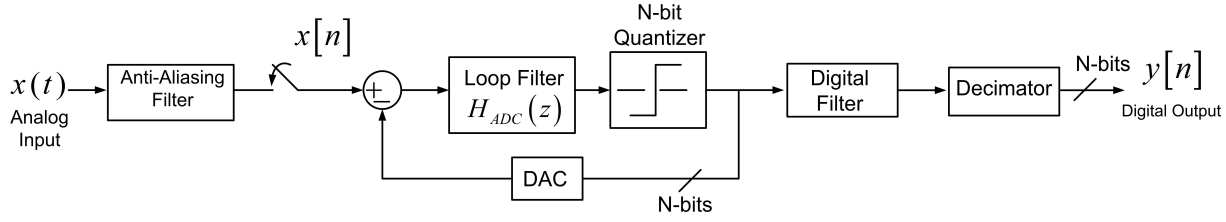



**Figure 9: A/D Σ-Δ Modulator**

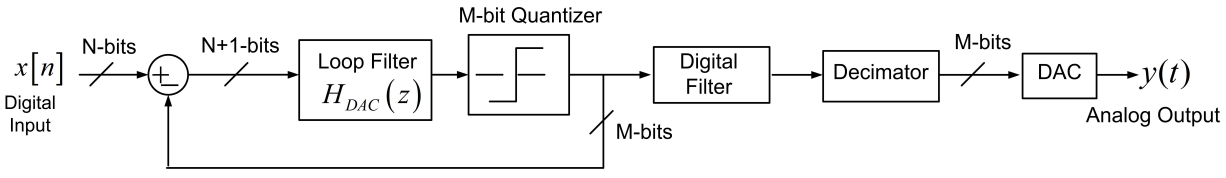



**Figure 10: D/A Σ-Δ Modulator**

### 2.3.1 Noise-Shaping

Noise-shaping is the term used for quantization noise filtering. This is where the in-band noise is reduced using a suitable NTF and the suppressed quantization noise is pushed to the out-of-band region as shown in Figure 11.

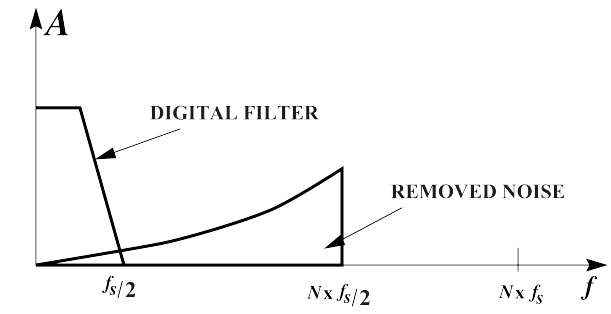



**Figure 11: Noise Shaping and Oversampling**

If the AWGN is utilized to mathematically model the quantizer behaviour as seen in Figure 12, the resulting equation is obtained in (7). $X(z)$ is the input to the Σ-Δ modulator whilst $E(z)$ represents the quantization noise. The Signal Transfer Function (STF) shapes the input signal, whereas the NTF shapes the quantization noise. The NTF is the most important part of the design process, as it has to ensure Σ-Δ modulator stability, minimise tonality and at the same time deliver the required SNR and DR.

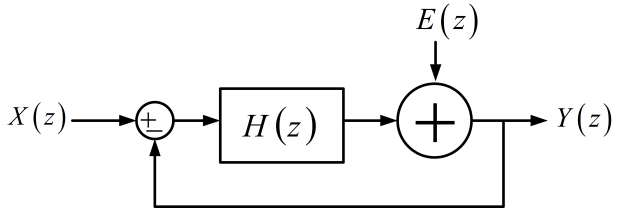



**Figure 12: AWGN Model in Σ-Δ Modulator**

$$Y(z) = X(z)\frac{H(z)}{1+H(z)} + E(z)\frac{1}{1+H(z)} \tag{7}$$

$$STF(z) = \frac{H(z)}{1+H(z)} \tag{8}$$

$$NTF(z) = \frac{1}{1+H(z)} \tag{9}$$

### 2.3.2 Oversampling

In addition to the noise-shaping, Σ-Δ modulators employ high OSR to spread the quantization noise over a wider frequency band as well as moving the sampling images further apart, thereby relaxing the AAF [30-32]. This was shown in Figure 3. As known from filter theory, a relaxed AAF can be implemented using simpler hardware. So, higher OSRs not only result in higher SNRs but also reduce the overall hardware. The OSR is defined in (10) where $f_s$ is the sampling frequency and $f_B$ is the bandwidth of the signal. After all, a high OSR is a trade-off between bandwidth and processor speed.

$$OSR = \frac{f_s}{2f_B} \tag{10}$$

Consequently, with the help of noise-shaping and oversampling, Σ-Δ modulators achieve high resolution in conjunction with a reduced number of quantizer bits. The reduction in the quantizer bits and the relaxed AAF topology simplify the overall hardware providing lower power consumption. By using a single-bit quantizer, a Σ-Δ modulator can accomplish resolution as high as the equivalence of 20-bits as reported in [33], [34].

## 2.4 BP Σ-Δ Modulation

The majority of published work presents the Low-Pass (LP) Σ-Δ modulators. Obviously this is due to the baseband applications that extensively use the Σ-Δ modulation technique. These baseband applications, such as in audio implementations, do not suffer from the high-speed requirements of the Σ-Δ modulators [35], [36]. As a result, there is already a huge amount of know-how for the LP Σ-Δ modulators in terms of design, system-level modelling, simulations and implementation.

Therefore, the basic design method of a bandpass Σ-Δ modulator is to convert a LP Σ-Δ modulator prototype to its bandpass counterpart. A basic BP Σ-Δ modulator can be built by replacing the integrator blocks of the already designed LP Σ-Δ modulator with resonator blocks. This assumes a delay-based integrator whose transfer function is given in (11). Basically by transforming the $z^{-1}$ to $-z^{-2}$, one can obtain a mid-band resonator as shown in (12).

$$H_{ID}(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{11}$$

$$H_{RMid}(z) = \frac{-z^{-2}}{1 + z^{-2}} \tag{12}$$

This easy conversion results in mid-band Σ-Δ modulators offering noise-shaping at the normalized frequency of $\nu = 0.25$. There are two main benefits of this conventional design method; firstly, the new BP Σ-Δ modulator preserves the performance metrics of the formerly designed LP Σ-Δ modulator that is the SNR, DR and the stability. Secondly, the mid-band resonator blocks are easy to implement both for Switched Capacitor (SC) circuits and digital circuits [7, 8]. However, these mid-band Σ-Δ modulators limit the flexibility of the overall system due to the fixed centre-frequency and bandwidth. Although the centre-frequency can be changed by appropriate feedback coefficients as shown in Figure 13 and calculated in (13), the bandwidth limitation still exists. More importantly, centre-frequencies close to DC or Nyquist result in unequal out-of-band gain levels of the NTF as depicted in Figure 14 and may result in instability especially for Σ-Δ modulators above second-order. It is worth pointing that 0 dB corresponds to an amplitude value of 1 for all the output frequency response plots in this thesis.

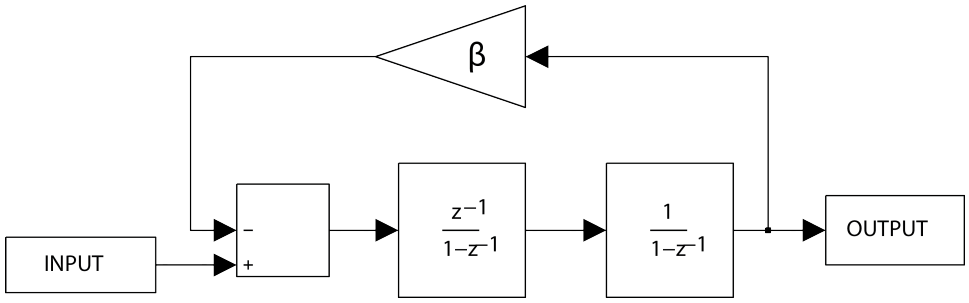



**Figure 13: Delayed Resonator Block**

$$H_R(z) = \frac{z^{-1}}{1 + (2 - \beta)z^{-1} + z^{-2}} \tag{13}$$

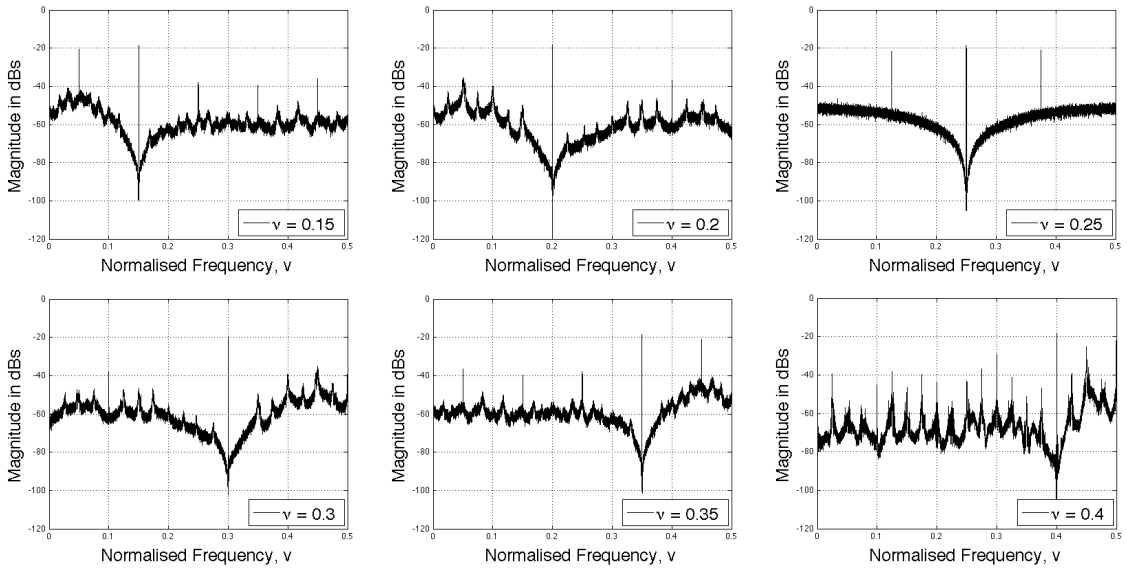



**Figure 14: Resonator-Based Second Order (Effective First Order) Σ-Δ modulator's Output Plots for Different Centre Frequencies**

## 2.5 Motivations for the TI VBP Σ-Δ Modulators

The traditional flash ADCs that directly convert the incoming signal through the comparators offer the fastest conversion technique. State-of-the-art flash ADCs are capable of operating up to 24 GHz of sampling frequency for 4-6 bits of resolution making them appropriate for high-speed and low-resolution technologies such as radar detection [37-42]. Other ADCs such as pipeline [43], [44] or successive approximation [45], [46] can provide higher resolution between 8-16 bits. Their conversion band, however, is limited to a few hundreds of MHz making them unsuitable for Radio Frequency (RF) signal conversion. But these converters are viable in moderate speed applications such as ultrasonic medical imaging, industrial controls and Charged Coupled Device (CCD) imaging. Subsampling may be introduced to such systems in order to overcome the speed limitation at the expense of performance degradation caused by the noise aliasing and the required high-quality BP AAFs [47].

The conventional LP Σ-Δ modulators are mostly employed by audio implementations where the bandwidth is around 20-30 kHz [48-50]. Thus high SNRs can be obtained without sacrificing much effort. On the other hand, there are reported implementations of up to 20 GHz of sampling frequency with a 1 GHz bandwidth range, where Continuous-Time (CT) Σ-Δ modulators are implemented by SiGe BiCMOS technology [51]. SiGe BiCMOS technology

might be promising for the future but at the moment SiGe wafers are extremely expensive to use in mass-production. In [52], a CT BP Σ-Δ modulator is built operating at 3.2 GHz of sampling frequency with a 1 GHz of bandwidth and it is implemented in CMOS technology. It should be noted that CT Σ-Δ modulators have the superior performance to operate at higher frequency but they are limited to a set of sampling frequencies [8]. Besides all the aforementioned conversion methods including the LP and mid-band Σ-Δ modulators, configurable bandwidth and centre-frequency BP Σ-Δ modulators are the best candidates to deploy in digitally intensive RF architectures for the emerging sub-micron technologies. These modulators provide high-speed and high-resolution conversion whilst maintaining the advantages of lower hardware complexity and cost.

In Figure 15, the aforementioned ADCs are compared in a single diagram in terms of their resolution and conversion bandwidth. Apparently, Σ-Δ modulators are attractive due to their high-resolution. However, the conversion bandwidth of these modulators limits their use to the narrow-band applications.

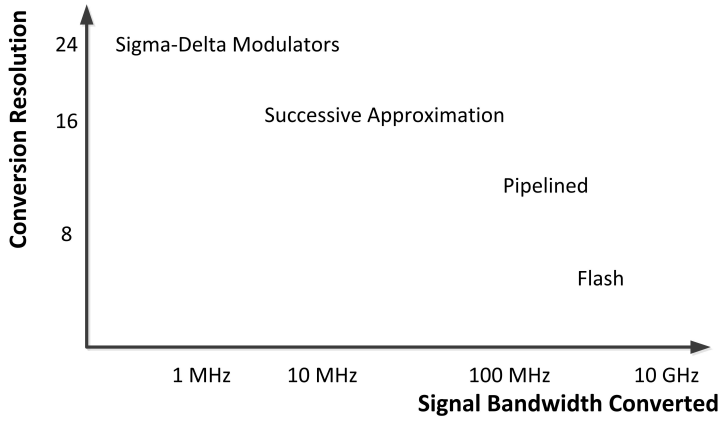



**Figure 15: Comparison of ADCs**

To clarify the motivation of this study, generalized VBP Σ-Δ modulators are designed to evaluate the entire frequency-band from DC to Nyquist with an adjustable bandwidth therefore offering greater flexibility for the design of BP Σ-Δ modulators. By supporting flexible topologies for the signal conditioning and the channelization, these generalized VBP Σ-Δ modulators make it possible to implement reconfigurable, multi-standard signal conversion. In addition, to achieve better resolution and/or to improve the integration of the system, the designer may fix these specifications to the desired values. For instance; in [53] a GSM

receiver Integrated Circuit (IC) is designed. However, to allow use of the IC in a broad range of narrow-band applications, including analog-FM, GSM/EDGE, the centre-frequency of the Σ-Δ modulator is fixed to $f_{clk}/8$. Therefore, the overall system's universal clocks can be switched to choose the desired conversion frequency.

Despite the flexibility and integration properties, designing a VBP Σ-Δ modulator has its own challenges. Primarily, bandwidth restriction is still an issue. High OSR requirements still apply limiting the modulator to narrowband applications. The proposed technique to ameliorate this situation is to utilize parallel Σ-Δ modulators to offer higher speed operation or increased conversion band. Specifically the chosen parallel structure is called the Time-Interleaved (TI) topology and is discussed in Section 3.3.2

Table 1 presents a list of Σ-Δ modulators, which compares their implementation performance in order to have a better understanding of the limitations of Σ-Δ modulation. Note that the the reference numbers in Table 1 are listed as presented in the References's chapter on page 192. As listed, with the help of the TI technique, designers managed to increase the overall sampling frequency therefore the required SNR values can be obtained by using lower-order Σ-Δ modulators. When [54-56] and [59] are compared, [59] increases the signal bandwidth with a lower sampling frequency by using an 8-path TI Σ-Δ modulator topology. On the other hand, although the orders of the Σ-Δ modulators in [55], [57] and [58] are the same, it is shown that the Σ-Δ modulator in [58] produces much higher SNR (i.e. 33 dBs and 36 dBs respectively) using lower sampling frequency. This superior SNR performance is attributed to its 2-path TI structure.

An extensive literature survey has revealed that all reported publications on TI topologies have been confined to LP and midband resonator-based Σ-Δ modulators as the recursive operation of Σ-Δ modulators complicate the TI conversion [60], [61]. Moreover, a great number of the architectures in the literature propose 2-path and low-order TI structures derived using the polyphase decomposition method [62-64]. This is due to the fact that polyphase decomposition of high order NTFs particularly for a higher number of interleaving paths is quite cumbersome to calculate [65]. Thereby the first aim of this study is to further develop the method proposed in [20] to enable the design of multi-path VBP Σ-Δ modulators. The

utilized and developed method is referred to as the Node Equation technique and is examined in Section 3.3.5.

**Table 1: Comparison of Σ-Δ Modulators in Use**

| Signal Band | Sampling Frequency | OSR | Modulator Structure | SNR | Reference |
|---|---|---|---|---|---|
| 10 MHz | 480 MHz | 24 | CT 3rd-order A/D | 70 dB | [54] |
| 100 MHz | 1 GHz | 5 | CT 2nd-order A/D | 43 dB | [55] |
| 500 kHz | 500 MHz | 500 | DT 1st-order A/D | 60 dB | [56] |
| 10 MHz | 50 MHz | 2.5 | DT 2nd-order A/D | 46 dB | [57] |
| 1.25 MHz | 50 MHz | 50 | DT 2-path 2nd-order TI D/A | 86 dB | [58] |
| 15.625 MHz | 250 MHz | 64 | CT 8-path 1st-order TI A/D | 45 dB | [59] |
| 1.25 MHz | 30 MHz | 50 | DT 5-path 2nd-order TI A/D | 48 dB | [60] |
| 80 MHz | 2.2 GHz | 27.5 | CT 2-path 1st-order TI A/D | 50 dB | [61] |

This thesis presents novel generalized TI VBP Σ-Δ modulators where designers are able to specify the centre-frequency, bandwidth, pass-band and stop-band attenuations. The flexibility of these modulators enables designers to integrate them with the overall system whilst providing larger bandwidth.

A step-by-step design technique is provided and performed for various A/D and D/A TI VBP-based Σ-Δ modulator topologies. This technique initially starts with developing SP VBP Σ-Δ modulator topologies and verifying their stability, tonality, SNRs and DRs by extensive behavioural-level simulations. The process commences with the design of the NTF, which is then mapped to an appropriate topology. Before selecting a suitable topology, the NTF specifications should be determined to ensure stability, adequate SNR and DR. In this sense, employing different filtering types where the designer has the control over the centre-

frequency and the bandwidth is indispensible. The NTF design in this study circumvents the imbalance in the shoulder gain levels by making use of Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical narrow-band filters, thus delivering more stable Σ-Δ modulators. The second step is to convert these SP VBP Σ-Δ modulators to their P-path TI counterparts. Thereafter, all the designed topologies are investigated including their performance and immunity to non-idealities. The node-equation technique presented for LP Σ-Δ modulators in [20] and further developed for VBP Σ-Δ modulators is detailed in Section 3.2. Finally, Matlab routines in conjunction with SIMULINK models were wrapped in a GUI environment to automate and speed-up the calculations.

**Contributions and Novelties**

The developed and novel contributions of this PhD study are listed in bullet points. The developed contributions' bullet points start with a 'D' whereas the novel contributions' bullet points start with an 'N'.

- **D:** A step-by-step design technique for generalized TI VBP Σ-Δ modulators is developed. This technique is an extension of the node-equation method. The node equation method is applied to a generalized NTF, and resulting generalized SP topologies are converted to their TI counterparts by using the node-equation technique.
- **N:** Using the developed design method, over 36 SP and multi-path Σ-Δ modulators are designed, analysed and evaluated. These generalized VBP Σ-Δ modulators are capable to perform noise-shaping at a desired centre frequency with the chosen bandwidth, passband and stopband attenuations.
- **D:** Simulation routines calculating the filter coefficients and overall performance of TI VBP Σ-Δ modulators are developed in MATLAB and evaluated with SIMULINK models.
- **D:** The proposed VBP Σ-Δ modulators are evaluated for many different centre frequencies and bandwidths.
- **D:** $6^{th}$- and higher-order CI-FBFF Σ-Δ modulator topologies whose normalised centre-frequencies lie within [0.25 0.5] are shown to be unsuitable for implementation. This is attributed to their large feedback and feedforward coefficients.

- **D:** A/D TI VBP Σ-Δ modulators' non-idealities are extensively evaluated at the behavioural level.
- **D:** A/D and D/A VBP Σ-Δ modulators that use Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters are compared and evaluated in terms of SNRs, DRs, tonality and hardware complexity.
- **N:** Significant reductions to the number of coefficients and internal connections are made for the OF D/A TI VBP Σ-Δ modulators.
- **N:** The tonal behaviour of quantizers when excited by single sinusoidal signal is mathematically modelled and verified both for A/D and D/A VBP Σ-Δ modulators. The model is called the sawthooth quantization noise model.
- **N:** The sawtooth quantization noise model is extended for the TI topologies and verified both for TI A/D and D/A VBP Σ-Δ modulators.
- **N:** $4^{th}$-order, SP, 2-path and 4-path D/A VBP Σ-Δ modulators are implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit.
- **N:** To further enhance the flexibility of the TI VBP Σ-Δ modulators, a $2^{nd}$-order reconfigurable and tunable D/A TI VBP Σ-Δ modulator topology is built and implemented.
- **N:** The SIMULINK models and MATLAB codes are combined in a GUI.

## 2.6 Performance Parameters

The main performance parameters that define a Σ-Δ modulator's overall behaviour are the SNR, DR, stability and tonality.

### 2.6.1 Signal to Noise Ratio

The Signal-to-Noise Ratio (SNR) of a Σ-Δ modulator is the ratio of the signal power to the in-band noise power. On page 10, the SNR is defined and calculated in (4) for a PCM converter. The SNR of a Σ-Δ modulator differs from the SNR of a PCM converter in two aspects. Firstly, the in-band noise that is shaped by the NTF should be taken into account for the SNR calculations. Secondly, the noise at the output of the modulator is not only composed of the quantization noise. There are some other noise sources in real life such as thermal noise and flicker noise that need to be considered. However, it is hard to approximate these noise

sources before designing the circuitry. Therefore in (16), equation (14) is recalled where the noise-shaping and bandwidth are taken into the equation in order to have a projection of the expected SNR. $\sigma_n^2$ is used to define the shaped noise power whereas the quantization noise power is defined by $\sigma_e^2$. $S_q(f)$ is the PSD of the non-shaped quantization noise and is equal to $S_q(f) = \sigma_e^2/f_s$. $f_{c1}$ and $f_{c2}$ are the cut-off frequencies of the designed band-pass filter. Note that for a lowpass Σ-Δ modulator $f_{c1}$ equals to $-f_{c2}$. By making proper alterations in (15), (22) is calculated.

$$SNR = 10\log\left(\frac{\sigma_s^2}{\sigma_e^2}\right) \tag{14}$$

$$\sigma_n^2 = \int_{f_{c1}}^{f_{c2}} S_q(f)\left|NTF(f)\right|^2 df \tag{15}$$

$$SNR = 10\log\left(\frac{\sigma_s^2}{\sigma_n^2}\right) = 10\log\frac{\sigma_s^2}{\int_{f_{c1}}^{f_{c2}} \sigma_e^2/f_s \left|NTF(f)\right|^2 df} \tag{16}$$

$$SNR = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_e^2 f_B/f_s \int_{f_{c1}}^{f_{c2}} \left|NTF(f)\right|^2 df\right) \tag{17}$$

$$SNR = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_e^2\right) - 10\log\left(\int_{f_{c1}}^{f_{c2}} \left|NTF(f)\right|^2 df\right) - 10\log\left(f_B/f_s\right) \tag{18}$$

$$SNR = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_e^2\right) - 10\log\left(\int_{f_{c1}}^{f_{c2}} \left|NTF(f)\right|^2 df\right) + 10\log\left(f_s/f_B\right) \tag{19}$$

$$SNR = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_e^2\right) - 10\log\left(\int_{f_{c1}}^{f_{c2}} \left|NTF(f)\right|^2 df\right) + 10\log\left(2OSR\right) \tag{20}$$

$$If \quad OSR = 2^r \tag{21}$$

$$SNR = 10\log\left(\sigma_s^2\right) - 10\log\left(\sigma_e^2\right) - 10\log\left(\int_{f_{c1}}^{f_{c2}} \left|NTF\left(f\right)\right|^2 df\right) + \left(3 + 3r\right) dB \qquad (22)$$

Every doubling in the OSR is supposed to increase the SNR by 3 dBs. In [7] the NTF integration is calculated for LP, integrator-based NTFs. The resulting SNR estimation is that; for every doubling of OSR an SNR increment of (*6L+3*) dB is expected, where L is the order of the modulator. In Section 3.6 the obtained SNRs are discussed, where it is shown that the (*6L+3*) dB increment cannot be obtained for the VBP Σ-Δ modulators when the OSR is doubled.

In this study, the SNR is directly calculated from the actual Σ-Δ modulator output using Matlab routines to obtain a more accurate value. This is due to the fact that the quantization operation is highly non-linear and an assumption is used to model its behaviour. This causes deviations in the noise-shaping. Furthermore, limit cycle tones, quantization tones and dithering noise are also added to the output that cannot be estimated by (16).

### 2.6.2 Dynamic Range

The Dynamic Range (DR) of a Σ-Δ modulator is defined as the ratio between the maximum and the minimum detectable signal amplitude values. The maximum detectable signal highly depends on the quantizer overload level, which drives the Σ-Δ modulator into unstable mode. The minimum detectable signal level depends on the noise-floor and is generally determined by the dither.

### 2.6.3 Stability

The stability of a Σ-Δ modulator is affected by many parameters. There is no precise mathematical model presented to-date that determines the stability of a Σ-Δ modulator. This in return, requires researchers to perform numerous iterative simulations in order to acquire an NTF that suitably meets the required design specifications.

A Σ-Δ modulator is said to be unstable if the output produces alternating long strings of 1s and 0s as is the case with low frequency oscillations. Another aspect of an unstable modulator is that the modulator exhibits quite large or unbounded states. In other words, the input

amplitude to the quantizer accumulates and results in extremely low gains for the quantizer. Consequently, the Σ-Δ modulator fails to perform noise-shaping. Both definitions are valid and need to be inspected.

In [66], the stability of a Σ-Δ modulator was shown to correlate with the NTF out-of-band gain where a rule of thumb was developed based on detailed simulations. Lee's stability criterion is widely used and is given by:

$$|NTF(z)| < 2 \tag{23}$$

In [67], the power of the NTF, rather than the gain is inspected. The resulting rule of thumb is called the power gain rule. According to [67], the total power of the normalized NTF needs to be less than 3 for the modulator to be stable. However, these rules are not sufficient to determine the stability of a Σ-Δ modulator. Because [66] is based on the simulation result of a fourth-order LP Σ-Δ modulator and in [67] the white noise assumption is used.

In the linear model, a more deterministic approach is provided. The idea is to model the quantizer as a variable gain block and a binary quantizer as seen in Figure 16. Thus the correlation of the input signal, modulator states and the modulator output are ensured. The resulting equations are calculated in (24) and (25) with the help of the linear quantizer noise model.

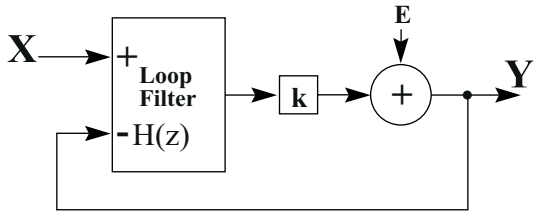



**Figure 16: Linear Stability Model**

$$STF(z,k) = \frac{kH(z)}{1+kH(z)} \tag{24}$$

$$NTF(z,k) = \frac{1}{1+kH(z)} \tag{25}$$

To investigate for the stability of the Σ-Δ modulator the root locus is plotted. If for all values of k the poles of the NTF remain within the unit-circle, the modulator is said to be stable. Otherwise the input-signal statistics are needed to determine the stability boundaries of the Σ-Δ modulator. It should be noted that the root locus method is applied to the designed TI VBP Σ-Δ modulators to ensure their stability.

In [9], the modulator is split into two linear subsystems for the signal and for the noise as seen in Figure 17. The idea of this method is to correlate the PSD of the subsystems‘ quantizer outputs using describing functions. However, for higher-order modulators, solving these nonlinear equations is cumbersome and can be done using numerical methods.

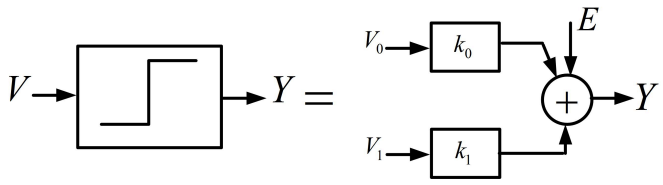



**Figure 17: Split Quantizer**

### 2.6.4 Tonality

Σ-Δ modulators may suffer from unwanted tones that will cause instability and/or ear detectable periodicities. Once again the non-linear nature of quantization interferes with the calculation of these tones, making it very hard to predict the frequencies and the amplitude of these tones.

Σ-Δ modulators act like Finite State Machines (FSMs) producing a set of states within certain periods. If the output state varies with a period of $T_L$, it is highly possible to observe tones at $f_s/T_L$. These tones are known as limit cycle oscillation tones and are mostly seen in non-linear systems. However the presence and the amplitude of these limit cycle oscillation tones also depend on the input amplitude, input frequency, quantization step and modulator order [67].

Idle channel tones describe an alternative type of tonality. They are generally observed at distinct frequencies superimposed on a noise background as depicted in Figure 18. A very common assumption about idle channel tones is that they are aliased high frequency harmonics of the limit cycle tones [69]. There are also some authors who assume that all

tonality sources in Σ-Δ modulators are caused by the periodic behaviour of the states. This depends on a number of variables such as the input amplitude, input frequency, quantization steps, modulator topology and modulator order. These tones may alias, diminish or be amplified.

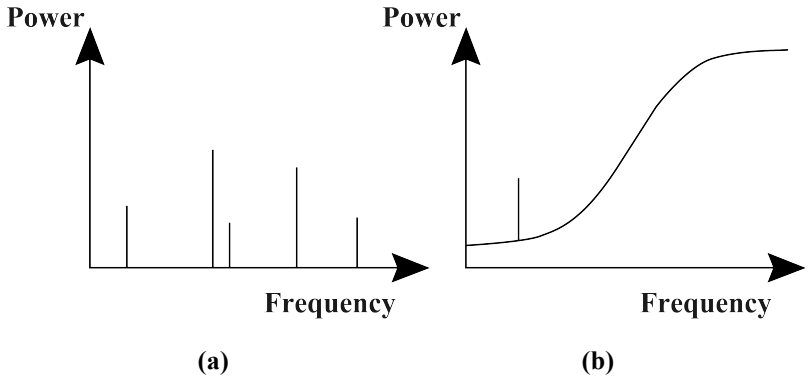



**Figure 18: a) Limit Cycle Tones b) Idle Channel Tones**

Papers that calculate the amplitude and frequency of these tones either use the AWGN approximation and/or successive simulation tools. Mostly, papers report individual topologies seeking tone-free or at least less tonal responses. These publications mainly agree on;

- Σ-Δ modulators whose inputs are periodic or DC produce more tones in their outputs.
- Lower order Σ-Δ modulators suffer from more tonality when compared to higher-order Σ-Δ modulators.
- Multi-stage Σ-Δ modulators are less prone to tonality when compared to single-stage Σ-Δ modulators.
- Initial conditions may play a vital role to break the short cycles therefore reducing the unwanted tones at the Σ-Δ modulator's output.
- Randomization is the key solution to these idle channel tones and can be accomplished either by employing more complex Σ-Δ modulator structures; or adding dither noise within the feedback loop.

Another cause for the unwanted tones is the quantization of the input signal and harmonic distortion. This will be addressed and mathematically modelled in Sections 3.11 and 4.3 for sinusoidal input signals. Moreover, TI topologies specifically suffer from channel mismatch tones that are elaborately discussed in Section 3.11.3.

### 2.6.5 Dithering

Dither refers to a source of white noise that is used to randomise the strong tones that appear at the output. However, dither inevitably increases the noise floor. Still, it is best injected at the quantizer input to take advantage of the noise-shaping process.

## 2.7 Concluding Remarks

The main objective of this chapter was to present the motivations of generalized TI VBP Σ-Δ modulators. In the first place, the gaps in the theory are defined. Therefore, the case for the design of generalized VBP Σ-Δ modulators was made. The basic principles of data conversion are explained covering quantization, sampling and their mathematical analysis.

Secondly, Σ-Δ modulators are presented as a solution to the conventional Nyquist rate PCM converters. However these modulators lack speed due to their high OSR requirements and are limited to baseband applications. BP Σ-Δ modulators provide solutions for narrow band RF applications as these modulators are confined to mid-band operations and there is no control over the conversion band.

To this extent, generalized VBP Σ-Δ modulators are the best candidates allowing noise-shaping at the desired centre-frequency with an adjustable bandwidth. However, these Σ-Δ modulators still suffer from high OSR requirements and are more suitable for narrow band applications. The TI technique is presented as a solution to overcome this narrow band restriction. A detailed up-to-date literature survey is discussed covering the fundamental TI conversion techniques, their applications and implementations. The node equation method is identified for its ease of application and therefore is chosen in the conversion of SP VBP Σ-Δ modulators to their TI counterparts. The node-equation method is subsequently extended for VBP Σ-Δ modulators and a step-by-step technique is developed. This process can be used to construct the P-path generalized TI VBP Σ-Δ modulators and is detailed in Section 3.3.5.

Finally, the main performance criteria that can be used to compare and evaluate the performance of the designed Σ-Δ modulators are defined and explained.

# Chapter 3. A/D TI VBP Σ-Δ Modulators

An A/D converter is the key building block for a highly digitized and monolithic receiver. To clarify this statement, a superheterodyne receiver architecture is depicted in Figure 19. Superheterodyne receivers firstly invented in 1910s are still widely used these days [70]. The idea is to modulate the input RF signal to a fixed IF frequency by means of a mixer. The modulated IF signal is then filtered and amplified to ensure a band-limited signal for A/D conversion. In order to have multi-channel implementation, a superheterodyne receiver requires discrete analog RF amplifiers and mixer blocks, which are highly complex to build and power consuming. Clearly the superheterodyne receiver is not suitable for integration.

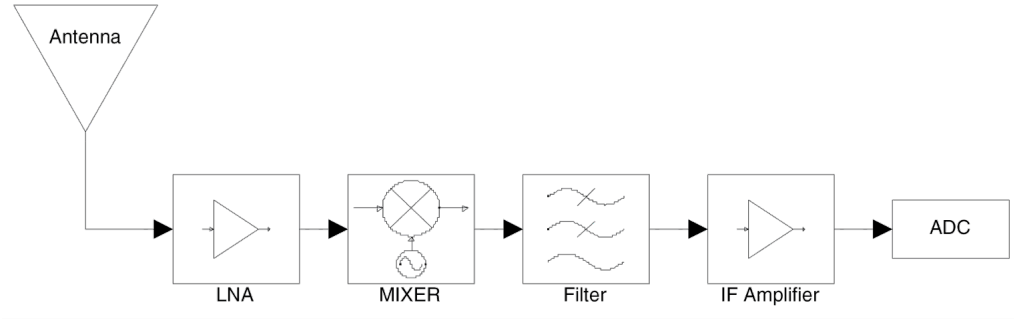



**Figure 19: Superheterodyne Receiver**

On the other hand, a direct conversion scheme also known as the homodyne receiver eliminates the passive filtering therefore providing better integration when compared to the superheterodyne receiver. The principle is to convert the RF signal to baseband frequency using a quadrature mixer [71]. Thereafter the analog baseband signal is applied to an ADC. The block diagram of a homodyne receiver is given in Figure 20.

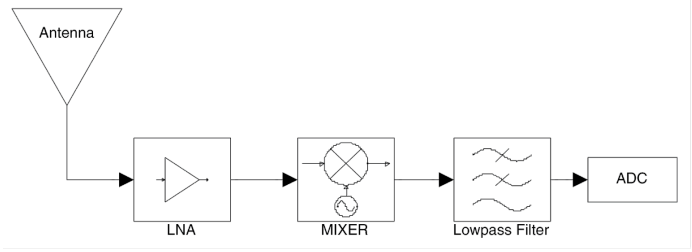



**Figure 20: Homodyne Receiver**

However, the direct conversion suffers from DC offset, I/Q mismatch as well as flicker noise problems. Rather than applying baseband conversion, low-IF conversion may be utilized to avoid DC offset and to mitigate the flicker noise. Yet, the LPF needs to be replaced with complex Band Pass Filters (BPF)s. Complex BPFs are not only hard to build but also use the double the chip area and therefore increase power consumption [72].

All these problems can be overcome by employing BP Σ-Δ modulators as depicted in Figure 21. Note that the mixer circuit and passive circuitry are excluded. The flicker noise and DC offsets are also avoided.

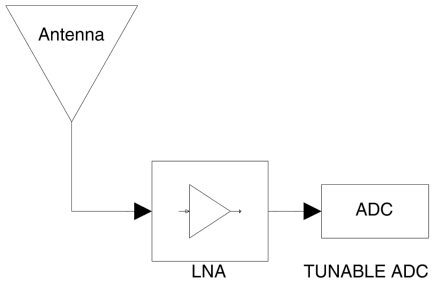



**Figure 21: Prospective Receiver with Tunable ADC**

The underlying problems of BP Σ-Δ modulators are defined in Section 2.4. A summary of the issues is listed below.

1. A conventional BP Σ-Δ modulator design can be derived from its LP prototype using the $z^{-1}$ to $-z^{-2}$ transformation. The resulting modulators are resonator based midband Σ-Δ modulators, which may have stability issues.
2. There is no control over the bandwidth of the NTF, which results in Σ-Δ modulators that are confined to narrow-band applications.
3. Flexibility of the overall system is restricted since the conversion frequency is fixed. In addition, multi-mode, multi-channel implementations suffer from signal aliasing.

The VBP Σ-Δ modulators, presented in Section 2.4, overcome the above limitations and offer the advantages listed below.

1. Flexibility is introduced where the designer is able to specify the center frequency bandwidth, stopband and passband attenuations from a menu of filters. This in return provides:
    a. More stable Σ-Δ modulator topologies.
    b. Improved integration for IC circuits.
    c. Improved SNR and DR.
2. The narrow band restriction is overcome by the time-interleaving technique thus enabling higher frequency and wider band conversion.

## 3.1 VBP Σ-Δ Modulator Design

It is anticipated due to the above benefits that VBP Σ-Δ modulator will become more widespread. Several Σ-Δ modulator structures are proposed and the entire frequency band from DC to Nyquist is investigated and evaluated in this study. To do so, generalized topologies are built that are capable of noise-shaping at any desired frequency for Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters.

A VBP Σ-Δ modulator can be designed for specific applications where the centre frequency, bandwidth, pass-band and stop-band attenuations can be prescribed by the designer. The system's clock and signal's bandwidth can be directly utilized whilst keeping the modulator stable. The required SNR can also be obtained with the help of different filters. In this sense the designer can attain a fully integrated signal conversion as no mixer circuitry and pre-filtering is required.

Another benefit is that the digital processor can be clocked with the highest value if required, as there is no frequency restriction of the data conversion. For example, the input signal with a centre-frequency equal to $f_x$ and the processor can be clocked at $10f_x$. If a conventional BP Σ-Δ modulator is employed, the sampling frequency needs to be $4f_x$. However, if a VBP Σ-Δ modulator is employed with a centre frequency of $\nu = 0.1$ as seen in Figure 22, the designer will get the benefit of high speed processing as well as the higher OSR.

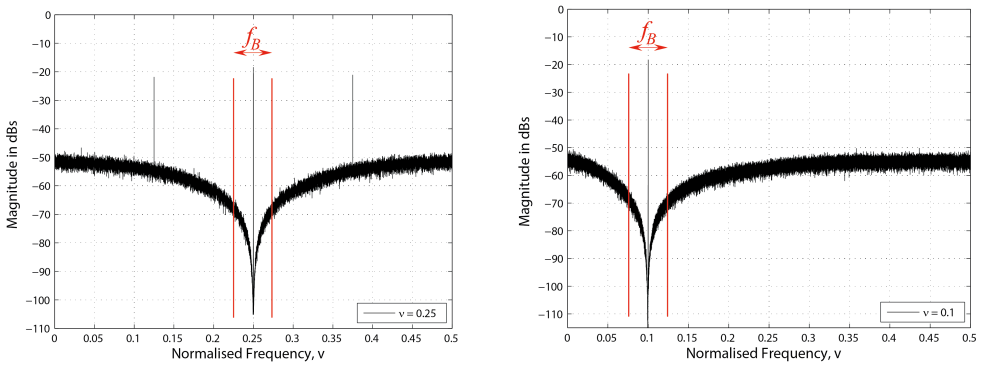



**Figure 22: Output Plots for Different Clock Frequencies**

Another advantage of VBP Σ-Δ modulators is that tunable, multi-mode and/or multi-channel data conversion is made feasible. As already stated, there is not much work reported in the open literature on VBP Σ-Δ modulators with the exception of a few publications on tunable or programmable ADCs that focus on tuning the centre-frequency of the modulator to the already defined fixed values [73-75]. In [73], 9 different centre-frequencies from $0.1f_s$ to $0.4f_s$ are predetermined and can be tuned. In [74], the centre-frequency can be tuned from DC to $0.31f_s$ with intervals of 0.052 $f_s$. In [75], 5 different centre-frequencies can be selected from DC to 1GHz.

The terms tunable and programmable slightly differ from each other. Tunable converters are mostly built with CT Σ-Δ modulators where a set of frequencies can be tuned to the chosen frequency band. In other words, channel selection is achieved where the bandwidth is fixed. On the other hand, programmable converters are constructed using discrete-time Σ-Δ modulators, where the user can select the conversion band and centre-frequency using switches. Yet, during the literature survey, a few publications have drawn the attention of the author that tunable switched capacitor circuits are being investigated mostly for MEMs applications, making it possible to build tunable, discrete-time Σ-Δ ADCs [76-80]. For those who are interested in the implementation of these circuits, the general idea is to tune the time constant by switches in series with the capacitors.

## 3.2 Generalized VBP NTF Design

The design of a Σ-Δ modulator starts with the NTF. The SNR, stability and DR are all dependent on the NTF. Choosing a flat response for the NTF provides more stable Σ-Δ modulators as this evens the out-of-band gain levels close to DC and Nyquist. As a result overloading of the quantizer and accumulators is alleviated. Therefore Butterworth filters are widely employed to ensure stability of the Σ-Δ modulator. On the other hand, Chebyshev-based filters offer higher resolution as their transition bands are narrower and steeper when compared to Butterworth filters [7].

Since the intention in this thesis is to build generalized topologies, a generalized NTF is chosen to realize Butterworth, Chebyshev and Elliptical filter-based Σ-Δ modulators. The generalized NTF of an $\boldsymbol{L^{th}}$-order Butterworth, Chebyshev and Elliptical band-stop filter is given in (26). The coefficients of a suitable band-stop Butterworth, Chebyshev, Inverse Chebyshev or Elliptical filters can be obtained using Matlab. The generalized transfer function of an $L^{th}$-order NTF is given by:

$$NTF_{gen}(z) = \frac{\prod_{k=1}^{L/2}\left(1 - 2b_k z^{-1} + z^{-2}\right)}{1 + a_1 z^{-1} + \cdots + a_{L-1} z^{-L+1} + z^{-L}} \tag{26}$$

An Output Feedback (OF) topology is chosen to explain the design methodology since its NTF and STF have already been derived as already presented in (7). The block diagram given in Figure 23 is modelled in Matlab/Simulink where an Infinite Impulse Response (IIR) filter block is used to represent the loop-filter. The system level design in Matlab/Simulink helps practitioners to improve their understanding of the operation of VBP Σ-Δ modulators for different loop-filters, centre frequencies and bandwidths.

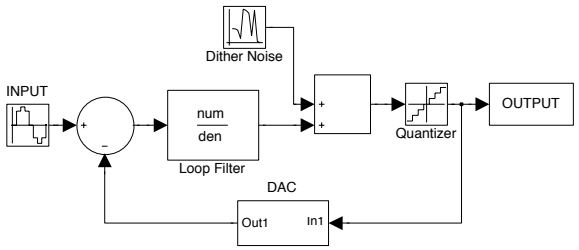



**Figure 23: The OF Σ-Δ Modulator Block Diagram**

After building the OF Σ-Δ modulator block diagram in Figure 23, designers can calculate the loop-filter's numerator and denominator coefficients in MATLAB without building the loop-filter topology. Therefore, the final loop-filter and Σ-Δ modulator coefficients may need to be adjusted following extensive simulations to meet the required specifications including the SNR, DR, stability and tonality. It should be noted that regarding the NTF filter type, the following functions can be employed, i.e., butter for Butterworth filters, cheby1 for Chebyshev filters, cheby2 for Inverse-Chebyshev filters and ellip for Elliptical filters.

## 3.3 VBP Σ-Δ Modulator Topologies

The second step in the design of VBP Σ-Δ modulator is mapping the generalized NTF in (26) to a generalized topology. The choice of the topology does not affect the performance at the behavioural level. From an implementation perspective, however, different topologies that use the same initial NTF may produce slightly different output response and resolutions. This is attributed to the sensitivity of coefficient variation of the Σ-Δ modulator structures. Therefore, this section mainly focuses on the choice of the building blocks: resonator-based or integrator-based.

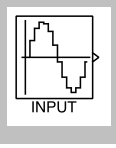
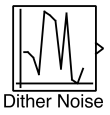
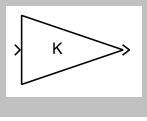
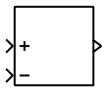
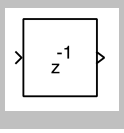
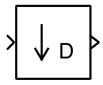
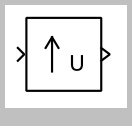
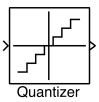
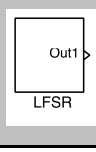
### 3.3.1 Chain of Integrators with FeedBack and FeedForward Coefficients (CI-FBFF)

As implied from its name, the CI-FBFF topology utilizes integrators as its main building blocks. Integrators process the variations of the input signal as they accumulate and low-pass filter the in-coming signal. Therefore, integrators are the key building blocks of Σ-Δ modulators. The block diagrams of delayless and delayed discrete-time integrators are boxed and displayed in Figure 24 in which the second-order SP CI-FBFF topology is shown. This topology is also used to explain the node-equation technique and its 2-path TI counterpart equations are calculated in (35)- (48). So internal nodes are named as n1, n2, n3, n4 and n5.

The behavioural-level drawings in the thesis are composed using the Matlab Simulink R2010b. For readers who are not familiar with the Simulink, Table 2 is given before the SP CI-FBFF topology explaining the building blocks. It must be noted that, the Simulink drawings are converted to EPS (Encapsulated PostScript) format using the "print" function of Matlab. Therefore, the converted EPS files do not owe the same precision for all topologies.

Moreover, in Appendix A, Appendix B, Appendix C and Appendix D the sizes of the building blocks may differ from one topology to another to fit individual topologies into a single page.

**Table 2 : Building Blocks of Simulink**

| Building Block | Function |
|---|---|
|  | The sampled single-sinusoidal input signal. |
|  | The white noise source used as the dither noise. |
|  | Gain block used to apply the feedback and feedforward multiplications. |
|  | Adder block. |
|  | Delayer. |
|  | Downsampler. |
|  | Upsampler. |
|  | Quantizer. |
|  | Linear feedback shift register built by the author using Simulink. |

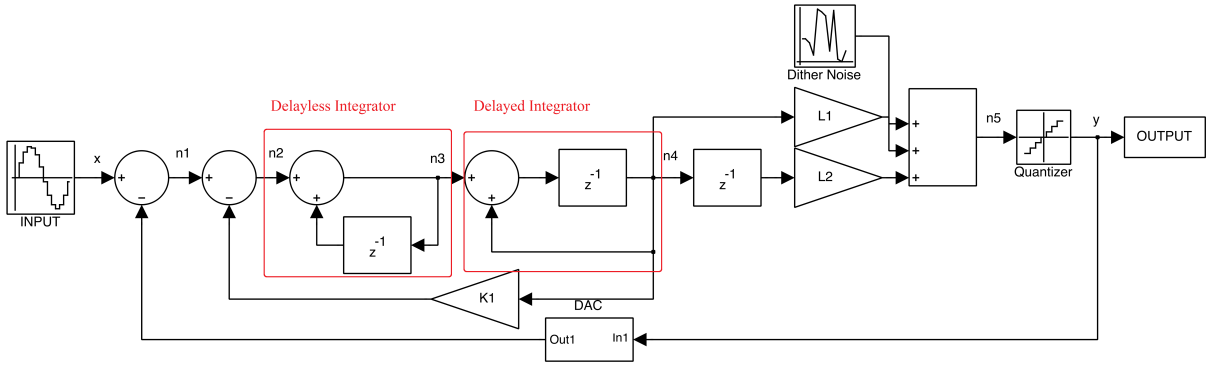



**Figure 24: 2nd-order SP CI-FBFF Topology**

The topology basically determines the numerator of the NTF by feedback coefficients and the denominator of the NTF by feedforward coefficients given in (27). Therefore, without even considering the non-idealities, it can be asserted that non-idealities of the feedback coefficients will degrade the SNR and DR performance. This is due to the fact that the in-band quantization noise is determined by the numerator of the NTF. On the other hand, the feedforward coefficients are calculated using the denominator coefficients of the NTF. In other words, the pole locations are affected by the feedforward coefficients. So the feedforward coefficients will affect the SNR, DR and stability performance.

$$NTF_{2^{nd}CI}(z) = \frac{1+(K_1-2)z^{-1}+z^{-2}}{1+(L_1+(K_1-2))z^{-1}+(L_2+1)z^{-2}} \tag{27}$$

In addition, the feedforward and feedback multiplications of each node are summed up together at the same adder. This in return may cause excessive signal accumulation leading to an unstable modulator. It can be foreseen that this topology gives a low dynamic range.

### 3.3.2 The TI Technique

One of the major issues of Σ-Δ modulation is the bandwidth restriction, less than a few MHz, arising from the oversampling requirements. Using higher-order NTFs may relax the oversampling demands as the required SNR is obtained by a steeper noise-shaping. However, higher-order NTFs drastically suffer from stability problems and low DRs [81]. Herein parallel working Σ-Δ modulators offer an appropriate solution to increase the conversion

bandwidth without sacrificing the performance. Yet the fundamental drawback of parallelism is the increased hardware.

There are various parallel structures in the open literature that extend the conversion bandwidth using different approaches. For instance, the frequency-band decomposition technique involves partitioning the conversion bandwidth into sub-bands each being processed by different channels at the same time [82]. This technique is challenging due to the design complexity since each channel requires different NTFs and therefore different structures [83]. Eventually larger conversion bandwidths or lower speed requirements can be accomplished at the expense of design complexity.

Another parallel Σ-Δ modulation technique is modulated-based architectures in which the input and output sequences are modulated by external signals [83]. Their circuitry and overall performance differ depending on the modulation sequence. A popular parallel structure is the Time-Interleaved Σ-Δ modulator, as it provides efficient and easy conversion from a SP Σ-Δ modulator. The input signal samples are distributed over the parallel, cross-connected channels by means of a commutator hence each sample is processed by different channels. The output is then combined in a sorted manner to obtain a single output sequence. Basically the input and the output signals are modulated by an identity matrix.

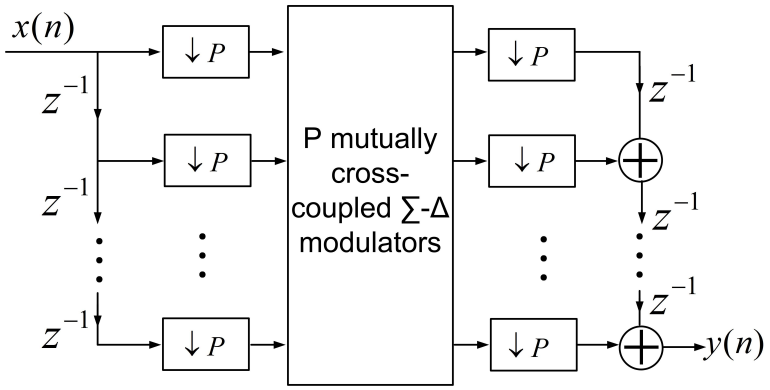



**Figure 25: Block Diagram of the TI Topology**

As depicted in Figure 25, the TI approach employs P mutually cross-coupled Σ-Δ modulators, each operating at a sampling frequency of $f_s$, which results in an equivalent sampling rate of $Pf_s$ [65]. Therefore, the TI Σ-Δ modulators also operate as multi-rate signal processors.

The design procedure of a TI Σ-Δ modulator commences with the design of a SP structure. Afterwards using one of the methods in the literature, the SP Σ-Δ modulator is converted to its TI counterpart. Mainly, there are two reported methods that enable the conversion of a SP Σ-Δ modulator to its P-path TI counterpart. The first method involves mathematically developing the polyphase decomposition elements of the loop-filter and mapping the resulting matrix to the TI topology [65]. It is clear that this method is challenging due to the cumbersome mathematical operations. Furthermore, for a VBP Σ-Δ modulator with the given NTF in (26), these mathematical operations are much more complex.

The second method, which will be further developed in this thesis, is mathematically less intensive and involves writing node equations of the SP Σ-Δ modulator topology in the time domain [20]. The fundamental idea underlying the node equation conversion is to share the samples with the subsequent and/or adjacent channel for the next time interval if needed. This in return results in fewer components when compared to the polyphase decomposition technique. In addition, it is an efficient and easy technique to apply. Another elegant feature of the node equation method is that it allows designers to build generalized topologies, as the coefficient values in the SP node-equations do not affect the resulting TI topology. However, the polyphase decomposition differs depending on the NTF coefficients.

### 3.3.3 Downsampler

The downsampler and the upsampler are the two vital building blocks of the TI topologies as they multiply the incoming signal by an identity matrix. The downsampling operation, generally known as decimation, is defined as reducing the sampling rate of a discrete-signal by a certain downsampling ratio.

In Figure 28, the time-domain behaviour of a 2-path downnsampler is shown. In Figure 26 the block diagram of a D-factor downsampler is depicted and in (29) the mathematical model of a downconverter is given where D is the dowsampling ratio.

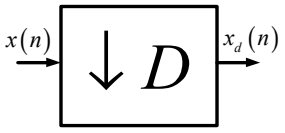



**Figure 26: Downsampler Block Diagram**

$$x_d(n) = x[nD] \tag{28}$$

$$X_d\left(e^{j\omega}\right) = \frac{1}{D}\sum_{i=0}^{D-1} X\left(e^{j\left(\frac{\omega}{D}-\frac{2\pi}{D}\right)}\right) \tag{29}$$

If the z-transform is applied;

$$X_d(z) = \frac{1}{D}\sum_{i=0}^{D-1} X\left(z^{1/D}W^i\right) \tag{30}$$

where;

$$W^i = e^{-\left(2\pi/D\right)i} \tag{31}$$

Downsampling produces D-1 shifted copies of the stretched input signal. Stretching occurs because of $z^{1/D}$ and shifting occurs because of $W^i$. These images are cancelled by the upsampler within the same topology as long as they are band-limited to $\pi/D$.

### 3.3.4 Upsampler

The upsampling operation, generally known as interpolation, is defined as increasing the sampling rate of a discrete-signal by an upsampling ratio. The block diagram of an upsampler is given in Figure 27 and its mathematical model is provided in (34) where U is the upsampling ratio.

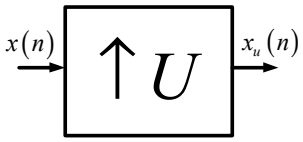



**Figure 27: Upsampler Block Diagram**

$$x_u(n) = x[\frac{n}{U}] \tag{32}$$

$$X_u\left(e^{j\omega}\right) = X\left(e^{j\omega U}\right) \tag{33}$$

If the z-transform is applied;

$$X_u(z) = X\left(z^U\right) \tag{34}$$

Upsampling creates U-fold compressed images of the input signal. These images are caused by the sampled-nature of the input signal.

### 3.3.5 Node Equation Method

The node-equation method was firstly presented in [20] in which a step-by-step methodology is developed for the conversion of LP SP Σ-Δ modulators to their P-path TI counterparts. In this thesis, the node equation method is further extended to VBP Σ-Δ modulators. Furthermore, using this technique 2-path and 4-path D/A TI VBP Σ-Δ modulators are implemented on VHDL validating the node-equation method and the resulting circuitry's performance. Assuming an already designed and examined SP topology such as Figure 24, the node equation method is applied as follows.

**Step 1:** Each node is named as seen in Figure 24 and the equations of these nodes are written in the time domain as in (35). Note that the DAC in the feedback loop is assumed to be ideal, in other words its gain is equal to unity and can be regarded as short circuited when the node equations are written. In addition, the non-ideal behaviour of the quantizer is modelled by the $Q(n)$ function whereas the dither noise is represented by $d(n)$.

$$\begin{aligned}
n_1(n) &= x(n) - y(n) \\
n_2(n) &= n_1(n) - K_1 n_4(n) \\
n_3(n) &= n_2(n) + n_3(n-1) \\
n_4(n) &= n_3(n-1) + n_4(n-1) \\
n_5(n) &= L_1 n_4(n) + L_2 n_4(n-1) + d(n) \\
y(n) &= Q\left(n_5(n)\right)
\end{aligned} \tag{35}$$

**Step 2:** This step involves modelling the behaviour of the downsampling in the time domain. A downsampler is basically a p-state commutator. For a downsampling level of two, the downsampler is a two-state commutator that distributes the input signal samples over the time interleaving paths as seen in Figure 28. It is advisable to make a P-path TI signal distribution diagram before moving to the third step.

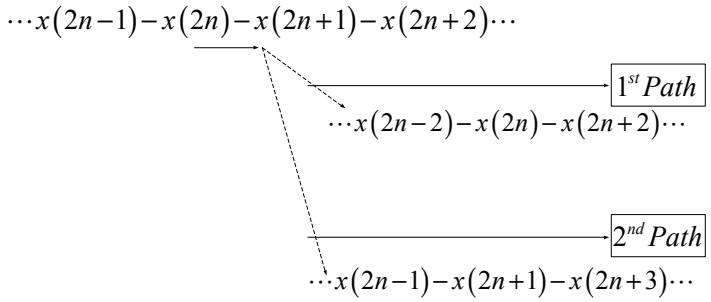



**Figure 28: 2-level Downsampler Behavioural Model**

**Step 3:** The third step is to label each node in accordance with the desired path number of the TI topology. Since a 2-path TI topology is intended, the nodes are labelled as in (36).

$$\begin{aligned}
&x(2n)=x_1(n),\ x(2n-1)=x_2(n)\\
&n_1(2n)=n_{1,1}(n),\ n_1(2n-1)=n_{1,2}(n)\\
&n_2(2n)=n_{2,1}(n),\ n_2(2n-1)=n_{2,2}(n)\\
&n_3(2n)=n_{3,1}(n),\ n_3(2n-1)=n_{3,2}(n)\\
&n_4(2n)=n_{4,1}(n),\ n_4(2n-1)=n_{4,2}(n)\\
&n_5(2n)=n_{5,1}(n),\ n_5(2n-1)=n_{5,2}(n)\\
&y(2n)=y_1(n),\ y(2n-1)=y_2(n)
\end{aligned} \tag{36}$$

**Step 4:** The final step is to convert each equation individually to its corresponding path-node equations calculated in (37)-(48).

$$\begin{aligned}
&n_1(2n)=x(2n)-y(2n)\\
&n_{1,1}(n)=x_1(n)-y_1(n)
\end{aligned} \tag{37}$$

$$\begin{aligned}
&n_1(2n-1)=x(2n-1)-y(2n-1)\\
&n_{1,2}(n)=x_2(n)-y_2(n)
\end{aligned} \tag{38}$$

$$n_2(2n) = n_1(2n) - K_1 n_4(2n)$$
$$n_{2,1}(n) = n_{1,1}(n) - K_1 n_{4,1}(n) \tag{39}$$

$$n_2(2n-1) = n_1(2n-1) - K_1 n_4(2n-1)$$
$$n_{2,2}(n) = n_{1,2}(n) - K_1 n_{4,2}(n) \tag{40}$$

$$n_3(2n) = n_2(2n) + n_3(2n-1)$$
$$n_{3,1}(n) = n_{2,1}(n) + n_{3,2}(n) \tag{41}$$

$$n_3(2n-1) = n_2(2n-1) + n_3(2n-2)$$
$$n_{3,2}(n) = n_{2,2}(n) + n_{3,1}(n-1) \tag{42}$$

$$n_4(2n) = n_3(2n-1) + n_4(2n-1)$$
$$n_{4,1}(n) = n_{3,2}(n) + n_{4,2}(n) \tag{43}$$

$$n_4(2n-1) = n_3(2n-2) + n_4(2n-2)$$
$$n_{4,2}(n) = n_{3,1}(n-1) + n_{4,1}(n-1) \tag{44}$$

$$n_5(2n) = L_1 n_4(2n) + L_2 n_4(2n-1) + d(2n)$$
$$n_{5,1}(n) = L_1 n_{4,1}(n) + L_2 n_{4,2}(n) + d(n) \tag{45}$$

$$n_5(2n-1) = L_1 n_4(2n-1) + L_2 n_4(2n-2) + d(2n-1)$$
$$n_{5,2}(n) = L_1 n_{4,2}(n) + L_2 n_{4,1}(n-1) + d(n) \tag{46}$$

$$y(2n) = Q(n_5(2n))$$
$$y_1(n) = Q(n_{5,1}(n)) \tag{47}$$

$$y(2n-1) = Q(n_5(2n-1))$$
$$y_2(n) = Q(n_{5,2}(n)) \tag{48}$$

Following the conversion of the equations, the corresponding TI Σ-Δ modulator topology is constructed as demonstrated in Figure 29. Moreover, the 4-path counterpart is shown in Figure 30.

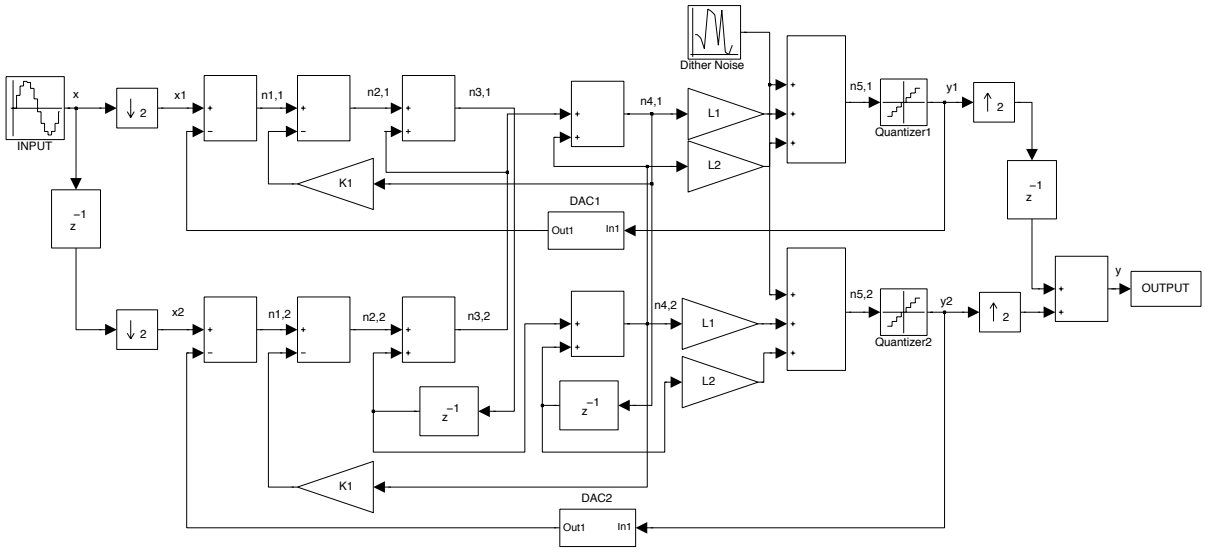



**Figure 29: 2nd-order 2-path CI-FBFF Topology**

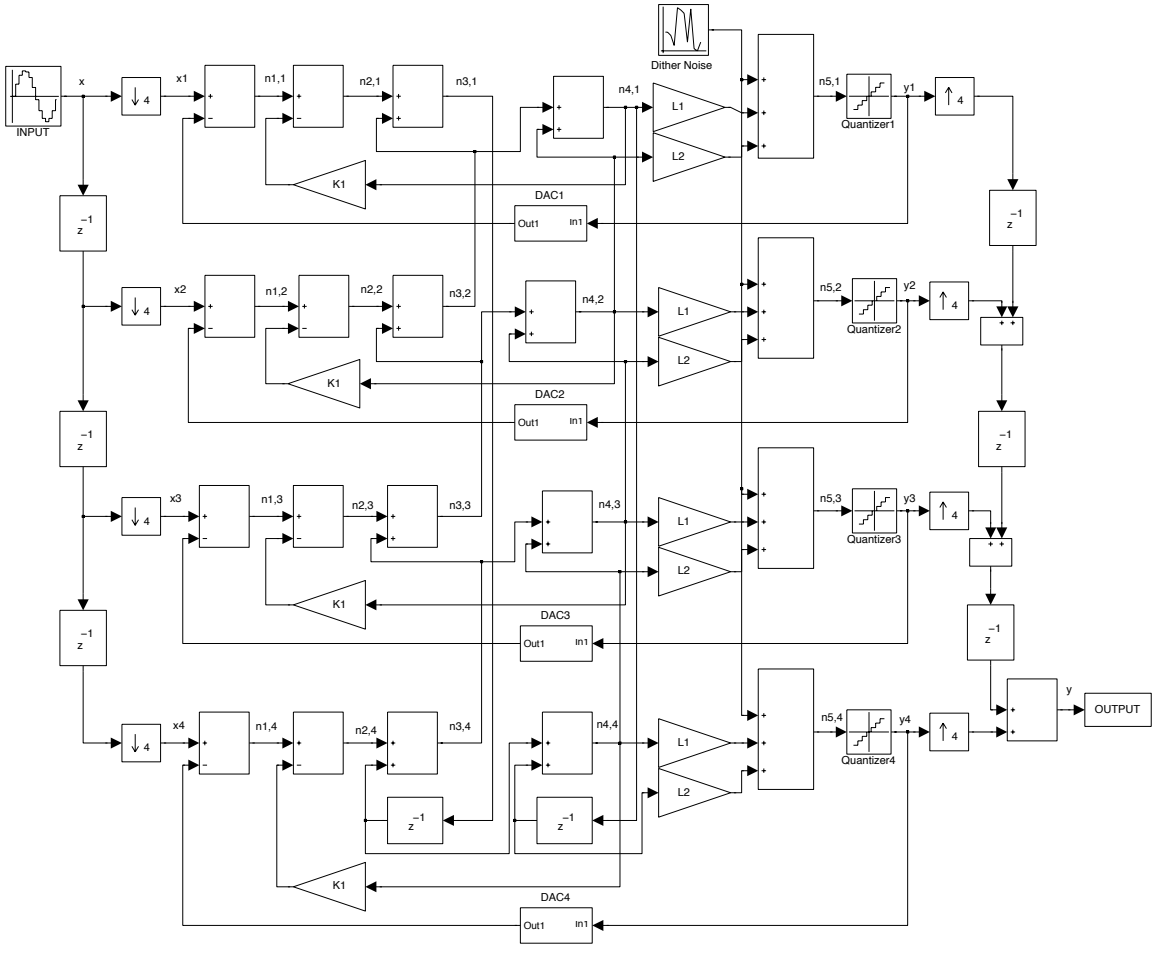



**Figure 30: 2nd-order 4-path CI-FBFF Topology**

### 3.3.6 Design Technique to Build Up Generalize TI VBP Σ–Δ Modulators

A step-by-step design methodology of TI VBP Σ–Δ modulators is given below:

1. Build an SP Σ–Δ modulator with an IIR block in Simulink to simulate the NTF given in (26).
2. Choose appropriate coefficients for the generalized NTF to implement Butterworth, Chebyshev, Inverse Chebyshev or Elliptical filters.
3. Analyse the SP Σ-Δ modulator topology in terms of its stability, resolution and dynamic range. If the required performance metrics are not met go to 2.
4. Map the chosen NTF to an SP Σ-Δ modulator topology.
5. Build the TI counterpart of the SP Σ–Δ modulator topology using the node-equation method.
6. Analyse the TI Σ–Δ modulator in terms of its stability, resolution and dynamic range.

### 3.3.7 Chain of Resonators with Feedforward and Local Resonator FeedBack Coefficients (CR-RFB)

This second topology is constructed using resonator blocks as shown in the dashed square of Figure 31 in which the $2^{nd}$-order SP CR-RFB topology is illustrated. Earlier in Section 2.4, a resonator structure was given in Figure 13, where two cascaded integrator blocks were utilized. This conventional topology has been employed in many applications due to its well-known structure and non-ideal model [84-86]. However, in [87] and [88], single-opamp SC resonators are proposed where double-sampling clocking is required. Single-opamp resonator blocks are gaining popularity as they lower the power dissipation and hardware of the overall circuitry. Moreover, in [89], a double-sampling SC resonator is proposed whose numerator is immune to circuit non-idealities, hence the resonant frequency and the Q-factor are not affected by the capacitance values.

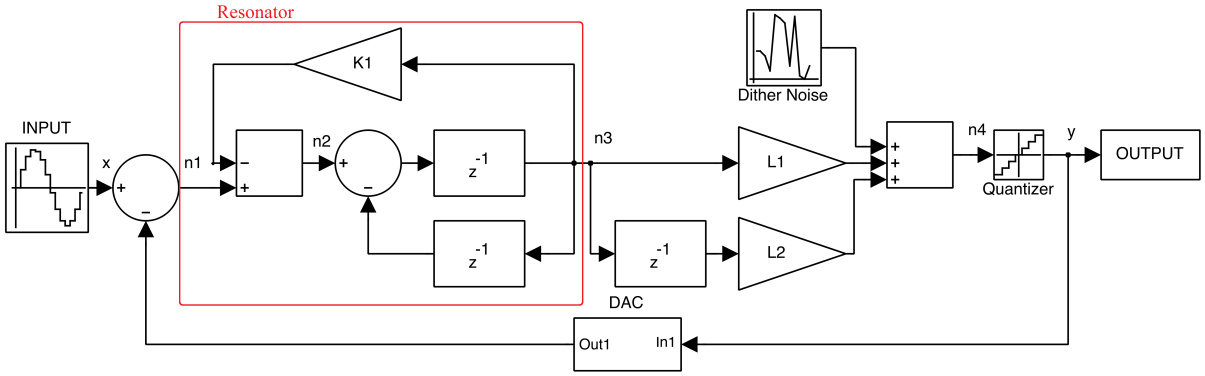



**Figure 31: 2nd-order SP CR-RFB Topology**

The corresponding symbolic NTF of the 2nd-order SP CR-RFB topology is given in (49). Once again the feedback coefficients determine the zeros of the NTF whereas the feedforward coefficients determine the poles.

$$NTF_{2^{nd}CR}(z) = \frac{1+(K_1)z^{-1}+z^{-2}}{1+(L_1+K_1)z^{-1}+(L_2+1)z^{-2}} \tag{49}$$

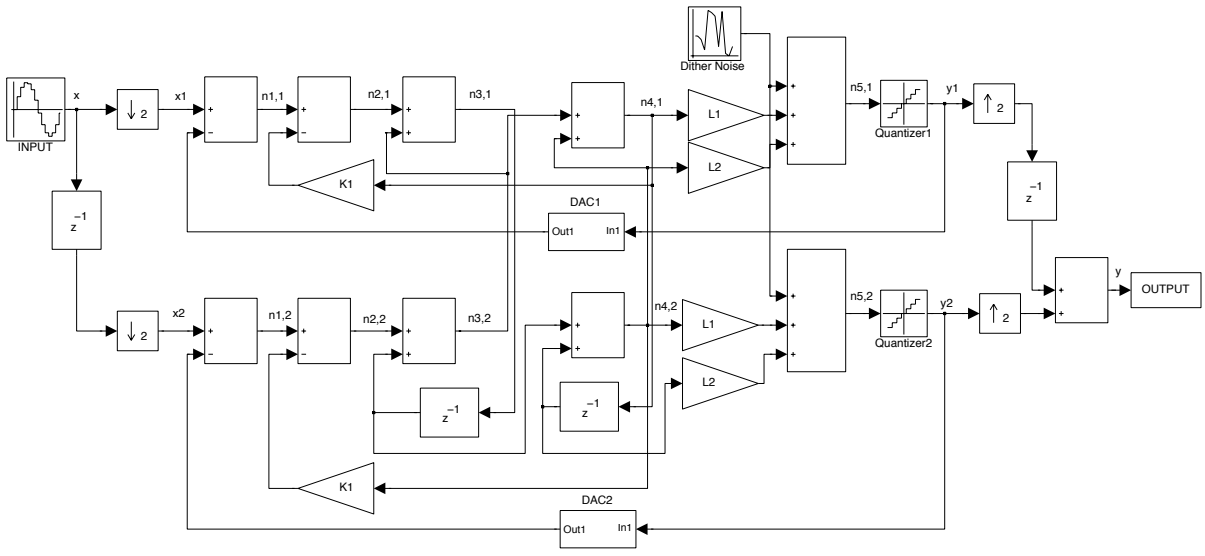



**Figure 32: 2nd-order 2-path CR-RFB Topology**

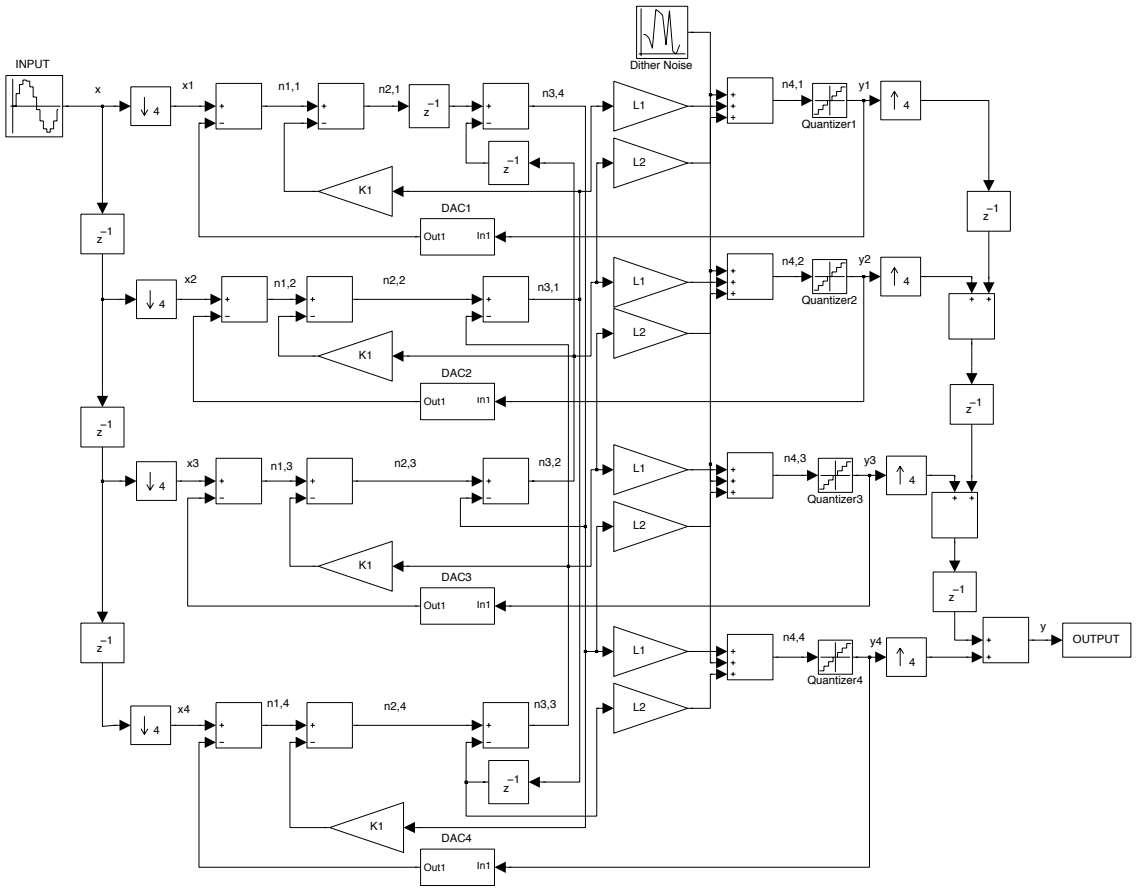



**Figure 33: 2nd-order 4-path CR-RFB Topology**

## 3.4 Hardware Complexity of the A/D VBP Σ-Δ Modulators

Although the A/D VBP Σ-Δ modulators are not implemented in this thesis it worth pointing out the hardware complexity of the resulting topologies. Regardless of the topology type, the TI topologies utilizes $P$x$N_{ad}$ adders and $P$x$N_{mul}$ multipliers where $P$ is the TI path number, $N_{ad}$ and $N_{mul}$ are the numbers of the adders and multipliers used to build the SP counterpart of the TI topology. Hence the relaxed sampling frequency or the higher OSR ratio is obtained at the expense of increased hardware. However, the SP and TI topologies strictly differ from each other in terms of their building blocks.

As mentioned earlier, the node-equation method shares the samples of the internal nodes between the adjacent and/or subsequent channels. Therefore, the resonators and integrators of the SP topology cannot be observed for the TI topologies. If Figure 29, Figure 30, Figure 32

and Figure 33 are investigated it can be seen that, the resonator and integrators are distributed over the channels. So, the main building blocks of the TI topologies are delayless and/or delayed adders and multipliers.

In this sense, if the TI topologies are implemented using voltage-mode circuits, designers will end using $P\text{x}N_{ad}$ adders and $P\text{x}N_{mul}$ multipliers. However, if the TI topologies are implemented using current-mode circuits, designer can save the $P\text{x}N_{ad}$ adders, because adding occurs through the internal nodes of the current-mode circuits. Consequently current mode TI topologies will use $P\text{x}N_{mul}$ multipliers only. Once again, this advantage can be benefited for the TI topologies built using the node-equation method. Hence their main building blocks are delayless and/or delayed adders and multipliers.

Finally, if the CR-RFB and the CI-FBFF topologies are compared, they both utilize *LxP* feedforward coefficients where *L* is the order of the modulator and *P* is the TI path number. On the other hand, the CR-RFB topology uses $P\text{x}L/2-1$ fewer feedback coefficients with respect to CI-FBFF topology. Obviously, for multi-path TI topologies it is wise to choose the CR-RFB topology in order to save multipliers and adders. Hence each reduction in the feedback coefficients equals to the reduction of one adder and one multiplier. Consequently, the CR-RFB topology can be implemented saving $PxL/2-1$ adders and $PxL/2-1$ multipliers.

### 3.5 Behavioural Level Simulations of the CI-FBFF Topology

The behavioural level-simulations are explained in this section for two reasons; firstly it is intended not to disturb the natural flow of the thesis, as the node equation technique needs to be well covered before getting into the analysis of the designed modulators. Secondly, this section also involves the comparison of the designed SP and TI CI-FBFF and SP and TI CR-RFB topologies for different orders.

$2^{nd}$-, $4^{th}$-, $6^{th}$-, $8^{th}$-order SP, 2-path, 4-path topologies of CI-FBFF and CR-RFB are built and the resulting structures including their symbolic NTFs are given in Appendix A and Appendix B.

**Simulation Methodology:** The behavioural level simulations of the SP CI-FBFF topologies of any order starts with measuring its SNR for different centre frequencies. Because the SNR plots involve the DR and output plots within the code, the output plot can be observed for discrete input amplitude values for each iteration. If any unstable output is noticed, the pole and zero locations of the designed filter type and resulting feedback and feedforward coefficients are noted to determine the hazardous region. If not, iterative simulations sweep the centre frequency for a fixed bandwidth until an unstable coefficient set is determined.

Afterwards, for each filtering type the safe centre frequencies are fixed and the bandwidth is swept to determine the bandwidth boundaries for each discrete centre frequency. These preliminary and time-consuming simulations are applied to each designed topology mentioned in the anterior sections to predict the stability of each topology.

After the stability, SNR and DR are provided, the designed topologies are compared and discussed in Section 3.9. Moreover the performance of Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical are compared and examined in Section 3.9. Finally and more importantly, the non-idealities are modelled in each designed topology and the resulting performances are given in Section 3.10.

**SNR Code:** The major concern in the SNR code is to correctly select the Fast Fourier Transform (FFT) samples, windowing function and overlapping number. The FFT conversion inevitably suffers from signal energy leakage due to the aperiodic nature of the Σ-Δ output data. To reduce this leakage, a Hanning window is selected as it provides good frequency resolution whilst keeping the signal amplitude and spectral leakage under control [90]. However, Hanning window is not sufficient to depict all the harmonics and other tones in the frequency band. Therefore, the overlapping technique is utilized to minimize the leakage. The idea of overlapping is to apply overlapping window frames to the output in order to reduce the loss of information as seen in Figure 34.

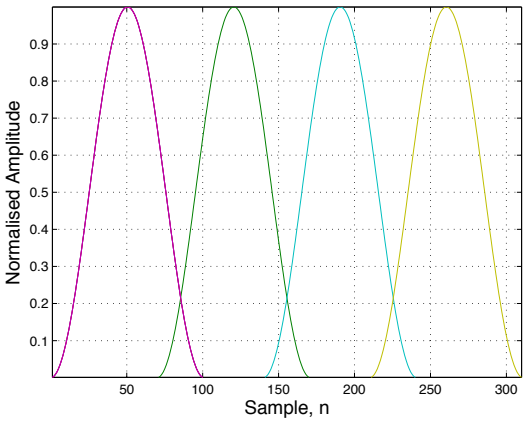



**Figure 34: Windowing and Overlapping**

Since windowing and overlapping are applied, the FFT size only needs to cover the period of the processing data to ensure good resolution. For this, as long as the periodicity of the output data is covered, the length of the FFT just determines the resolution. The wider the FFT window is chosen, the better resolution is provided in the frequency domain and the poorer resolution is obtained in the time-domain. In this study, an FFT window size of $2^{20}$ is chosen with an overlapping 8 windows.

Finally, oversampling is achieved by simply filtering the output data using the FFT sample number and OSR. The signal-band is calculated as in (50) where $N_{FFT}$ is the FFT sample number and $P_{TI}$ is the time-interleaving path number.

$$BW_{signal} = \frac{N_{FFT}/2}{P_{TI} \times 2 \times OSR} \tag{50}$$

The negative frequency is discarded for the calculations and therefore $N_{FFT}$ is divided by 2. Moreover, to accomplish accurate resolution for the TI topologies, the signal bandwidth is narrowed, i.e., the bin size is reduced for the ease of calculation. As a result, the OSR is increased.

## 3.6 Analysis of the Behavioural-Level Topologies

In Figure 35 - Figure 38, the output plots of discrete-time CI-FBFF and CR-RFB are given when the same NTF is applied to both topologies. These simulation results validate the node-equation method and resulting TI VBP Σ-Δ modulators' performance. Secondly, they highlight

the characteristics of the topologies. For instance; the tones seen in Figure 36 - Figure 37 need to be investigated. More importantly, in the ideal case the CI-FBFF and CR-RFB topologies are supposed to perform the same NTF function with different feedback and feedforward coefficients. However in Figure 38, it is seen that CR-RFB topology has a deeper notch.

Different VBP Σ-Δ modulators are compared and evaluated at the behavioural level in terms of their order, filter type, topology and path number.

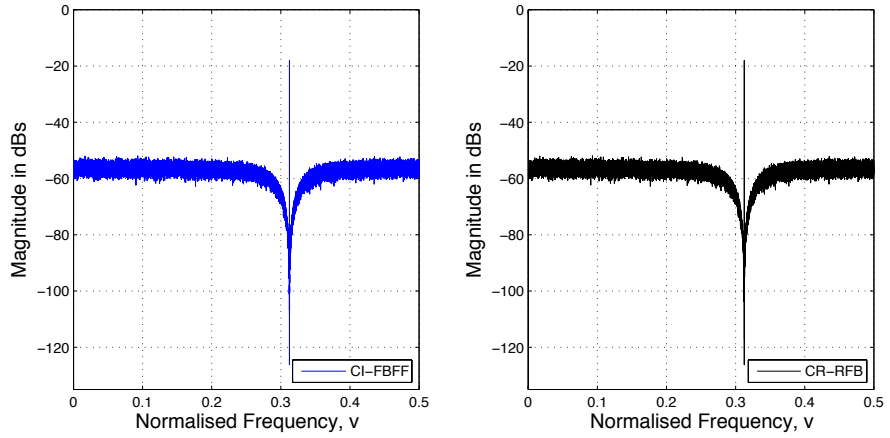



**Figure 35: SP 2nd-order, Butterworth Filtering**

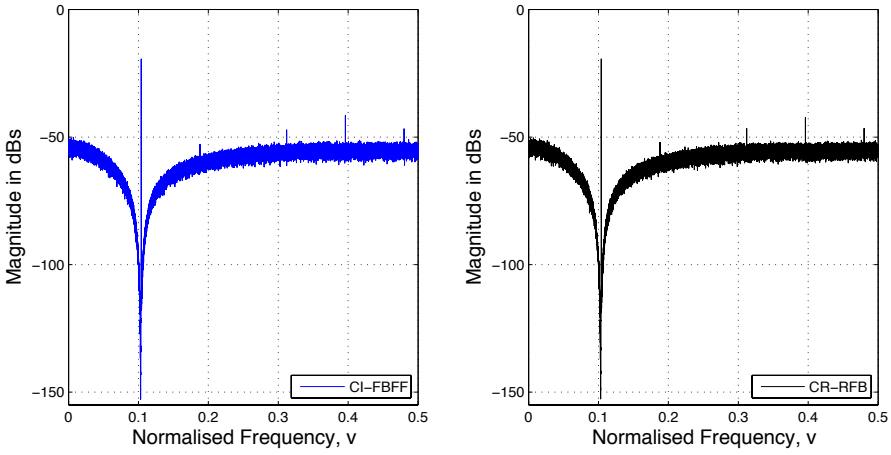



**Figure 36: 2P 4th-order, Chebyshev Filtering**

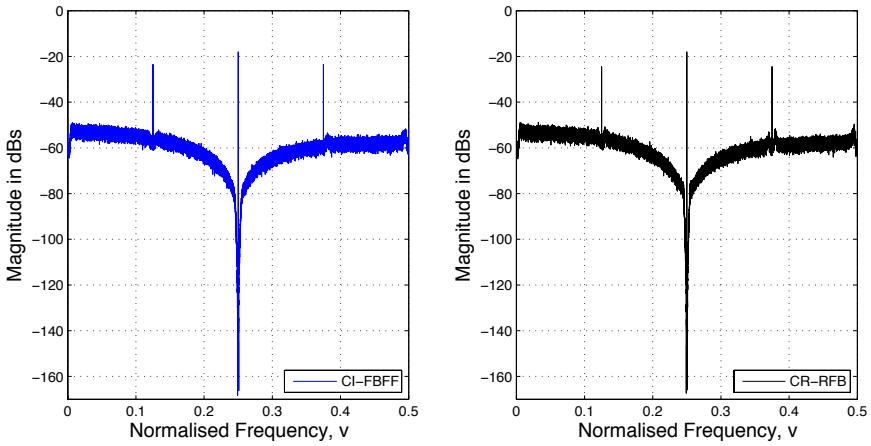



**Figure 37: 4P 6$^{th}$-order, Elliptical Filtering**

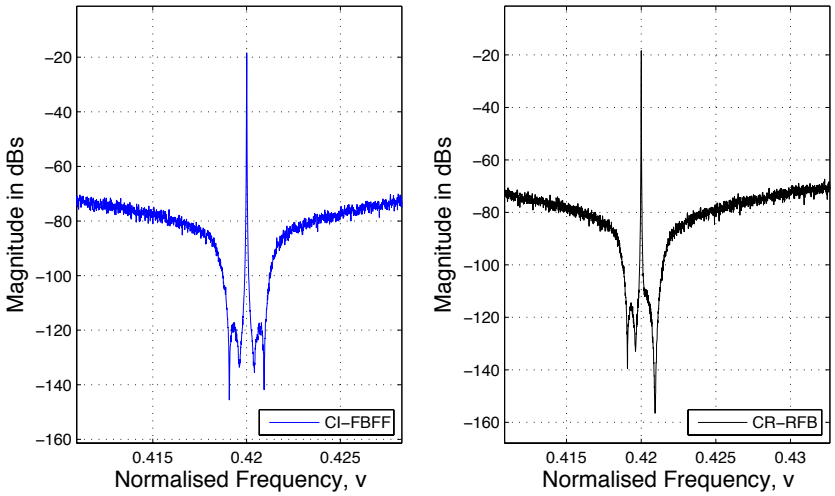



**Figure 38: 4P 8$^{th}$-order, Inverse-Chebyshev Filtering, Zoomed Plot**

## 3.7 Coefficient Comparison

This section will discuss in detail the effects of the coefficients on the output amplitude frequency response of the proposed VBP Σ-Δ modulator topologies. As will be explained and illustrated in the upcoming sections, stability, tonality, DR and SNR degradation are mostly caused by the coefficients' values and coefficient mismatches.

**Feedback Coefficients:** The CR-RFB topology uses $PxL/2$ feedback coefficients whereas the CI-FBFF topology uses $(PxL) - 1$ feedback coefficients where $P$ is the TI path number and $L$ is the order of the modulator. Consequently a P-path $L^{th}$ –order CR-RFB topology saves $PxL/2 - 1$ feedback coefficients with respect to the same path number and order CI-FBFF topology.

Another major difference between the two topologies is that the CR-RFB topology utilizes local feedback coefficients. Thereby the resonant frequency is directly determined by the local feedback coefficients. Hence, for the CR-RFB topology, the local feedback coefficients always fall within the range [-2, 2], which is map to the normalized frequency values of [0, 0.5].

For the CI-FBFF topology, the resonant frequency is determined by multiple feedback coefficients as given in Appendix A. This in turn may cause the feedback coefficients of the CI-FBFF topology to be excessively large up to 900.

Large feedback coefficients of the CI-FBFF topology unfortunately increase the accumulation in each node causing the integrators to be saturated even for small input amplitudes. This in turn, has a deleterious effect on stability and can only be observed in the case of non-ideal integrators.

The resulting values of feedback coefficients versus centre frequency of the Butterworth NTFs are given in Figure 39 - Figure 42.

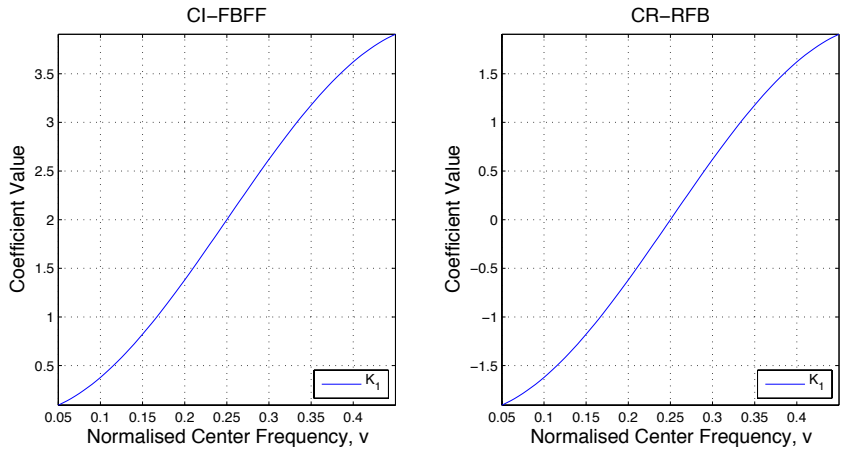



**Figure 39: 2nd-order, Butterworth NTF Feedback Coefficients, BW is fixed to 0.02**

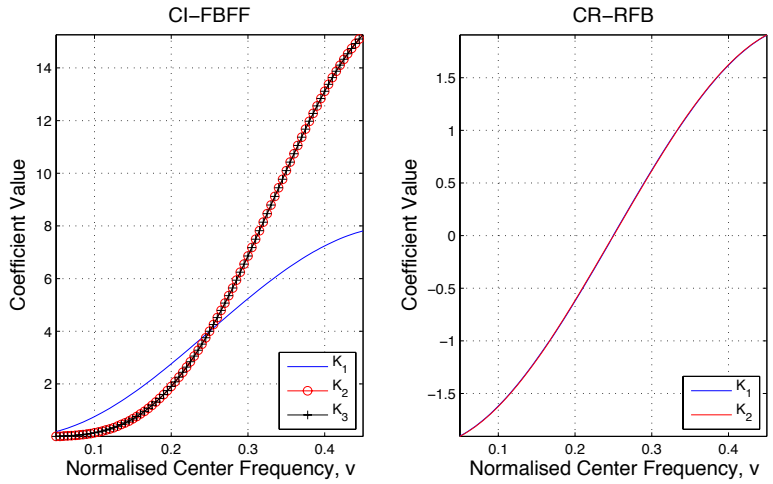



**Figure 40: 4th-order, Butterworth NTF Feedback Coefficients, BW is fixed to 0.02**

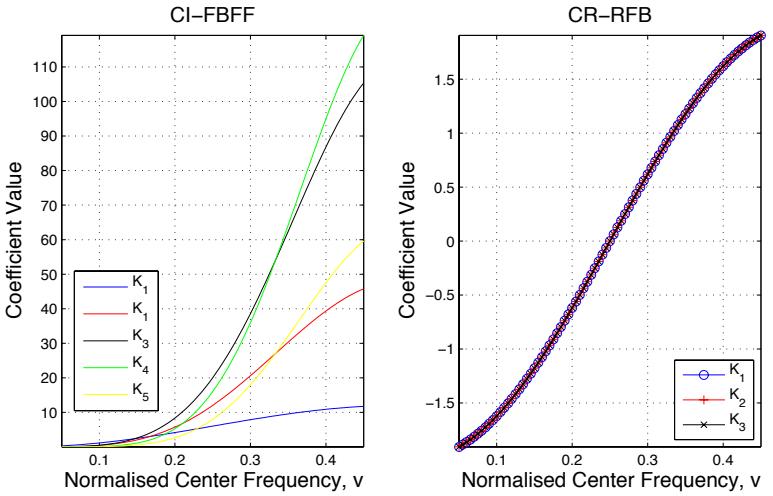



**Figure 41: 6th-order, Butterworth NTF Feedback Coefficients, BW is fixed to 0.02**

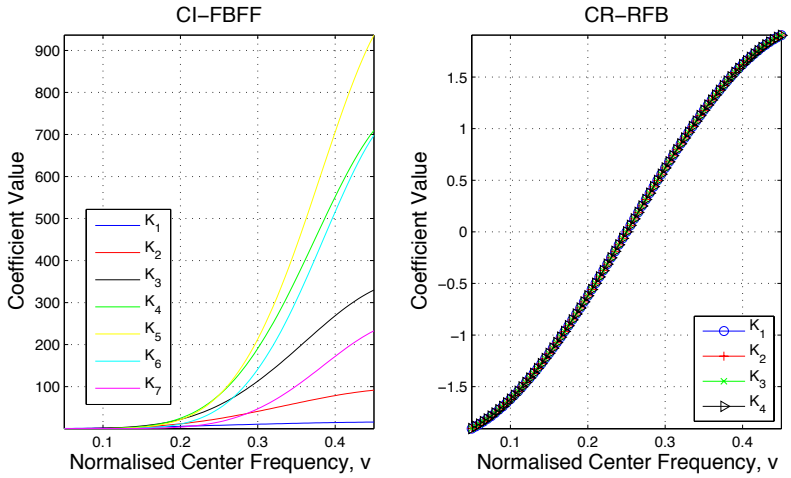



**Figure 42: 8th-order, Butterworth NTF Feedback Coefficients, BW is fixed to 0.02**

The frequency range between [0.25, 0.5] significantly degrades the DR as frequencies larger than $\nu = 0.25$ exponentially increase the feedback coefficients of the CI-FBFF topology. In addition, for higher order NTFs the mid-coefficients get the highest values. This is due to the fact that the cascaded topology forms the NTF numerator from the polynomial function. In other words, Pascal's Triangle polynomials are obtained simply by multiplying binomials of the resonator function of the generalized NTF [91].

As mentioned earlier in this section, the two topologies are supposed to produce the same NTF for the ideal-case behavioural-level simulations. However, it is also shown that some tones and notch dips do not match in the output plots. For the SNR plots depicted in Figure 56 on page 61, the ideal-case behavioural simulations are compatible for the CI-FBFF and CR-RFB topologies.

To give an initial idea on the implementation of large coefficients, it must be kept in mind that the coefficient values of the Switched Capacitor (SC) circuitry are determined by the ratio of the capacitors. In the meantime, the sampling speed is provided by two factors: the on-resistance of the switches and the value of the sampling capacitors. To achieve high-speed operation small capacitors must be utilized. In other words, the capacitor values need to be reduced for an area and/or power efficient implementation. Therefore, the implementation of the large feedback coefficients shown in Figure 41 and Figure 42 is physically impossible despite the fact that the circuit works perfectly well in a simulation environment.

Generally speaking;

- Centre frequencies higher than $\nu = 0.25$ increase the feedback coefficients of the CI-FBFF topology. Whilst the CR-RFB topology's feedback coefficients are always between [-2, 2
    - From the implementation perspective, the CI-FBFF topology cannot perform stable, low-power, low-hardware implementations for orders of 6 and above at the frequency interval [0.25 0.5].
    - The frequency interval [0 0.25] seems feasible for the implementation of CI-FBFF topology.

- The CI-FBFF feedback coefficients get their highest values in the mid-coefficients due to the nature of Pascal Triangle polynomials.
- The NTF type and filter specifications such as the pass-band and stop-band attenuations and bandwidth do not affect both topologies' feedback coefficients' range.

**Feedforward Coefficients:** The feedforward coefficients are determined by the pole locations of the NTF for both topologies. Therefore, the bandwidth, stop-band and pass-band attenuations strictly affect only the feedforward coefficient values. In other words, the feedforward coefficients depend on the NTF filter type.

The denominator of the symbolic NTFs of the CR-RFB topologies is affected by the feedback and the feedforward coefficients as given in Appendix B. The limited interval of the CR-RFB feedback coefficients keeps the feedforward coefficients to closer values of the same order magnitude to the denominator coefficients. However, the feedback coefficients of the CI-FBFF increase the feedforward coefficients especially for orders 6 and above.

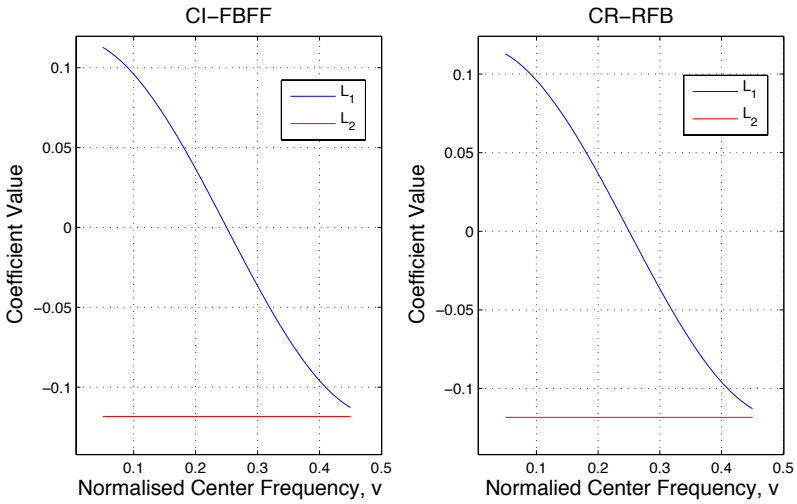



**Figure 43: 2nd-order, Butterworth NTF Feedforward Coefficients, BW is fixed to 0.02**

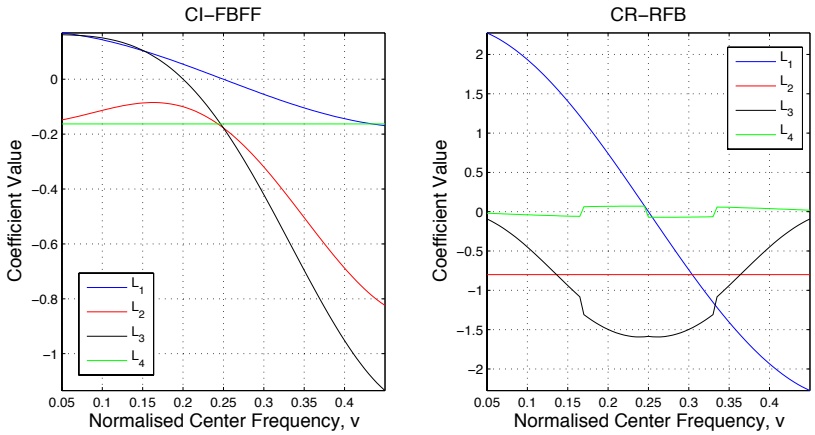



**Figure 44: 4th-order, Butterworth NTF Feedforward Coefficients, BW is fixed to 0.02**

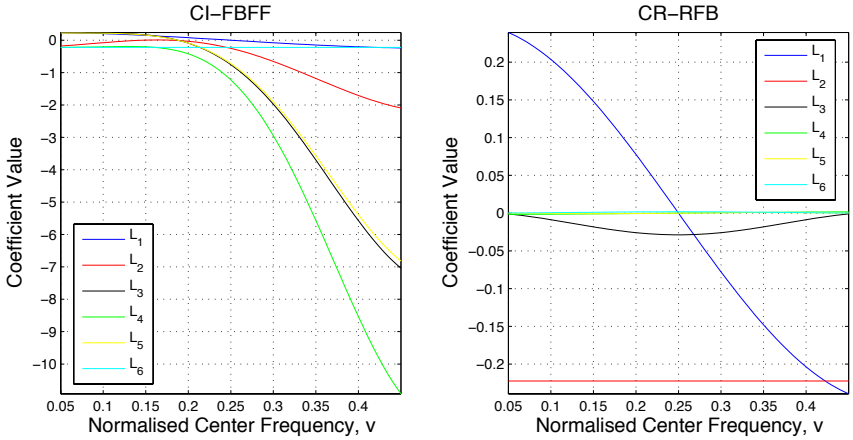



**Figure 45: 6th-order, Butterworth NTF Feedforward Coefficients, BW is fixed to 0.02**

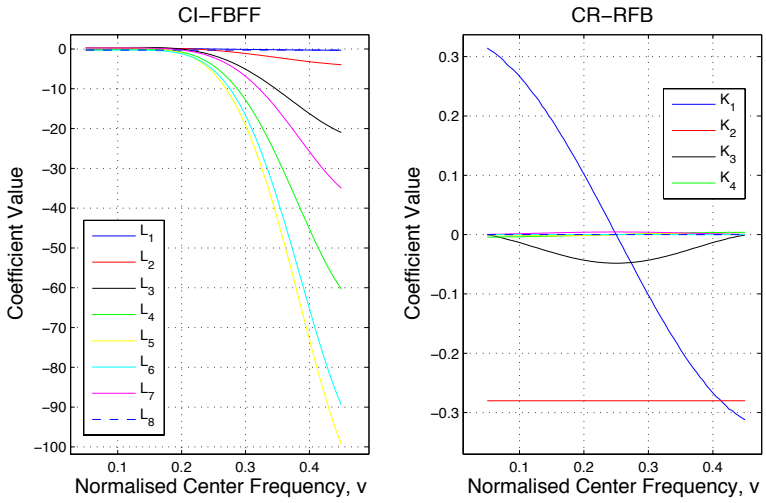



**Figure 46: 8th-order, Butterworth NTF Feedforward Coefficients, BW is fixed to 0.02**

In Figure 47 - Figure 54 the BW sweep plots for the feedforward coefficients of both topologies are given for two distinct centre-frequencies; $\nu = 0.1$ and $\nu = 0.4$ for the Elliptical NTF. These plots are presented to show how the coefficient interval is affected by the centre-frequency when bandwidth is swept. As expected, the CR-RFB feedforward coefficient interval is not affected much (maximum of $\pm 2$) by the bandwidth sweep for these different centre-frequencies.

However, the CI-FBFF feedforward coefficients for orders 6 and 8, exponentially increase for the centre-frequency interval [0.25 0.5]. As mentioned, this is actually caused by the cascaded structure of the CI-FBFF topology. Frequencies over 0.25 increase the feedback coefficients thus the internal node accumulation can be balanced by larger feedforward coefficients. This leads to quantizer overload as the feedforward coefficients are multiplied by the internal signals and added up just before the quantizer. Quantizer overload may cause unstable modulators.

If Figure 51 is compared to Figure 52 and Figure 53 is compared to Figure 54, it is clearly seen that the CI-FBFF topology's feedforward coefficients extensively increase; i.e., up to 1500 for the $6^{th}$-order NTF and up to 350 for the $8^{th}$-order NTF when the centre frequency equals to 0.4. However Figure 47, Figure 48, Figure 49 and Figure 50 show that the centre frequency does not cause significant change in the feedforward coefficient interval for the $2^{nd}$- and $4^{th}$-order CR-RFB and CI-FBFF topologies.

If a multi-frequency and/or multi-band system using the CI-FBFF topology is required, centre-frequency and bandwidth sweep simulations need to be held together. Once again, the CI-FBFF topology is not suitable for VBP Σ-Δ modulators whose input's centre frequencies fall within the interval of [0.25 0.5].

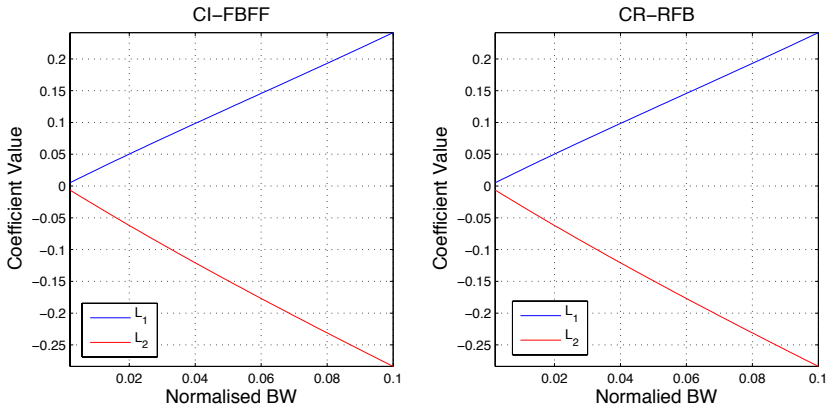



**Figure 47: 2nd-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.1, Pass-Band Attenuation (PBA) = 1dB, Stop-Band Attenuation (SBA) = 80 dB**

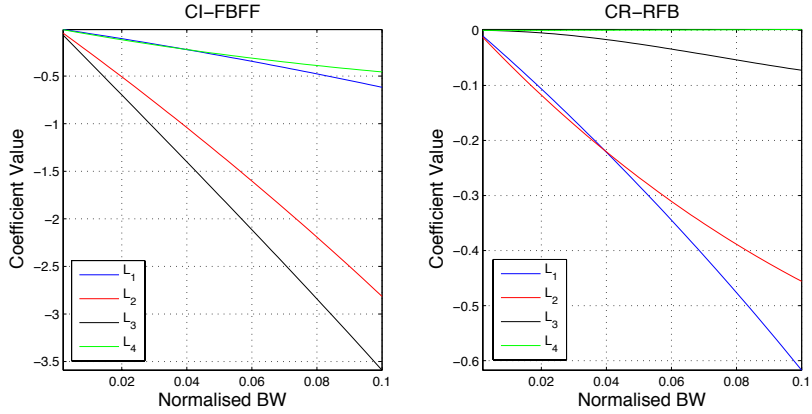



**Figure 48: 2nd-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.4, PBA = 1dB, SBA= 80 dB**

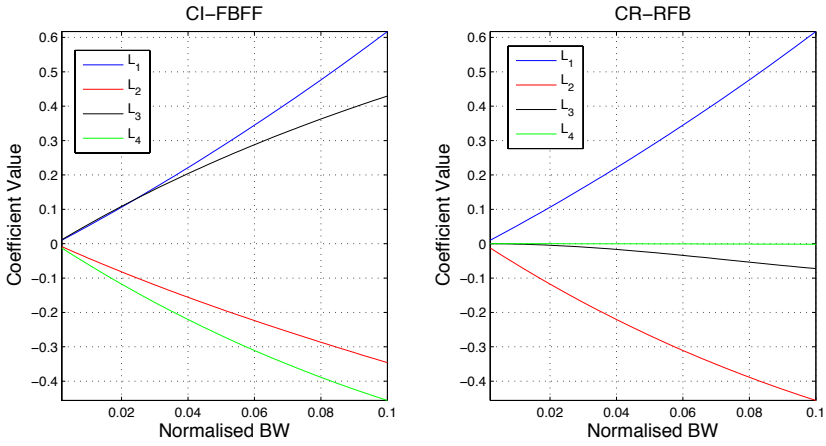



**Figure 49: 4th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.1, PBA = 1dB, SBA = 80 dB**

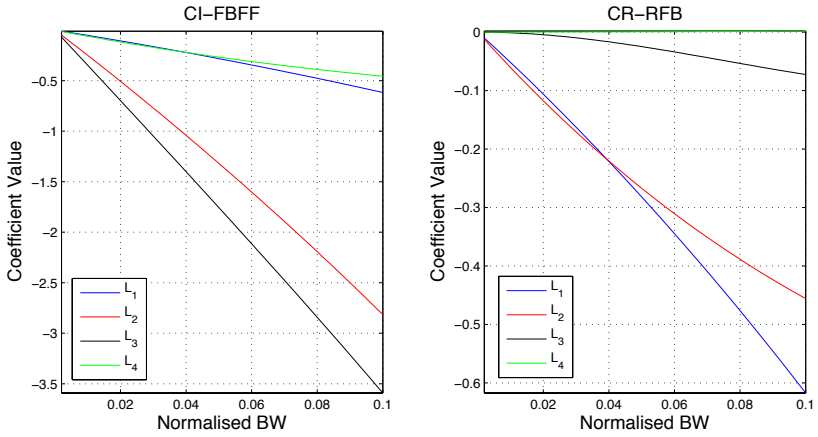



**Figure 50: 4th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.4, Pass-Band Attenuation = 1dB, Stop-Band Attenuation = 80 dB**

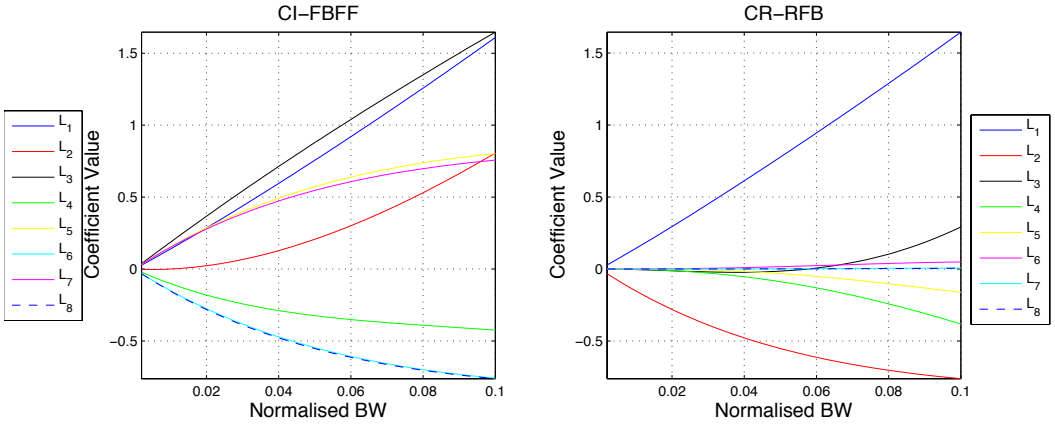



**Figure 51: 6th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.1, PBA = 1dB, SBA = 80 dB**

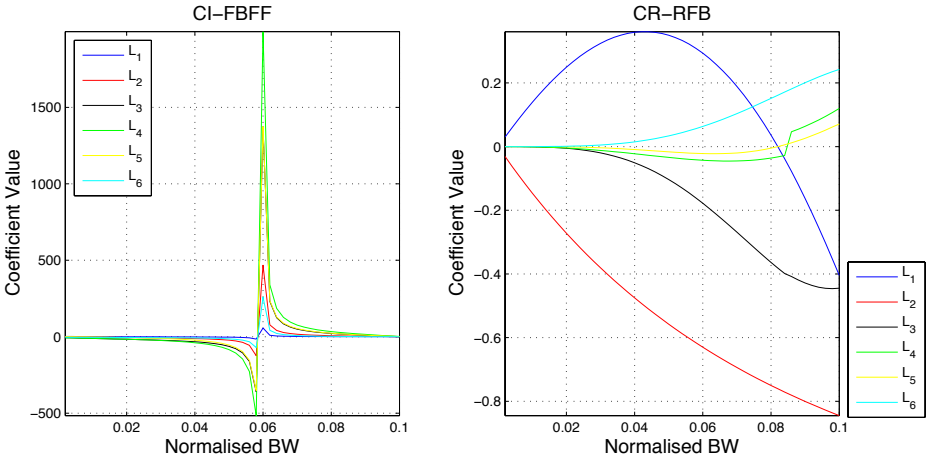



**Figure 52: 6th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.4, PBA = 1dB, SBA= 80 dB**

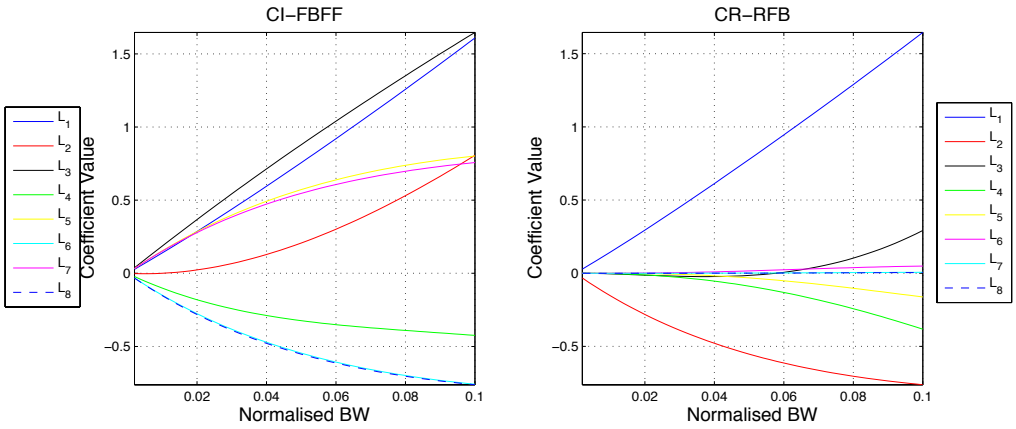



**Figure 53: 8th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.1, PBA = 1dB, SBA = 80 dB**

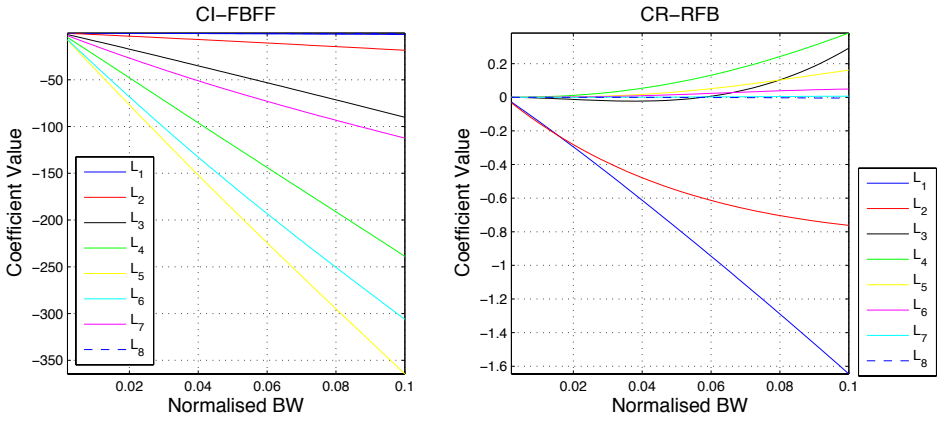



**Figure 54: 8th-order, Elliptical NTF Feedforward Coefficients, Centre Freq. = 0.4, PBA = 1dB, SBA = 80 dB**

Generally speaking;

- Centre frequencies higher than $\nu = 0.25$ increase the feedforward coefficient of the CI-FBFF topology. However these centre frequencies do not have a noticeable effect on the CR-RFB topology's feedforward coefficients.
- The NTF type and filter specifications affect the topologies feedforward coefficients' value
    - The more aggressive the NTF is designed, the smaller the coefficients become.

## 3.8 Filtering Performance

The NTF filter type affects the performance and stability of the VBP Σ-Δ modulators as examined below.

### Butterworth NTFs

Basically a band-stop Butterworth filter has its poles on a semi-circle with a radius of $\nu_{co}$ where $\nu_{co}$ is the cut-off frequency. Butterworth filters provide maximally flat out-of-band gain as their gain function derivatives of frequency approximates to zero. The output plots of the Butterworth-based VBP Σ-Δ modulators are depicted in Figure 35 on page 49.

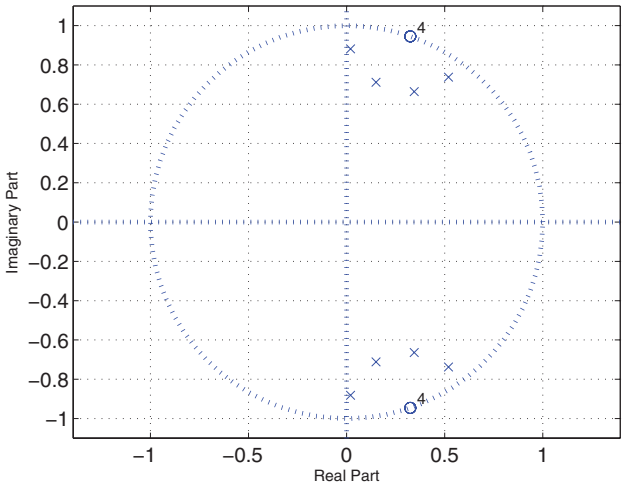



**Figure 55: Butterworth Pole-Zero Map**

To give an overall understanding, Butterworth NTFs have a wider transition band compared to the other filter types. Hence Butterworth-based NTFs achieve much better SNRs and DRs for larger BW values. Due to its maximally flat out-of-band gain, the stability performance of Butterworth based NTFs are comparatively more robust. As far as the analyses allow, they have delivered stable outputs for all the designed VBP Σ-Δ modulators in the thesis for any centre frequency and up to a normalized bandwidth of 0.1.

The numerator and denominator coefficients of the desired Butterworth NTF are obtained using the 'butter' function in Matlab. These coefficients are mapped to the desired topology by using the Matlab Symbolic Toolbox.

### 2nd Order Topologies Employing Butterworth NTF

Both topologies produce noise shaping at their outputs with a few tones. These observed tones are mainly caused by the quantization operation and are analysed in Section 3.11. As both topologies have their coefficients within the same interval, the resulting DR and SNR values

have a perfect match. The SNR plots of both topologies for different OSRs and number paths are shown in Figure 56. It should be noted that all SNR figures in this thesis is plotted such that 0 dB indicates a signal to noise ratio of 1.

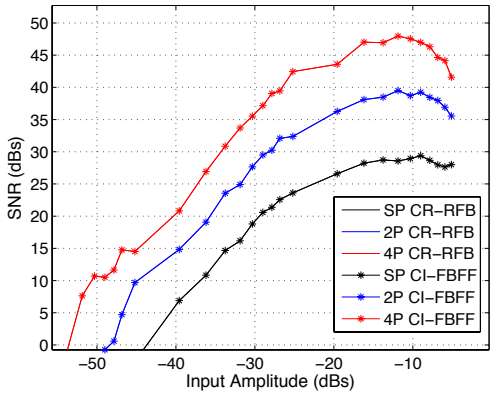



**Figure 56: SNR Plot, 2nd-order Both Topologies, Butterworth NTF, Centre Frequency = 0.375, BW = 0.01, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

In the first place, this plot validates the node-equation method and its extension to VBP Σ-Δ modulators since a higher path number provides better SNR without increasing the individual path OSR. In addition, if the SNR estimation stated in Section 2.6 and calculated in [13] is recalled; every doubling of OSR is supposed to increase the SNR value by (6L + 3) dB where L is the order of the modulator. Increasing the path number without changing the path-OSR increases the overall OSR in multiples of P, where P is the path number.

The resulting SNR values depicted in Figure 56 are quite compatible with their theoretical SNR increment values. Note that an $L^{th}$-order VBP NTF's transition band roll-off is equivalent to the $(L/2)^{th}$-order LP NTF. So for a 2nd-order VBP Σ-Δ modulator, an SNR increment of is expected. Refer to Table 3 and Table 4 on pages 65 and 66 for a compared SNR versus OSR summary.

As expected, the centre frequency sweep in other words the feedback coefficients' variations do not affect the performance as shown in Figure 57. Whereas the bandwidth sweep affects the obtained SNR up to 15 dBs and DR up to 14 dBs as shown in Figure 58. Normalised bandwidths larger than 0.04 do not increase the SNR more than 1-2dBs. Different bandwidth values can be chosen to increase the DR.

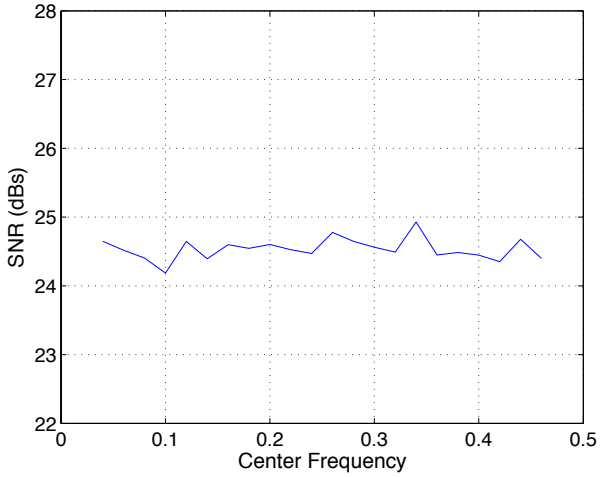
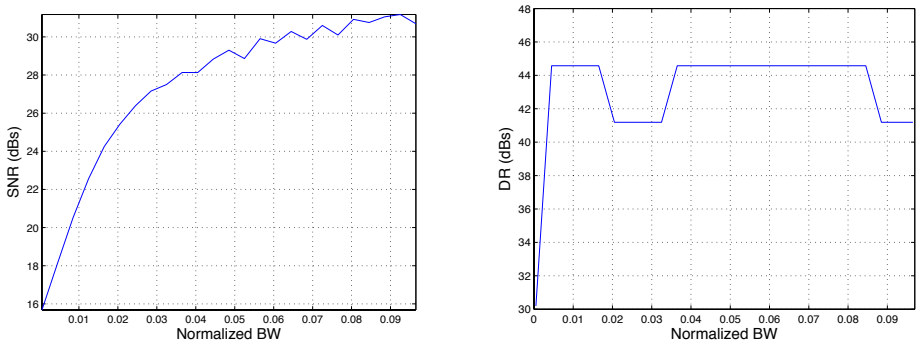



**Figure 57: SNR vs Centre Frequency Plot, 2nd-order 2-path CI-FBFF Topology, Butterworth NTF, BW=0.02, $OSR_{2P} = 16$**

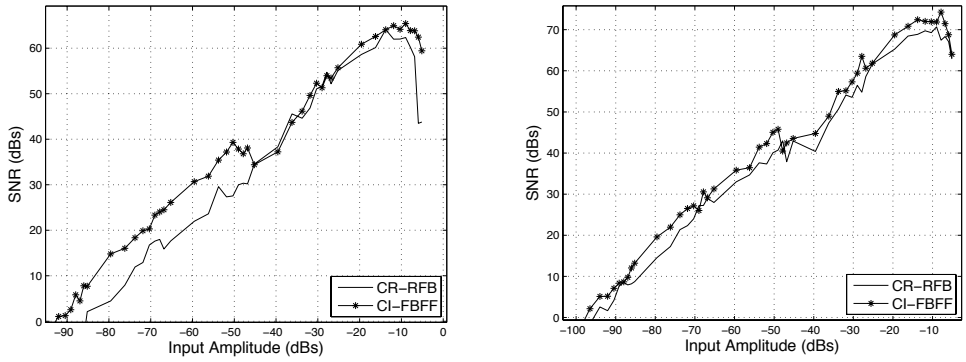



**a)SNR vs BW** **b)DR vs BW**

**Figure 58: BW Sweep Plot, 2nd-order 4-path CR-RFB Topology, Butterworth NTF, Centre Freq.=0.2, $OSR_{4P} = 16$**

## $4^{th} – 6^{th} – 8^{th}$ Order Topologies Employing Butterworth NTF

The output and SNR plots have an adequate matching between the CI-FBFF and CR-RFB for $4^{th}$- $6^{th}$- $8^{th}$ orders of the SP, 2-path and 4-path topologies. However, minor differences occur for different OSRs as shown in Figure 59. These variations are caused by the in-band tones.



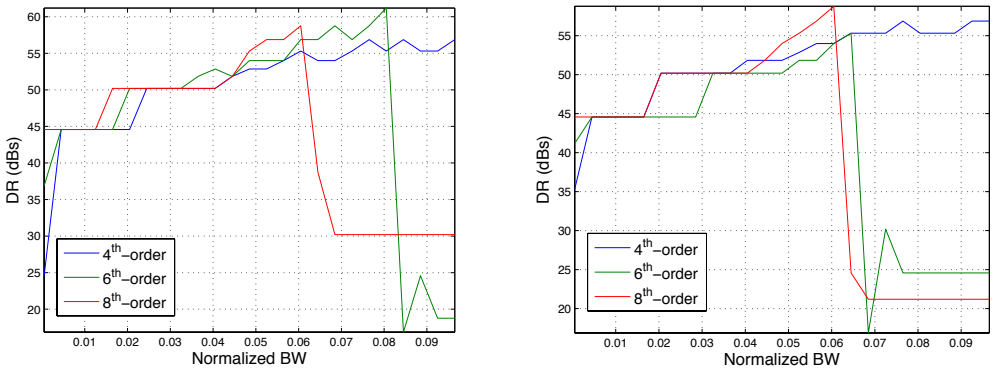

**a)** **b)**

**Figure 59: SNR Plots, Both Topologies, Butterworth NTF, Different OSRs**

**a) 6$^{th}$-order, 4-path, Butterworth, Centre Frequency = 0.405, BW=0.01, $OSR_{4P} = 32$**

**b) 8$^{th}$-order, 2-path, Butterworth, Centre Frequency = 0.405, BW=0.01, $OSR_{2P} = 64$**

Moreover, the SNR versus centre frequency relationship remains the same; the SNR value is not affected by the chosen centre frequency. On the other hand, the DR clearly changes with the bandwidth and the order of the modulator as depicted in Figure 60. This is due to the fact that larger bandwidths and higher-order VBP Σ-Δ modulators tend to possess larger coefficients. Hence the resulting VBP Σ-Δ modulators overload the quantizer for smaller input amplitudes, decreasing the DR as seen in Figure 61.




**a)CI-FBFF, 2-path** **b)CR-RFB, 4-path**

**Figure 60: DR vs BW Plot, Both Topologies, Butterworth NTF, BW=0.02, $OSR_{2P,4P} = 16$**

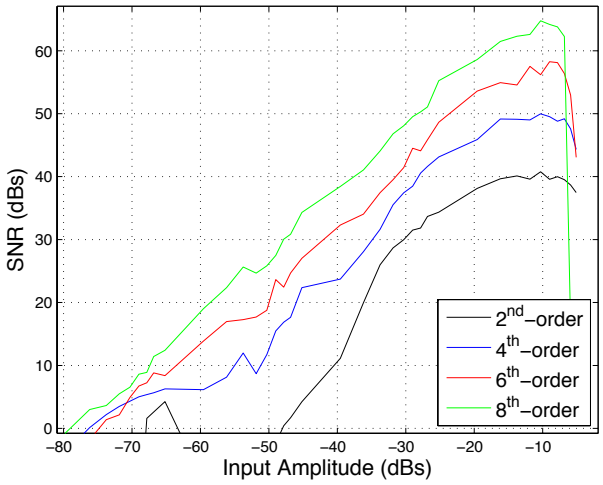



**Figure 61: SNR Plot, All Orders 4-path, Butterworth, CI-FBFF Topology, Butterworth NTF, Centre Frequency = 0.1, BW=0.02, $OSR_{4P} = 16$**

Note that the overall OSR employed in Figure 61 is 16 and the SNR values for the 4-path topologies are depicted. The individual path OSR equals to $16/4$. With such a low OSR, even the 2nd-order 4P CI-FBFF topology delivers an SNR of 39 dB and 8th-order 4P CI-FBFF topology accomplishes 65 dB SNR whilst providing DRs of 45 dB and 75 dB respectively.

In Figure 62, the SNR plot of the 6th-order CR-RFB topology for all path numbers are displayed. But in this plot, the overall OSRs for each SP, 2-path and 4-path topologies are chosen to equate each other. In other words, individual OSRs are chosen to be 64, 32 and 16 respectively. To do so, it is expected to obtain a well-matched SNR plot since all the SP, 2-path and 4-path topologies of same order have the same overall NTF. However, it is clearly seen that, even in the ideal-case simulations the 4-path topology SNR and DR values are smaller. This is due to the tones caused by the time-interleaving nature of the topology and is explained in Section 4.3. To summarize this concept, it must be stated that the TI idea depends on the perfect cancellation of the downsampling images. However before being cancelled at the upsampling circuitry, these images cause quantization tones, which might be folded back into the signal band.

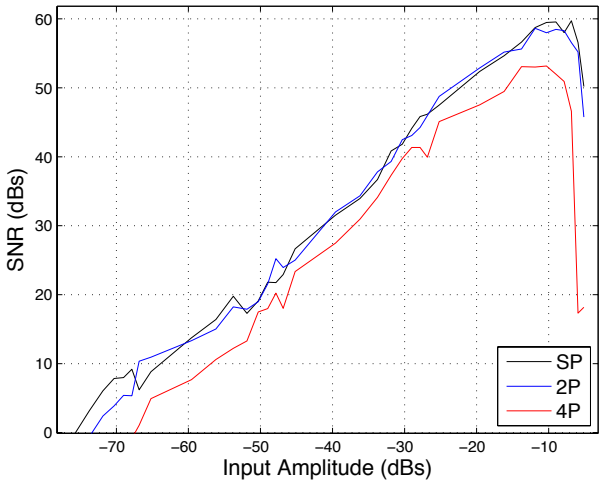



**Figure 62: SNR Plot, 6th-order, All Paths, Butterworth, CR-RFB Topology, Butterworth NTF, Centre Frequency = 0.1, BW=0.02, $OSR_{SP} = 64, OSR_{2P} = 32, OSR_{4P} = 16$**

In Table 3 and Table 4, the summary of obtainable SNRs of Butterworth-based NTFs are given for a specific centre frequency, BW and OSR. The expected SNR increment for every doubling of OSR for different orders are as follows; 2nd-order: 9 dB, 4th-order: 15 dB, 6th-order: 21 dB, 8th-order: 27dB. Since the OSR is fixed in Table 3 and Table 4, these results are expected for every doubling of the TI path number. However, this increment cannot be obtained especially for higher-order Butterworth-based VBP Σ–Δ modulators. This performance degradation is attributed to the in-band tones acquired in the TI topologies and modelled in Section 4.3.

**Table 3: CI-FBFF Topology SNRs and DRs, Butterworth, Centre Frequency =0.3, BW =0.02 , $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **2nd** | 33/42/47 | 40/45/47 |
| **4th** | 38/52/59 | 47/65/73 |
| **6th** | 40/58/70 | 53/69/81 |
| **8th** | 39/65/78 | 53/76/92 |

**Table 4: CR-RFB Topology SNRs and DRs, Butterworth, Centre Frequency =0.3, BW =0.02 , $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **2nd** | 33/42/47 | 38/44/47 |
| **4th** | 38/52/60 | 46/65/73 |
| **6th** | 40/58/70 | 51/70/79 |
| **8th** | 40/58/78 | 52/70/94 |

## Chebyshev NTFs

Chebyshev filters produce amplitude fluctuations in exchange for a steeper transition band. These variations are called pass-band attenuations. To do so; poles lie on an ellipse whereas zeros are placed at the same frequency as shown in Figure 63. Poles closer to the zeros make the filter more aggressive; thus providing a narrower transition band when compared to the Butterworth filters of the same order.

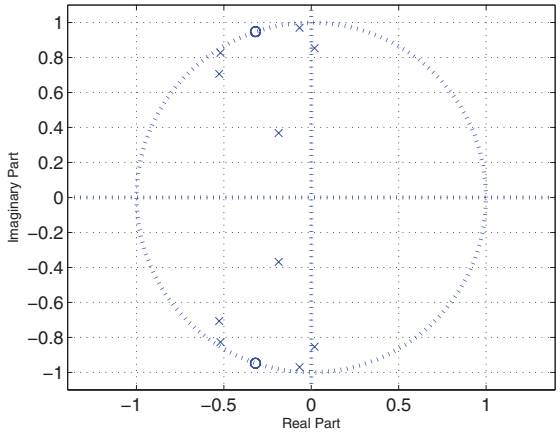



**Figure 63: Chebyshev Pole-Zero Map**

Figure 64 shows a zoomed output plot of the 8th-order SP CI-FBFF topology when a Chebyshev filter is applied. Choosing higher pass-band attenuation eventually causes a more aggressive filter characteristic and raises the possibility of an unstable modulator.

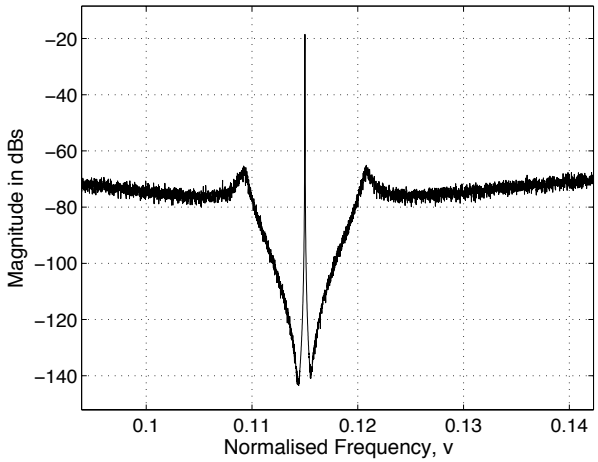



**Figure 64: Zoomed Output Plot, Chebyshev**

The numerator and denominator coefficients of the desired Chebyshev based NTFs are obtained using the 'cheby1' function in Matlab. These coefficients are mapped to the desired topology by using the Matlab Symbolic Toolbox.

### 2nd-, 4th-, 6th-, 8th-Order Topologies Employing Chebyshev NTF

The resulting 2nd-order output plots, the SNR and DR ranges perfectly match as depicted in Figure 65.

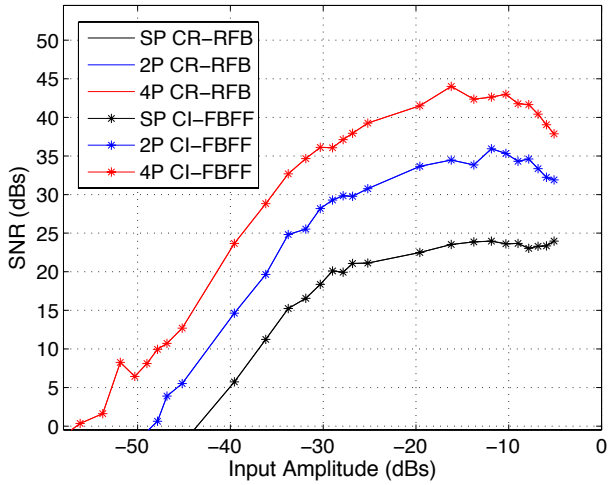



**Figure 65: SNR Plot, 2nd-order Both Topologies, Chebyshev NTF, Centre Frequency = 0.415, BW = 0.01, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

The 6th- and 8th-order SNR and DR performance have minor differences due to the coefficient interval mismatches between the topologies. These values are given in Table 5 and Table 6. In Table 6, a more relaxed Chebyshev NTF is designed whereas in Table 5, a more aggressive Chebyshev NTF is designed. As expected the NTF designed in Table 5 is capable of providing higher SNR and DR. The increases in SNR and DR are obtained by adjusting the passband attenuation rather than modifying the bandwidth. This feature is quite functional for wide-band and high-resolution implementations. Note that the (6L+3) dB of SNR increase for every doubling of the OSR does not apply for Chebyshev NTF-based VBP Σ-Δ modulators for any path number.

**Table 5: CI-FBFF Topology SNRs and DRs, Chebyshev, Centre Frequency =0.4, BW =0.01, PBA=2 dB, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **2nd** | 33/40/43 | 49/50/48 |
| **4th** | 43/55/60 | 57/69/75 |
| **6th** | 50/69/76 | 62/78/88 |
| **8th** | 57/70/84 | 75/81/105 |

**Table 6: CR-RFB Topology SNRs and DRs, Chebyshev, Centre Frequency =0.4, BW =0.01, PBA=0.5 dB, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **2nd** | 21/30/36 | 39/50/48 |
| **4th** | 29/40/49 | 40/51/62 |
| **6th** | 32/45/58 | 40/56/67 |
| **8th** | 39/48/67 | 53/61/77 |

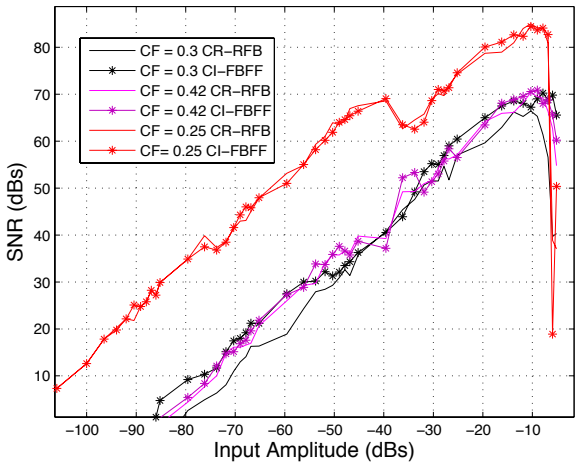



**Figure 66: SNR Plot, 6th-order, 4P, Both Topologies, Chebyshev NTF, BW = 0.01, PBA = 1dB, $OSR_{4P} = 128$**

An interesting observation about Chebsyhev NTF-based VBP Σ–Δ modulators is that they perform quite higher SNR and DR at mid-band even if the pass-band attenuation and bandwidths are fixed. This observation is plotted in Figure 66. This could be attributed to the presence of more or higher amplitude tones at the output since some strong out-of band tones are observed. These limit cycle tones result in deeper notches for Chebyshev NTFs since the overall power at the output spectrum of a quantizer is fixed. This is due to the fact that the expected quantization noise is distributed over $\left[-{}^{\nu_s}/_2, {}^{\nu_s}/_2\right]$.

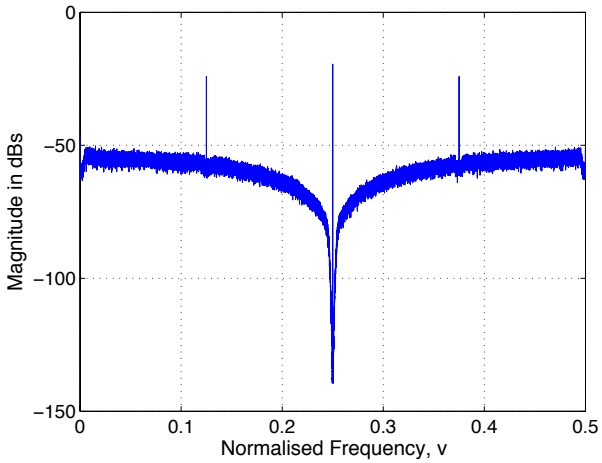



**Figure 67: Output Plot, 6th-order, SP, CI-FBFF Topology, Chebyshev NTF, Centre Frequency = 0.25, BW = 0.01, PBA = 1dB**

These tones may or may not be a problem depending on the implementation. If they are filtered and do not alias with other signals within the system, mid-frequency Chebyshev NTFs give higher resolution. Yet if they are not filtered and pass through other cascade circuits, they may be amplified and therefore degrade the quality of the output signal.

Note that these tones are also observed for other NTF types. An SNR increment as in the case of Chebyshev-based filters cannot be obtained at mid frequency. This is due to the fact that the limit cycle tones appear at close frequencies to the passband attenuations. In a way they help the passband frequency distortion hence steeper transition and higher SNRs are provided.

**Inverse-Chebyshev NTFs**

Inverse-Chebyshev filters distribute zeros over the stop-band to fluctuate the frequency response in order to provide narrow transition-bands. This time, attenuations are at the pass-band region. The numerator and the denominator coefficients of the designed Inverse-Chebyshev based NTF are obtained using the 'cheby2' function in Matlab. These coefficients are then mapped to the desired topology by using the Matlab Symbolic Toolbox.

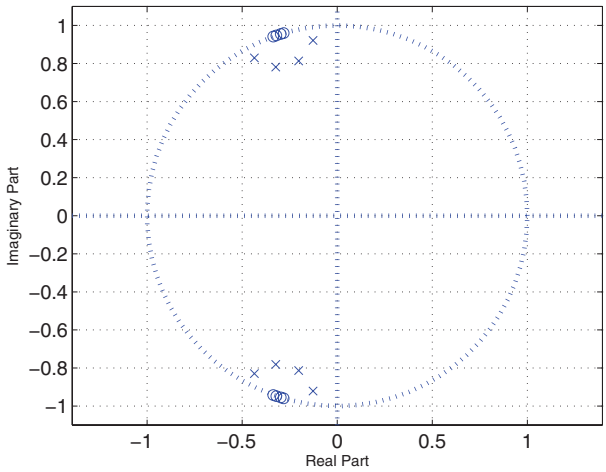



**Figure 68: Inverse-Chebyshev Pole-Zero Map**

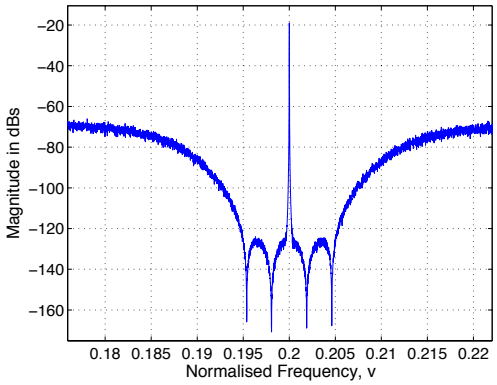



**Figure 69: Zoomed Output Plot, Inverse-Chebyshev**

### $2^{nd}$-, $4^{th}$-, $6^{th}$-, $8^{th}$-Order Topologies Employing Inverse-Chebyshev NTF

The SNR and DR values are given for all orders and all path numbers of the both CI-FBFF and CR-RFB topologies in Table 7-Table 8. Once again, these values are listed to give an idea of the Inverse-Chebyshev NTF-based topology performance. The *(6L+3)* SNR increment rule does not work for Inverse-Chebyshev filters as well.

**Table 7: CI-FBFF Topology SNRs and DRs, Inverse-Chebyshev, Centre Frequency =0.46, BW =0.001, SBA = 80 dB, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **$2^{nd}$** | 41/51/57 | 38/42/46 |
| **$4^{th}$** | 48/63/73 | 64/74/84 |
| **$6^{th}$** | 35/52/63 | 52/69/78 |
| **$8^{th}$** | 30/41/48 | 42/58/73 |

**Table 8: CR-RFB Topology SNRs and DRs, Inverse-Chebyshev, Centre Frequency =0.4, BW = 0.01, SBA = 80 dB, $OSR_{SP} = 16, OSR_{2P} = 32, OSR_{4P} = 64$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **$2^{nd}$** | 34/40/47 | 31/38/40 |
| **$4^{th}$** | 29/46/53 | 43/60/70 |
| **$6^{th}$** | UNSTABLE | UNSTABLE |
| **$8^{th}$** | 32/US/US | 50/US/US |

The Inverse-Chebyshev filters accomplish the highest SNR and DR values when compared to the other NTFs. This is attributed to the distributed zeros over the signal-band. These zeros strongly reduce the overall in-band noise. This becomes more observable for higher-order Inverse-Chebyshev NTFs, as there are more zeros within the signal band. However, there are two main restrictions of Inverse-Chebyshev filter-based NTFs. Firstly, Inverse-Chebyshev filters operate in narrow-band designs; otherwise they drive the Σ–Δ modulator to unstable mode as shown in Table 8.

Secondly the choice of the OSR becomes vital. It was mentioned earlier that distributed zeros over the signal band reduces the in-band quantization noise hence delivering higher SNRs. If the NTF stop-band is not designed such that its zeros remain within the signal band, the Inverse-Chebyshev NTFs lose their attraction. As shown in Figure 70 for higher OSRs, the SNR does not increase within the same slope of the lower OSRs. This is due to the fact, if high OSR is chosen the output frequency response is stretched over a larger frequency scale causing NTF zeros to be placed out of the signal band.

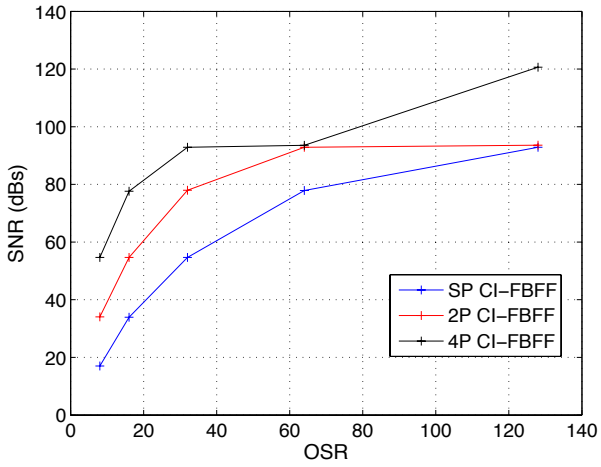



**Figure 70: SNR vs OSR Plot, Inverse-Chebyshev, 6$^{th}$-order, Centre Frequency = 0.3, BW = 0.04, SBA = 80dB**

### Elliptical NTFs

Elliptical filters use both passband and stopband attenuations to accomplish the narrowest transition band with respect to the aforementioned filters. The numerator and denominator coefficients of the desired Elliptical based NTF are obtained using the 'ellip' function in Matlab. These coefficients are then mapped to the desired topology by using the Matlab Symbolic Toolbox. In Figure 71 pole-zero map of an Elliptical band stop filter is given. In addition, to depict the pass-band and stop-band attenuations, a zoomed output response of a $6^{th}$-order Elliptical band stop filter is given in Figure 72.

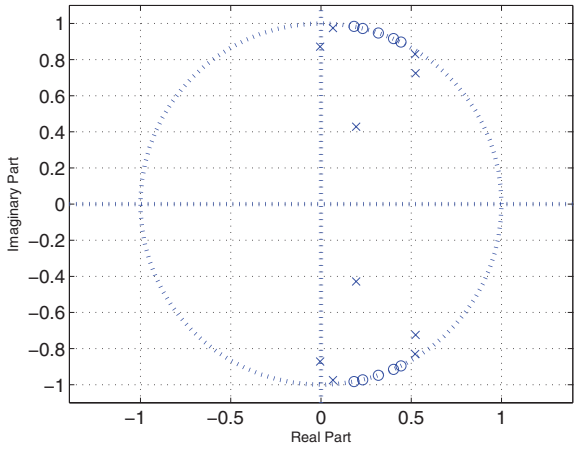



**Figure 71: Elliptical Pole-Zero Map**

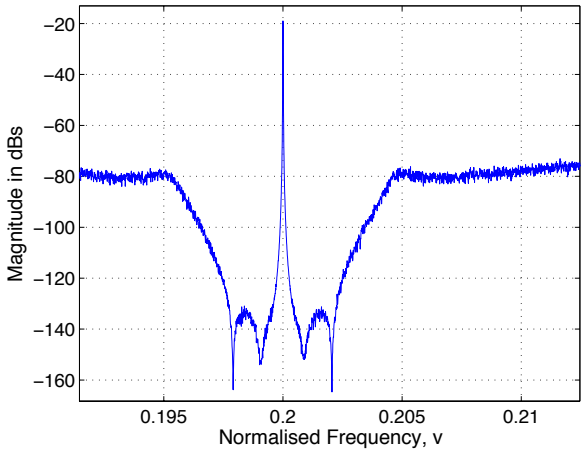



**Figure 72: Zoomed Output Plot, Elliptical**

### $2^{nd}$-, $4^{th}$-, $6^{th}$-, $8^{th}$-Order Topologies Employing Elliptical NTF

See Table 9 and Table 10 for the SNR and DR performance of some Elliptical NTF-based VBP Σ–Δ modulators. The (*6L+3*) SNR increment rule does not work for Elliptical filters.

**Table 9: CI-FBFF Topology SNRs and DRs, Elliptical, Centre Frequency =0.3, BW =0.02, PBA = 1dB, SBA=80dB, $OSR_{SP} = 32, OSR_{2P} = 64, OSR_{4P} = 128$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **$2^{nd}$** | 33/42/47 | 40/45/47 |
| **$4^{th}$** | 38/52/59 | 47/65/73 |
| **$6^{th}$** | 40/58/70 | 53/69/81 |
| **$8^{th}$** | 39/65/78 | 53/76/92 |

**Table 10: CR-RFB Topology SNRs and DRs, Elliptical, Centre Frequency =0.1, BW =0.01, PBA = 1dB, SBA=80dB, $OSR_{SP} = 16, OSR_{2P} = 32, OSR_{4P} = 64$**

| | SNR (dB) (SP/2P/4P) | DR (dB) (SP/2P/4P) |
|---|---|---|
| **$2^{nd}$** | 14/20/23 | 33/39/41 |
| **$4^{th}$** | 19/28/34 | 33/43/61 |
| **$6^{th}$** | 23/31/32 | 32/44/33 |
| **$8^{th}$** | 24/32/36 | 35/46/55 |

The main benefit is that they can accomplish superior SNRs and DRs compared to Butterworth and Chebyshev-based Σ–Δ modulators of the same order for relatively wide narrow-band designs. This is due to the fact that they utilize both pass-band and stop-band attenuations in exchange for a narrower transition band. Moreover, the passband attenuation compensates the effect of the distributed zeros in the out-of-band gain. It lowers out-of-band gain thus providing more stable circuits when compared to Inverse-Chebyshev filters.

## 3.9 Filtering Comparison

The discrepancies in performance of the employed NTF filters were discussed and evaluated in the above section. This section sums up the main diversities.

In Figure 73 a narrow-band NTF's SNR plot is given whereas in Figure 74 an SNR plot for larger-band design is given for all filters. These plots are obtained by setting the cut-off frequencies of each filter as close as possible to each other in order to make a fair comparison of the topologies.

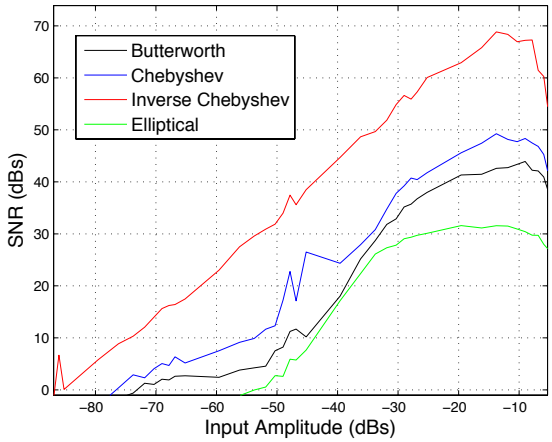



**Figure 73: SNR Plot, All Filters, 4th-order, 2P, CR-RFB Topology, BW = 0.01, OSR = 64**

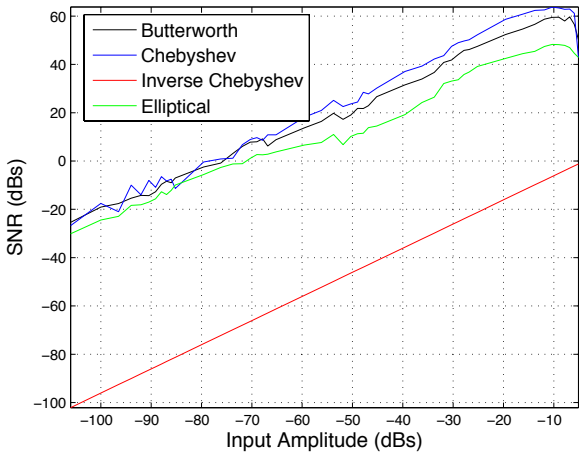



**Figure 74: SNR Plot, All Filters, 4th-order, 2P, CR-RFB Topology, BW = 0.04, OSR = 64**

As seen in Figure 74, the Inverse-Chebyshev based NTF delivers negative SNR for all input amplitude values whilst the other filters provide positive SNR values. This is caused by the increased bandwidth. It can be concluded after several simulations performed within the thesis that the Inverse-Chebyshev NTF based VBP Σ–Δ modulators provide mostly unstable outputs when bandwidth is larger than 0.04 for the 4th-, 6th- and 8th-order topologies. For narrow-band applications the Inverse-Chebyshev based VBP Σ–Δ modulators are highly suitable as long as

the in-band zeros are kept within the signal band. Otherwise, there occurs an apparent SNR reduction as explained in Section 3.8 within the subtitle of Inverse-Chebyshev NTFs.

The Butterworth-based VBP Σ–Δ modulators can be chosen for relatively wide-band applications because they remain stable whilst providing high SNRs and DRs. This is attributed to the maximally flat out-of-band gain of the Butterworth NTFs. As detailed in Section 3.8 within the subtitle of Butterworth NTFs, Butterworth NTF based VBP Σ–Δ modulators they have delivered stable outputs up to a normalized bandwidth of 0.1.

In Section 3.8 the subtitle Chebyshev NTFs explains that the Chebyshev filters actually produce stable outputs with quite strong out-of-band tones at the centre frequency of 0.25. These out-of-band tones might be problematic for implementation purposes as they may alias with other signals within the overall receiver and/or they may be ear-detectable as well.

Finally, the Elliptical and Chebyshev NTFs seem to preserve stability for relatively large bandwidths whilst maintaining the same level of SNR and DR performance to that of their Butterworth counterparts.

### 3.10 Non-Idealities

The designed VBP Σ-Δ modulators' non-ideal behaviours are modelled in order to investigate their immunity to non-idealities. Since discrete-time analogue VBP Σ-Δ modulators are designed, the switched-capacitor circuits' non-ideal behaviours are examined.

Switched capacitor circuits are exposed to several non-idealities such as capacitance voltage dependency, capacitor mismatches and op-amp finite gain. One single non-ideality may result in multiple performance degradation. For instance, finite op-amp gain causes integrator leakage and integrator gain error. Therefore, non-ideal building blocks are investigated rather than addressing components' non-idealities.

**Non-Ideal Integrator:** The transfer function of a non-ideal integrator is given in (51) where $g$ is the gain error and $\alpha$ is the leakage error.

$$H_{ID,non-id}(z) = \frac{gz^{-1}}{1-\alpha z^{-1}} \tag{51}$$

Gain blocks model the gain error, *g,* and the leakage error, α, as shown in Figure 75.

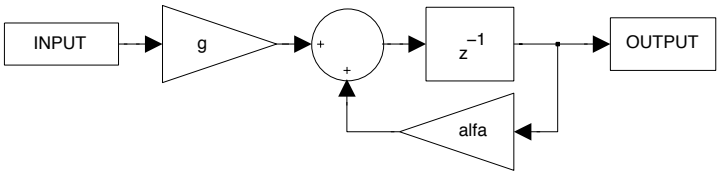



**Figure 75: Simulink Model of Non-Ideal Integrator**

## Non-ideal SP CI-FBFF Topologies

The designed SP CI-FBFF topologies are investigated by applying non-ideal integrators, as their main building blocks are delayless and delayed integrators. The non-idealities are applied to the Simulink model by generating random values for g and α. The random parameters *g* and α lie between $[(-1+e)\ (1+e)]$ where e has a white distribution between a chosen percentage.

In Figure 76 the non-ideal 2nd-order SP CI-FBFF topology is given. In Figure 77 and Figure 78, SNR plots of non-ideal 2nd-order SP CI-FBFF topology are given when 10% gain errors and 10% leakage errors are applied.

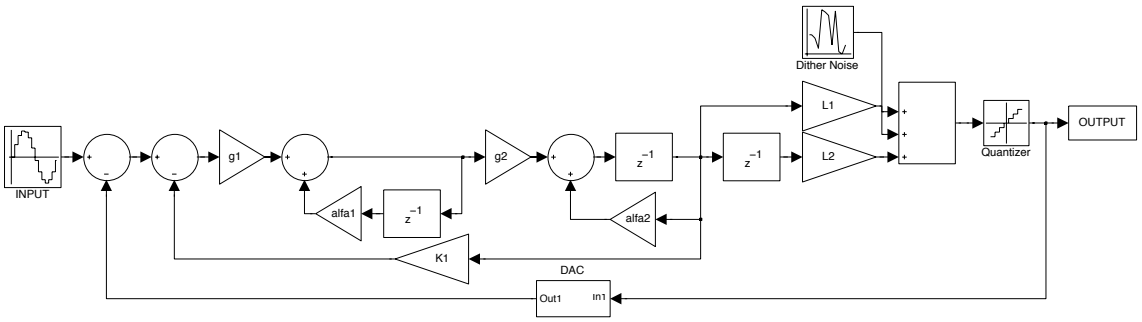
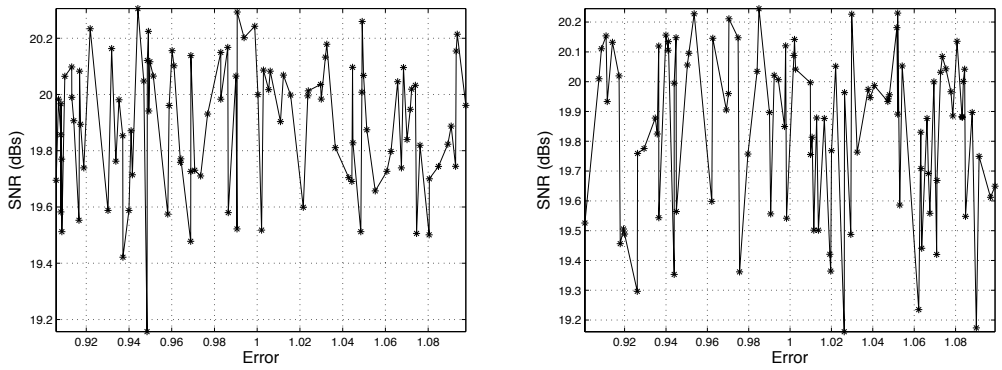
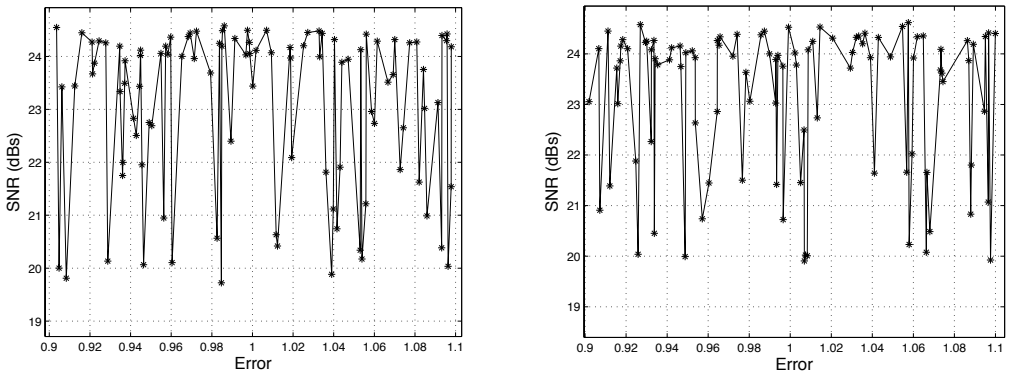



**Figure 76: Non-Ideal 2nd-order SP CI-FBFF Topology**




**a)$g_1$ applied** **b) $g_2$ applied**

**Figure 77: SNR vs Gain Error, 2nd-order CI-FBFF Topology, Elliptical NTF, Centre Frequency =0.1, BW=0.02, PBA= 1 dB, SBA= 80 dB, OSR=16**




**a)$\alpha_1$ applied** **b) $\alpha_2$ applied**

**Figure 78: SNR vs Leakage Error, 2nd-order CI-FBFF Topology, Butterworth NTF, Centre Frequency =0.1, BW=0.02, OSR=16**

The 10% error causes a maximum of 4 dB SNR variations for an OSR of 16. In the mean time, the stability is preserved. If higher OSR values are employed, the tolerable error percentage decreases because of the in-band noise-shaping degradation.

Various simulations showed that SP CI-FBFF topologies are quite sensitive to integrator non-idealities especially for orders above second. This is due to the fact that non-ideal integrators cause both pole and zero displacements. Therefore, both *g* and α may lead to poor SNR and/or unstable modulator. In Table 11, tolerable gain and leakage error percentages are summarized depending on the numerous simulations. These values are concluded such that the modulators do not become unstable and provide 4-8 dBs of SNR and 3-9 dBs DR variations.

**Table 11: Tolerable Error Percentage for SP CI-FBFF Topology**

| Order | Error Percentage |
|---|---|
| **2nd** | 5 % |
| **4th** | 1 % |
| **6th** | 0.1 % |
| **8th** | 0.1 % |

In Section 3.7, the coefficient analysis of the CI-FBFF topologies was given. In this analysis it was depicted that the coefficients of the CI-FBFF topology incredibly increases for centre frequencies above 0.25. This is caused by the cascaded nature of the topology. Hence cascaded integrators accumulate signals at the internal nodes, the feedback and feedforward coefficients will need to increase to balance this accumulation. This situation results in extra sensitivity to non-idealities for centre frequencies above 0.25. In other words, any attempt to impair the ideal behaviour of the topology causes significant variations for pole zero locations. Therefore the CI-FBFF modulators can easily become unstable for centre frequencies above 0.25. Once again, the CI-FBFF topology is not suitable for centre frequencies above 0.25.

Moreover, 4th- and 6th-orders of the SP CI-FBFF topology is quite sensitive to non-ideal behaviours of the integrators. As seen in Table 11, they tolerate only up to 0.1% of errors without going into the unstable region.

**Non-Ideal Resonator:** The transfer function of a non-ideal resonator is given in (52) where $g$ is the gain error, $\alpha$ and $\beta$ are the leakage errors. Note that β causes the centre frequency to shift whilst α results in a finite gain at the resonant frequency.

$$H_{ID,non-id}(z) = \frac{gz^{-1}}{1+\beta K_1 z^{-1} + \alpha z^{-2}} \tag{52}$$

The behavioural simulation model of a non-ideal resonator is depicted in Figure 79.

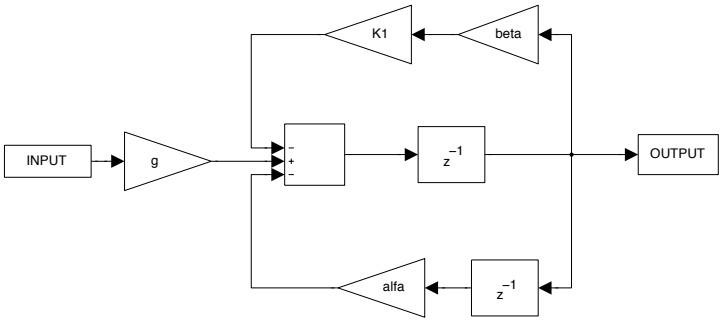



**Figure 79: Simulink Model of Non-Ideal Resonator**

**Non-ideal SP CR-RFB Topologies** All orders of SP CR-RFB topologies are investigated with non-ideal resonators. The non-ideal 2nd-order SP CR-RFB topology is shown in Figure 80.

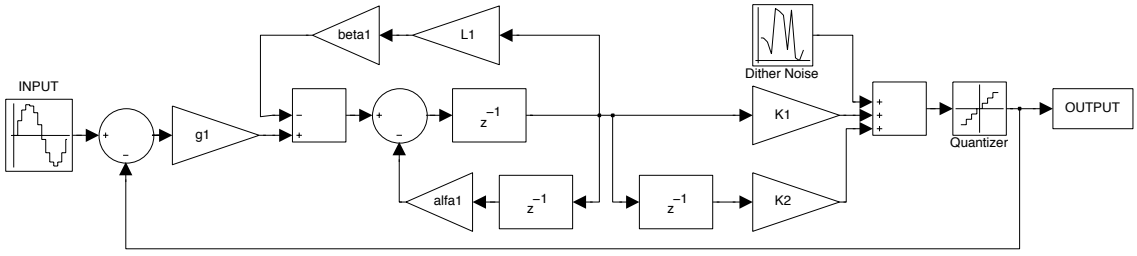


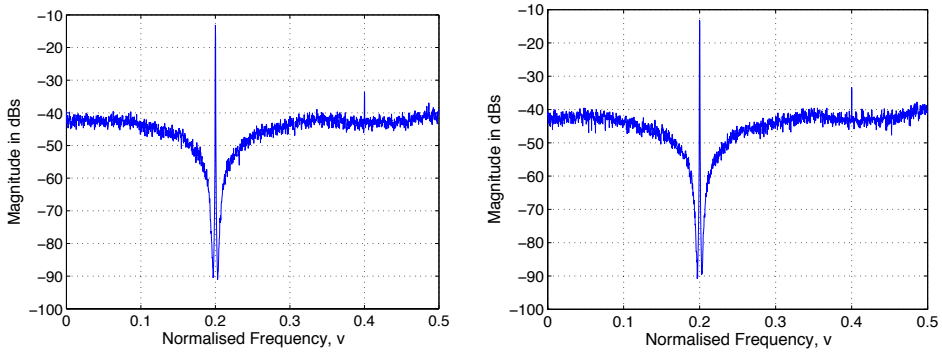

**Figure 80: Non-Ideal 2nd-order SP CR-RFB Topology**

Conversely to the CI-FBFF topologies, the CR-RFB topologies are quite immune to non-idealities from DC to Nyquist. Although the resonators are cascaded, the local feedbacks prevent signal accumulation therefore keeping the coefficients within a suitable interval for different centre frequencies. Once again, in Table 12 tolerable percentage errors are listed. These values have been arrived at to provide 4-8 dBs of SNR and 3-9 dBs DR variations as well as ensuring modulator stability.

**Table 12: Tolerable Error Percentage for SP CR-RFB Topology**

| Order | Error Percentage |
|---|---|
| **2nd** | 20% |
| **4th** | 5% |
| **6th** | 5% |
| **8th** | 5% |

Moreover, the resonant centre-frequency and resonant gain are formed directly by $\alpha$ and $\beta$ respectively. The gain error $g$ only affects the pole locations. So, as long as the poles do not cause instability, the gain error does not affect the output response much as shown in Figure 81.




**a) Ideal case** **b) 10% gain error applied**

**Figure 81: Output Plots, 6th-order SP CR-RFB Topology, Inverse Chebyshev Filter**

**Adder Non-Idealities:** The node-equation technique shares the samples of each node. Therefore, the resulting TI topologies do not require integrator/resonator blocks. Instead resonators and integrators are distributed over the channels just like the samples. The TI topologies only use delayless and delayed adders to perform integration and resonation operations.

The TI topologies are investigated using the non-ideal adder model given in (53). Note that a double delayer adder is depicted in Figure 82. Using a delayed or delayless adder does not change the defined errors; $a_1$ and $a_2$.

$$Out_{adder,non-id}(z) = a_1 z^{-1} In_1 + a_2 z^{-1} In_2 \tag{53}$$

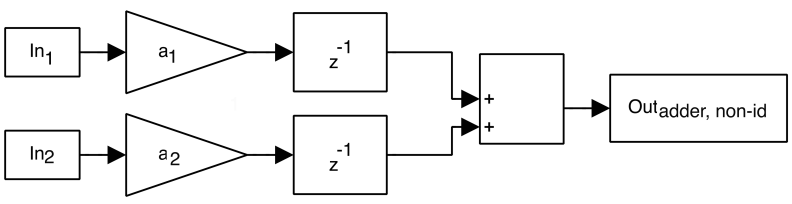



**Figure 82: Simulink Model of Non-Ideal Adder**

**Non-ideal TI Topologies:** The TI topologies' tolerances to non-idealites are listed in Table 13-Table 16. Once again, these values have been evaluated such that the modulators provide 4-8 dBs of SNR and 3-9 dBs DR variations ensuring modulator stability.

**Table 13: Tolerable Error Percentage for 2P CI-FBFF Topology**

| Order | Error Percentage |
|---|---|
| **2nd** | 6% |
| **4th** | 3% |
| **6th** | 3% |
| **8th** | 3% |

**Table 14: Tolerable Error Percentage for 4P CI-FBFF Topology**

| Order | Error Percentage |
|---|---|
| **2nd** | 5% |
| **4th** | 2% |
| **6th** | 2% |
| **8th** | 0.5 % |

As seen, the TI CI-FBFF topologies are more immune to non-idealities when compared to their SP counterparts. This is because of the cross-connected structure of the TI topologies. These non-idealities do not affect the resonant frequency and/or centre frequency directly as is the case with SP topologies. The non-ideal adders inherently create tones and white noise therefore mitigating the in-band NTF degradation.

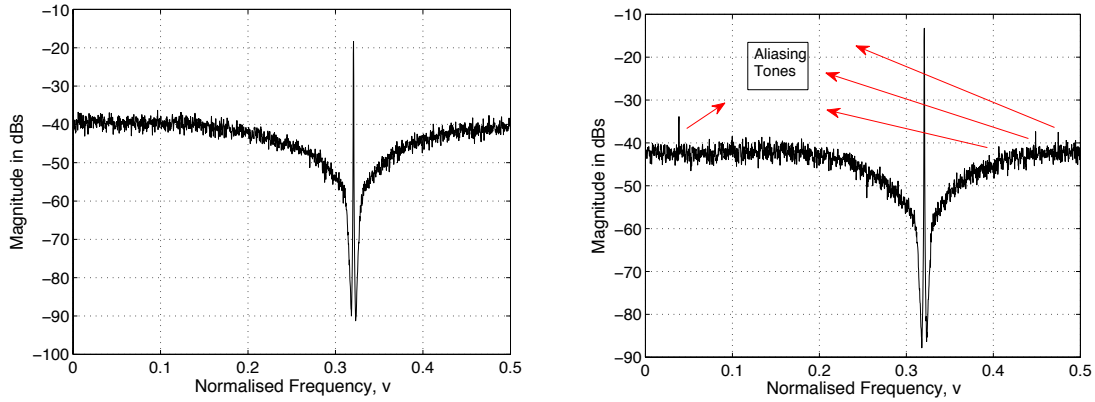
**Table 15: Tolerable Error Percentage for 2P CR-RFB Topology**

| Order | Error Percentage |
|---|---|
| **2nd** | 8% |
| **4th** | 5% |
| **6th** | 5% |
| **8th** | 2% |

**Table 16: Tolerable Error Percentage for 4P CR-RFB Topology**

| Order | Error Percentage |
|---|---|
| $2^{nd}$ | 8% |
| $4^{th}$ | 5% |
| $6^{th}$ | 4% |
| $8^{th}$ | 1% |

However, as will be discussed in Section 3.11.3, the mismatches among channels may create strong tones. These tones are called aliasing tones and tend to appear at frequencies $2\pi i/M$ where $i = 1, 2, \cdots M - 1$ due to the imperfect cancellation of the downsampling images. They may cause instability or they can be folded back into the signal-band degrading the SNR and DR performance of the modulator.




**a) Ideal Case Output** **b) 4% Random Adder Non-Idealities are Applied**

**Figure 83: Aliasing Tones, $6^{th}$-order 4P CR-RFB Topology, Chebyshev Filter**

## 3.11 Quantization Tones

The tonality sources are already defined in Section 2.6.4. The frequency and amplitude of idle channel tones and limit cycle tones are hard to predict. However, there is another source of tonality seriously influencing the performance of VBP Σ–Δ modulators, i.e. the quantization tones. Basically the quantization of a sinusoid creates tones whose amplitudes and frequencies can be mathematically determined. Since the VBP Σ–Δ modulators are excited by single sinusoids, these tones may become observable in some cases. In this section, these tones are investigated for one-bit quantizers.

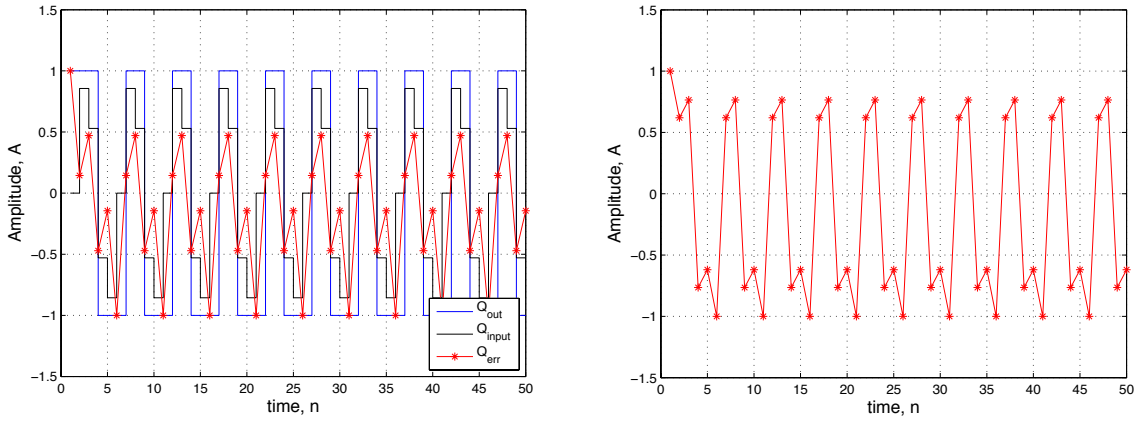
The truth is that D/A VBP Σ–Δ modulators are more likely to produce these tones since the finite wordlength also quantizes the signal. The quantization-tone performance of the D/A VBP Σ–Δ modulators is discussed in Section 4.3.

The quantizaton tones can be modelled using the sawtooth quantization noise model. However, since the quantization noise is highly input signal dependent, the actual power of these tones may become extremely difficult to predict. As a result, a mathematical model is developed for the tones that are caused by the quantization of the sinusoids. This mathematical model is developed for SP VBP Σ–Δ modulators and further extended for the TI VBP Σ–Δ modulators.

### 3.11.1 Sawtooth Quantization Noise Model, One-bit Quantizer, Single Sinusoid

The first step of the sawtooth quantization noise model is to use the additive noise model as already shown in the Section 2.1.

The second step is to define this additive quantization noise as an input signal dependent function. To have a better understanding of this theory, the simulated quantization noise of a sampled-sinusoid for a 1-bit quantizer is shown in Figure 84. In Figure 84-b the quantization noise clearly converges to a sawtooth signal with a frequency of $2\nu_c$ multiplied by a sinusoidal signal with a frequency of $\nu_c$, where $\nu_c$ is the input signal frequency.




**a)** **b)**

**Figure 84: Quantization Noise of a Sinusoid for a 1-bit Quantizer, A=0.9**
**a) Input to the Quantizer, Output of the Quantizer and the Quantization Noise b)The Quantization Noise**

Before getting into the mathematical analysis it must be mentioned that a mathematical model for the triangle wave is also built and compared with the simulation results and a decision is made that the sawtooth error model gives closer amplitude and frequency estimation.

The quantization noise is modelled accordingly in (54) where $SW[n]$ represents the reverse sawtooth function.

$$Q_{err}[n] = SW[n] A_{\sin} \sin\left[2\pi(\nu_c n)\right] \tag{54}$$

An ideal sawtooth wave function can be written as the sum of sinusoids with integer multiples of the fundamental frequency which is $2\nu_c$ in this case.

$$SW[n] = \frac{A_{sw}}{2} - \frac{A_{sw}}{\pi} \sum_{k=1}^{\infty} (-1)^k \frac{\sin\left[2\pi(2\nu_c k)n\right]}{k} \tag{55}$$

The amplitudes are set such that the multiplication of two signals' amplitudes equal to $\Delta_Q$. This is due to the fact that, if the sinusoidal signal sample value is zero, the quantizer will map it to the $\Delta_Q$ value. Moreover, the amplitude values given in (56) are determined after extensive simulations and comparisons of the provided mathematical model to the quantization noise obtained by simulations.

$$A_{sw} = \left(\Delta_Q - A - \varepsilon_1\right), \quad A_{sw} = \Delta_Q \Big/ \left(\Delta_Q - A - \varepsilon_2\right) \tag{56}$$

The trigonometric identity in (57) should be kept in mind to calculate the overall quantization noise in (60).

$$A_1 \sin(a) A_2 \sin(b) = \frac{A_1 A_2}{2}\left(\cos(a-b) - \cos(a+b)\right) \tag{57}$$

$\Delta_Q$ is the quantization step size and $A$ is the input amplitude. Also, $\varepsilon_1$ and $\varepsilon_2$ are the input amplitude dependent errors that are assumed to have a white distribution over $[-\Delta_Q\ \Delta_Q]$. However, in this case they are assumed to be negligible and are approximated to zero for ease

of calculation. Depending on the input signal, a statistical approximation can be made. In addition, it is assumed that there is no overload of the quantizer.

$$Q_{err}[n] = \frac{A_{sw}}{2} A_{\sin} \sin[2\pi\nu_c n] - \left(A_{\sin} \sin[2\pi\nu_c n]\right)\left(\frac{A_{sw}}{\pi} \sum_{k=1}^{\infty} (-1)^k \frac{\sin[2\pi(2\nu_c k)n]}{k}\right) \quad (58)$$

Since the one-bit quantizer is examined; $\Delta_Q = 1$;

$$Q_{err}[n] = \frac{A_{sw}A_{\sin}}{2} \sin[2\pi\nu_c n] - \left(\frac{A_{sw}A_{\sin}}{2\pi} \sum_{k=1}^{\infty} (-1)^k \frac{\cos[2\pi(\nu_c(2k-1))n] - \cos[2\pi(\nu_c(2k+1))n]}{k}\right) \quad (59)$$

$$Q_{err}[n] = \frac{1}{2} \sin[2\pi\nu_c n] - \left(\frac{1}{2\pi} \sum_{k=1}^{\infty} (-1)^k \frac{\cos[2\pi(\nu_c(2k-1))n] - \cos[2\pi(\nu_c(2k+1))n]}{k}\right) \quad (60)$$

Hence, the sawtooth signal is multiplied by a sinusoid, the process of calculating the quantization noise signal is similar to double-sided AM modulation. It is well known that, if a sinusoidal signal with a frequency of $f_1$ is AM-modulated by another sinusoid with a frequency of $f_2$, the resulting tones will be at $(f_2 - f_1)$ and $(f_2 + f_1)$. Since $f_1 = 2f_c, 4f_c, 6f_c$ ... and $f_2 = f_c$, the resulting tones will be at $[\ldots (6-1)f_c, (4-1)f_c, (2-1)f_c,\ f_c, (2+1)f_c, (4+1)f_c, (6+1)f_c \ldots]$.

This mathematical model in (59) has given some knowledge to estimate the frequencies and amplitudes of the tones. In order to visualize the derived mathematical model, an example of the sawtooth quantization noise model is given below. A sinusoid with a normalized frequency of 0.12, given in (61), is directly applied to a 1-bit quantizer. This results in a quantization noise of (62). The simulation results are given in Figure 85 for two different input amplitudes. The output plots of the quantization noise validate the proposed mathematical model. The quantization noise harmonics of a sinusoid are not input amplitude dependent. It should be remembered that tones beyond 0.5 are folded back and added to the already existing tones within the range of [0, 0.5] as their frequency is mapped to $\nu_N$-$\lfloor \nu_N + 0.5 \rfloor$. The operator $\lfloor x \rfloor$ represents the largest integer less than or equal to $\lfloor x \rfloor$ and $\nu_N$ is the normalized frequency of the signal.

$$S_{input} = A\sin\left[2\pi\left(0.12\right)n\right] \tag{61}$$

$$Q_{err}\left[n\right] = \frac{1}{2}\sin\left[2\pi\left(0.12\right)n\right] - \left(\frac{1}{2\pi}\sum_{k=1}^{\infty}\left(-1\right)^{k}\frac{\cos\left[2\pi\left(\left(0.12\right)\left(2k-1\right)\right)n\right] - \cos\left[2\pi\left(\left(0.12\right)\left(2k+1\right)\right)n\right]}{k}\right) \tag{62}$$

The simulated and mathematical results are compared in Figure 85-Figure 86. It should be noted that only fundamental harmonic amplitude is misleading as the sawtooth error model calculates the fundamental signal amplitude using fixed value of 0.5. However, the fundamental harmonic's frequency is actually where the input signal frequency is. So there is no point in calculating it correctly. On the other hand, other harmonics of the quantization noise is calculated such that the maximum difference occurring between the calculated and simulated harmonics is 5 dBs.

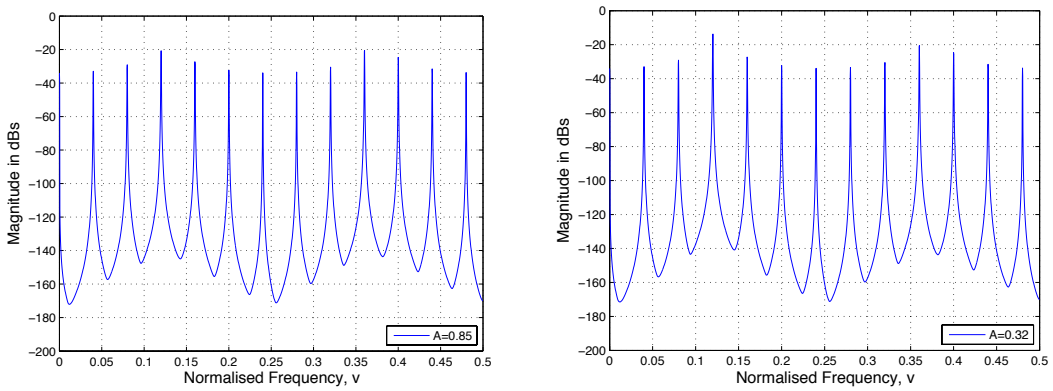



**Figure 85: Simulated Results for Quantization Noise of a Sinusoid, $\boldsymbol{\nu_c = 0.12}$**

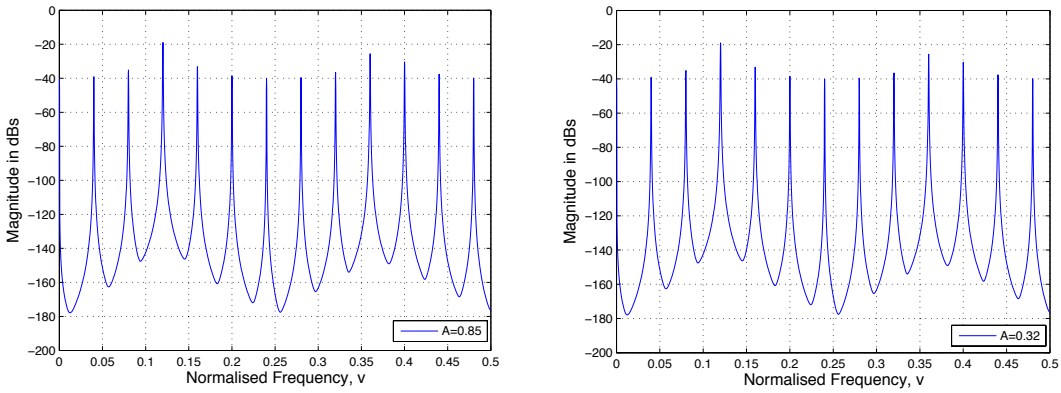
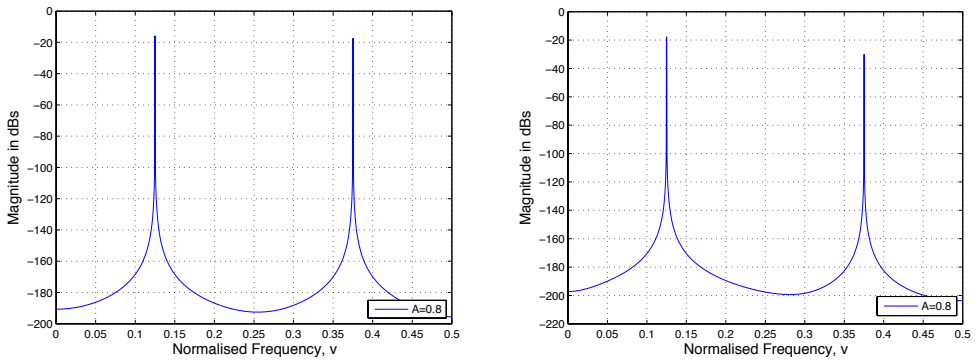



**Figure 86: Calculated Results for Quantization Noise of a Sinusoid, $\boldsymbol{\nu_c = 0.12}$**

The sawtooth quantization noise model can be summed up as follows:

1. The expected high tones in a Σ–Δ modulator resulting from the quantization of a sinusoid, not the limit cycle tones, can be calculated in terms of their frequency and amplitude.
2. The quantization harmonics are not input-amplitude dependent but are dependent on the quantization step. Only the fundamental harmonic's amplitude is determined by the input signal and cannot be calculated by the developed mathematical model.
3. These tones can be whitened by dithering, especially for multi-level quantizers. Due to their smaller $\Delta_Q$s, multi-bit quantizers result in lower amplitude tones when compared to the 1-bit quantizer as expected.
4. At some particular frequencies such as 0.25, 0.125, 0.375…etc dithering may not work sufficiently for all the tones. This is because harmonics of the sawtooth signal are mapped and added to each other at the same frequencies resulting in higher amplitude tones as depicted in Figure 87.

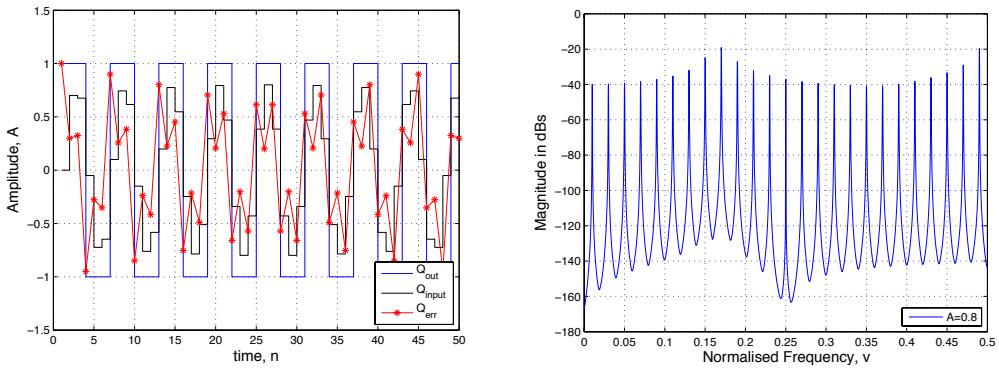
   On the other hand, utilizing a variable centre frequency exhibit more but smaller amplitude tones that can be reduced sufficiently when dithering is employed. This makes the proposed VBP Σ–Δ modulator topologies more attractive compared with their mid-band counterparts.




**a) Simulated** **b) Calculated**

**Figure 87: Quantization Noise of a Sinusoid $\nu_c = 0.375$**

5. Input frequencies, whose frequencies are irrational, result in a higher number of tones since the harmonics of the sawtooth signal are not folded back to the same frequencies. Therefore, the resulting quantization tones have lower amplitudes as shown in Figure 88b. This is due to the fact that irrational frequency tones are mapped close to each other and may not be sufficiently suppressed within the signal-band, thus resulting in significant SNR reduction.




**a) Time Domain** **b) Frequency Domain**

**Figure 88: Simulated Quantization Noise of a Sinusoid, $\nu_c = 0.17$**

Moreover, the presented mathematical model becomes less accurate when the input frequency is irrational. This is due to the fact that, the estimated sawtooth signal is deterioted when the input signal has an irrational frequency as depicted in Figure 88a. Strong in-band tones are still presented with the sawtooth quantization noise model although tones close to DC and Nyquist amplitude values are quite different from the simulation results. Yet their frequencies are calculated precisely as seen in Figure 89.

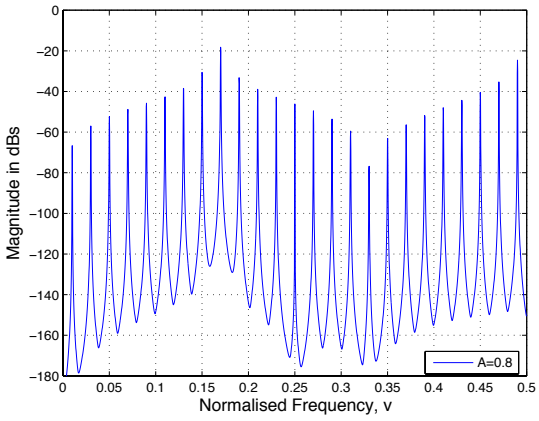



**Figure 89: Calculated Quantization Noise of a Sinusoid, $\nu_c = 0.17$**

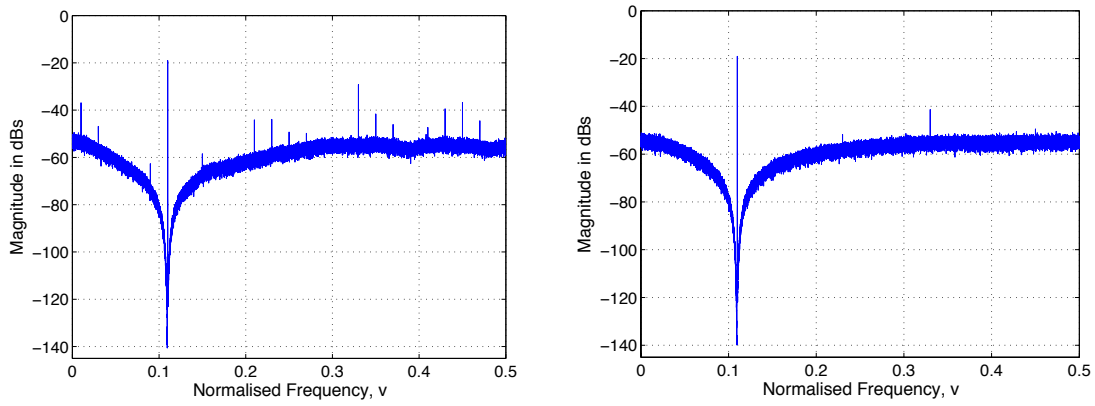
6. The presented quantization noise mathematical model can be extended to any input signal that can be decomposed to a Fourier series. Every single harmonic should be treated as a single input to the quantizer and the resulting quantization noise will be a sum of the individually calculated quantization noise.

### 3.11.2 SP VBP Σ–Δ Modulators Excited by Single Sinusoids

This section presents some output plots for the designed SP VBP Σ–Δ modulator topologies. These Σ–Δ modulators are excited by single sinusoids to characterise and evaluate the effects of quantization tones. Since A/D VBP Σ–Δ modulators work in the discrete analog domain, the only source of quantization tones is the quantizer. Note that in the digital domain the finite wordlength of each path causes the quantization tones as will investigated in Section 4.3.

In A/D modulators, a sampled sinusoid is firstly filtered by the STF and then quantized. The quantization tones are shaped by the NTF hence they pass through the feedback path. Depending on extensive simulations, observations and calculations, it can be concluded that the frequencies of expected quantization tones of a VBP Σ–Δ modulators can be calculated whereas the amplitude of these tones depend on the NTF and STF of the modulator. Moreover, dithering may whiten some of the harmonics.

In Figure 90a, the output plot of a $4^{th}$-order SP-FBFF topology is depicted where the out-of band quantization tones are observed. The in-band tones are mostly suppressed by the NTF. In Figure 90b, the dither noise amplitude is increased to randomise the strong in-band tones at the expense of increased noise floor. Despite this, the second and third harmonics of the developed mathematical model are still present.




**a) Dither Amplitude = 0.005** **b) Dither Amplitude = 0.05**

**Figure 90: Output Plot, SP CI-FBFF 4th-order, Butterworth NTF, Centre Frequency = 0.11, BW=0.02**

In Figure 91, a centre frequency of 0.375 is chosen and applied to the CR-RFB 8th-order topology. Although a 6th-order NTF is employed, the only occurring harmonic cannot be diminished. Since it is way out of the signal band, it does not cause any performance degradation.

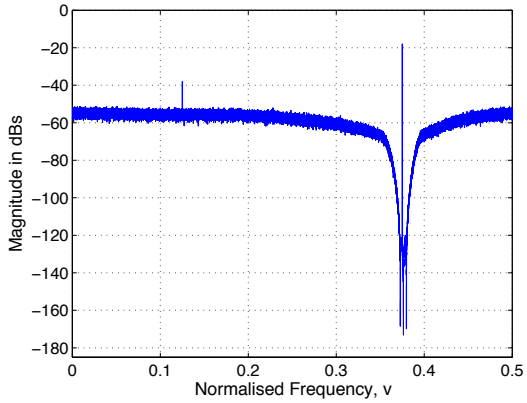



**Figure 91: Output Plot, SP CR-RFB 6th-order, Elliptical NTF, Centre Frequency = 0.375, BW=0.04**

### 3.11.3 TI VBP Σ–Δ Modulators Excited by Single Sinusoids

The TI topologies are likely to produce quantization tones due to the downsampling operation. In addition, if mismatches occur, these tones are not cancelled by the upsamplers. If downsampler's mathematical model is recalled;

$$X_d\left(e^{j\omega}\right) = \frac{1}{D}\sum_{i=0}^{D-1} X\left(e^{j\left(\frac{\omega}{D}-\frac{2\pi i}{D}\right)}\right) \tag{63}$$

Due to the frequency scaling property given in (64), the quantization noise of a sinusoid is recalculated in (65) for a P-path TI structure.

$$f(at-\theta)=\frac{1}{|a|}F\left(\frac{\omega}{a}\right)e^{-\theta/a} \tag{64}$$

$$Q_{err,Downsample}[n]=\sum_{i=0}^{P-1}\left\{\begin{array}{l}\frac{1}{2}\sin\left[2\pi P\nu_c n-2\pi i\right]\\ -\frac{1}{2\pi}\sum_{k=1}^{\infty}(-1)^k\left(\begin{array}{l}\frac{\cos\left[2\pi\left(P\nu_c(2k-1)\right)n-2\pi i\right]}{k}\\ -\frac{\cos\left[2\pi\left(P\nu_c(2k+1)\right)n-2\pi i\right]}{k}\end{array}\right)\end{array}\right\} \tag{65}$$

These tones are shaped by the NTF and thereafter pass through the upsamplers. Harmonics will be attenuated and folded back to the signal band by the upsamplers. If the upsampler's mathematical model is recalled and combined with the frequency scaling property of Fourier analysis, the expression given in (69) is obtained where P is the path number.

The sawtooth quantization noise mathematical model given in (69) is developed for a single downsampled and upsampled sinusoidal signal that is directly applied to a quantizer. As a result, each path of the TI topologies produce the resulting tones as they are all stimulated by downsampled sinosidal signals. Note that, the amplitude of the quantization tones are shaped by the overall NTF for a TI Σ-Δ modulators. Therefore, the amplitudes in (69) are replaced by *B* and *C* representing the NTF shaped amplitudes..

$$X_u\left(e^{j\omega}\right)=X\left(e^{j\omega U}\right) \tag{66}$$

$$X_u(n)=\frac{1}{|U|}X_u\left(\frac{n}{U}\right) \tag{67}$$

$$Q_{err,Upsample}[n]=\sum_{i=0}^{P-1}\left\{\begin{array}{l}\dfrac{1}{2P}\sin\left[\dfrac{2\pi P\nu_c n-2\pi i}{P}\right]\\ -\left(\dfrac{1}{2\pi P}\sum_{k=1}^{\infty}(-1)^k\left(\begin{array}{l}\dfrac{\cos\left[\dfrac{2\pi\left(P\nu_c(2k-1)\right)n-2\pi i}{P}\right]}{k}\\ -\dfrac{\cos\left[\dfrac{2\pi\left(P\nu_c(2k+1)\right)n-2\pi i}{P}\right]}{k}\end{array}\right)\right)\end{array}\right\} \tag{68}$$

$$Q_{err,TI}[n]=\sum_{i=0}^{P-1}\left\{\begin{array}{l}B\sin\left[2\pi\nu_c n-\dfrac{2\pi i}{P}\right]\\ -\left(C\sum_{k=1}^{\infty}(-1)^k\left(\begin{array}{l}\dfrac{\cos\left[2\pi\left(\nu_c(2k-1)\right)n-\dfrac{2\pi i}{P}\right]}{k}\\ -\dfrac{\cos\left[2\pi\left(\nu_c(2k+1)\right)n-\dfrac{2\pi i}{P}\right]}{k}\end{array}\right)\right)\end{array}\right\} \tag{69}$$

The quantization tones seen in the SP topologies are also observed in TI topologies. Yet the shifted copies of these tones are also observed. More importantly, they are folded back into the signal band and can cause in-band tones. Another fundamental problem is that the strongest quantization harmonic will not occur at the input frequency where the NTF zeros are placed. Therefore, of course depending on the input frequency, some very strong tones can be observed within the signal band. Specifically the odd-path numbered TI topologies may produce odd frequency multiples that cannot be mapped onto each other but rather harmonics are distributed over the frequency band. Hence this is the main reason to design even-path numbered TI topologies.

The output plots of some TI topologies are given below where the quantization tones can be clearly observed whereas in their SP counterparts these tones do not occur. This basic phenomenon has not been mentioned in any previous publications to the best knowledge of the author. In [92] these tones are observed and referred to as limit-cycle tones caused by the path

mismatches. However, it is proved that these tones can be observed even for the ideal-case simulations.

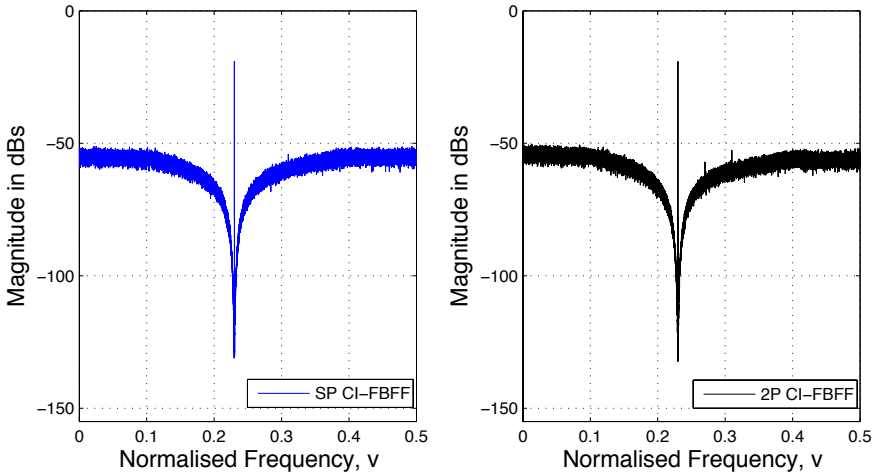



**Figure 92: Output Plot, 2P and SP CI-FBFF 4th-order, Chebyshev NTF, Centre Frequency = 0.23, BW=0.02**

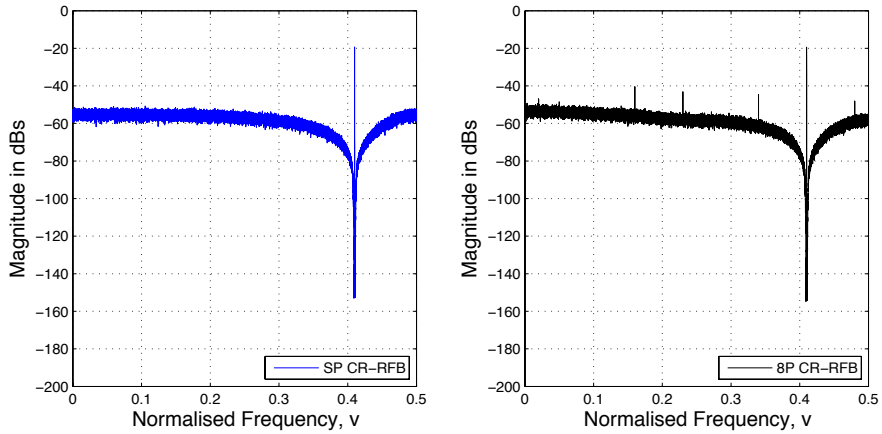



**Figure 93: Output Plot, SP and 8P CR-RFB 8th-order, Inverse-Chebyshev NTF, Centre Frequency = 0.42, BW=0.002**

## 3.12 Conclusion

This chapter constitutes the backbone of the overall thesis. Firstly, the motivations to build up A/D VBP Σ-Δ modulators are detailed whilst inspecting the conventional receiver architectures; superheterodyne and homodyne receivers. It is shown that VBP Σ-Δ modulators are promising for future technologies as they eliminate the mixer and passive circuitry. Moreover, they provide flexibility hence making it easier to build tunable architectures.

A generalized NTF of a VBP Σ-Δ modulator was developed from filter principles. By utilizing the given NTF and mapping it to an appropriate Σ-Δ modulator topology, a generalized SP VBP Σ-Δ modulator could be constructed. However, the high OSR requirements of Σ-Δ modulation technique needed to be compensated. So, the node-equation method was introduced and applied to VBP Σ-Δ modulators. The node-equation method is an easy-to-apply mathematical technique. Moreover, it is not coefficient-dependent like the polyphase decomposition technique. It simplifies the process of designing and building generalized TI VBP Σ-Δ modulators. Finally, a step-by-step design technique to construct generalized TI VBP Σ-Δ modulators was provided and supported with an example as presented in Section 3.3.6.

Generalized 2-path and 4-path TI VBP Σ-Δ modulators of $2^{nd}$-, $4^{th}$-, $6^{th}$- and $8^{th}$-orders were developed using this design technique. Two different loop-filter topologies were selected to map the NTF. The CI-FBFF utilizes the integrators whereas the CR-RFB utilizes the resonators as their building blocks. Therefore their ideal and non-ideal simulation results give different responses.

These two generalized topologies are evaluated in terms of their coefficients, stability, SNR and DR performance as well as immunity to non-idealites. It is concluded that the CI-FBFF topology is not suitable to implement for frequencies above 0.25 because of its very large feedback and feedforward coefficients. However, the CR-RFB topology's feedback and feedforward coefficients are within a realizable interval. Thereby, the CR-RFB topology provides good resolution and is suitable for implementation for any centre frequency.

On the other hand, the non-ideality simulations revealed that the node-equation technique and resulting TI topologies are quite immune to non-idealities. They can provide their resolution and stability up to the given percentage errors listed in Table 13-Table 16. This is the result of their cross-connected architectures. The resonant behaviour of the overall TI structure is not determined by individual adders. All adders contribute to the NTF zeros and poles' locations. Hence, the presence of a highly non-ideal adder can be compensated by other adders. Therefore another advantage of building TI topologies has been established.

Finally, the quantization tones that are produced by a quantizer that is excited by a single sinusoid were mathematically modelled. The developed mathematical model uses the sawtooth error model and extends it to calculate the amplitude and frequency of these tones. The simulation tones and calculated tones were compared and the findings of this model were listed in Section 3.11. The SP topologies and the TI topologies are investigated in terms of their quantization tones. It has shown that the TI topologies were more likely to produce the quantization tones.

# Chapter 4. D/A TI VBP Σ-Δ Modulators

D/A Σ-Δ modulators are basically digital data processors, in which a multi-bit digital data stream is converted to coarse digital data. By doing so, the actual DAC circuitry saves hardware, area and power [93], [94]. In this chapter, one-bit D/A Σ-Δ modulators are investigated. Hence the required DAC circuitry is represented by a comparator that maps the one-bit data to a positive or negative supply voltage [95], [96]. Moreover the expensive trimming and/or calibration circuit is excluded [97], [98]. The block diagram of the intended D/A converter scheme is given in Figure 94.

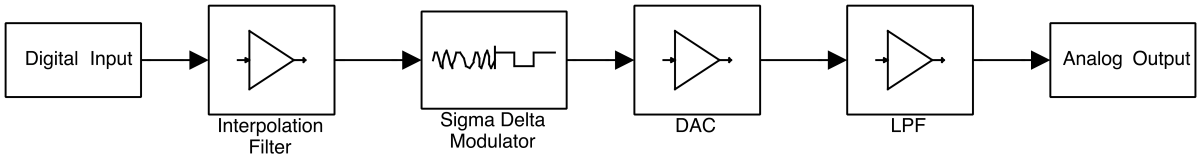



**Figure 94: D/A Converter Block Diagram**

The interpolation filter mainly accommodates the signal rate to the desired oversampling-ratio and suppresses the spectral images. Then the VBP Σ-Δ modulator converts the N-bit digital data to one-bit digital data. Thereafter the DAC, in other words the comparator, produces the analog signal. This signal is either band-pass or low-pass filtered regarding its-band.

The subject of interest in this study is the single-bit VBP Σ-Δ modulators in which the analog design challenges still exist such as high OSR, BW limitation, stability and tonality. Therefore generalized D/A VBP Σ-Δ modulators are designed and implemented that are capable of achieveing noise shaping at any desired center frequency and bandwidth with a choice of filter types: Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical. As mentioned, these NTFs ensure stability whilst giving the ability to control the bandwidth, pass-band and stop-band attenuations. This in return helps to tune the Σ-Δ modulator to the desired signal band without the need for extra filter blocks.

Once again the node-equation method is applied to the designed SP topologies in order to overcome the high OSR requirement.

The key feature of the VBP Σ-Δ modulator topologies built in this section is that they use delay elements as their main building blocks rather than integrators. Integrators are especially advantageous in A/D Σ-Δ modulators for two reasons. First of all; they are easy to build using switched capacitor circuits. Secondly, they supress high frequency noise, therefore resulting in more stable circuits. However, they cause signal accumulation through the internal nodes. The accumulation in the internal path increases the overall hardware of the digital implementations. This is due to the fact that the accumulated internal path requires an increased number of bits. In addition, the pitched analog signals do not occur in digital circuits, thus making integrators less attractive. Delay blocks not only prevent signal accumulation but are also easy to build in digital circuits requiring less power and area.

In this section; two fundamental Σ-Δ modulator topologies, ErrorFeedback (EF) and OutputFeedback (OF), are built in MATLAB, implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit. The step taken further is that the hardware consumption of the OF topology is significantly decreased as will be covered in Section 4.2.1.

## 4.1 Output Feedback and Error Feedback Topologies

The block diagrams of the EF and the OF topologies are illustrated in Figure 95 and Figure 96 respectively.

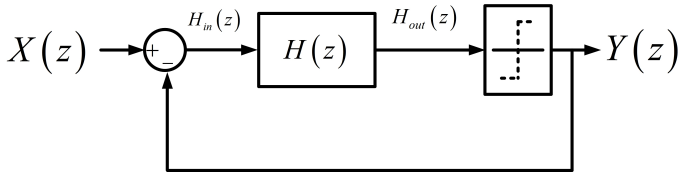



**Figure 95: The OF Topology**

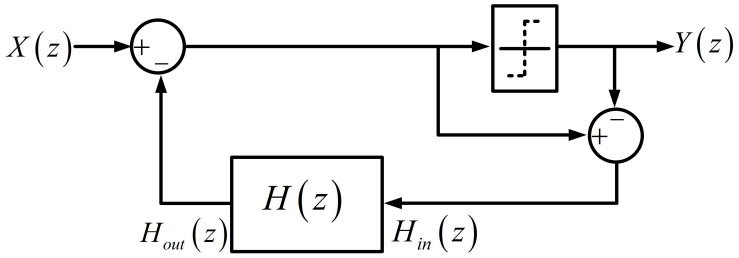



**Figure 96: The EF Topology**

The NTFs and the STFs of both topologies are given in (70)-(73) where $H(z)$ is the transfer function of the loop-filter. Note that the NTFs and the STFs are calculated using the white-noise approximation.

$$STF_{OF}(z) = \frac{H(z)}{1+H(z)} \tag{70}$$

$$STF_{EF}(z) = 1 \tag{71}$$

$$NTF_{OF}(z) = \frac{1}{1+H(z)} \tag{72}$$

$$NTF_{EF}(z) = 1 - H(z) \tag{73}$$

The EF topology filters the quantization noise, i.e. the quantization noise. The quantization noise is obtained by subtracting the quantization input from its output in the block diagram. However in the implementation, the quantization and subtraction operations are performed by the truncation of the quantizer's input signal. The MSB is the output of the Σ-Δ modulator and the remaning LSBs are fedback to the loop-filter. That is why in EF topologies, the quantization noise is usually referred to as the truncation error. In addition, the EF topology has another advantage when implemented digitally; it does not cause any signal corruption due to its unity STF.

On the other hand, the OF topology is generally chosen in analog implementations, since analog non-idealities of the loop-filter are not directly added to the input as in the EF topology. However, this study reveals that for a digital VBP Σ-Δ modulator implementation, the OF topology is more beneficial when implementation limitations such as internal data-path number and propagation delays arise.

## 4.2 Loop-Filter Design

The NTF is chosen to provide generalized Σ-Δ modulators that can accomplish noise shaping from DC to Nyquist for various filter types such as Butterworth, Chebyshev, Inverse-

Chebyshev and Elliptical. The generalized transfer function of an L[th]-order generalized Band Stop (BS) NTF is given in (74).

$$NTF_{gen}(z) = \frac{\prod_{k=1}^{L/2}\left(1 - 2b_k z^{-1} + z^{-2}\right)}{1 + a_1 z^{-1} + \cdots + a_{L-1} z^{-L+1} + z^{-L}} \tag{74}$$

As given in (74), the numerator is an $L^{th}$-order resonator in which $b_k$ determines the resonant frequency. The 4[th]-order resonator transfer function is calculated in (75) and (76).

$$H_{res,4^{th}}(z) = \left(1 - 2b_1 z^{-1} + z^{-2}\right)\left(1 - 2b_2 z^{-1} + z^{-2}\right) \tag{75}$$

$$H_{res,4^{th}}(z) = \left(1 - 2\left(b_1 + b_2\right) z^{-1} + \left(1 + 4b_1 b_2\right) z^{-2} - 2\left(b_1 + b_2\right) z^{-3} + z^{-4}\right) \tag{76}$$

It can be clearly seen in (76) that the second and fourth coefficients of a 4[th]-order resonator transfer function are symmetrical. Moreover, the fifth coefficient is unity. To simplify the equation, the coefficients of (76) are renamed as in (77). The transfer function of an $L^{th}$-order resonator is given in (78).

$$H_{res,4^{th}}(z) = \left(1 + c_2 z^{-1} + c_3 z^{-2} + c_2 z^{-3} + z^{-4}\right) \tag{77}$$

$$H_{res,L^{th}}(z) = \left(1 + c_2 z^{-1} + c_3 z^{-2} + \cdots + c_{(L/2)+1} z^{-(L/2-1)} + \cdots + c_3 z^{-(L-2)} + c_2 z^{-(L-1)} + z^{-L}\right) \tag{78}$$

To sum up, the $L^{th}$ and the $1^{st}$ coefficients of an $L^{th}$-order resonator are unity and the remaining coefficients are symmetrically equal. This symmetry can be very useful in the design of the loop-filter since it eliminates half of the multiplication blocks. The NTFs of the OF and EF topologies are given in (72) and (73) respectively. The NTFs are re-calculated in (79) and (80), where the transfer functions of the loop-filters are replaced by $num_H/den_H$.

$$\begin{aligned} NTF_{OF}(z) &= \frac{1}{1 + num_H / den_H} \\ NTF_{OF}(z) &= \frac{den_H}{den_H + num_H} \end{aligned} \tag{79}$$

$$NTF_{EF}(z) = 1 - num_H / den_H$$
$$NTF_{EF}(z) = \frac{den_H - num_H}{den_H} \quad (80)$$

(79) reveals that the denominator of the loop-filter directly determines the numerator of the $NTF_{OF}$. To take the advantage of the symmetrical numerator of the NTF, a loop-filter must be designed such that the denominator coefficients are individually determined by the loop-filter's coefficients.

### 4.2.1 FBFF TDA Loop-filter

In Figure 97, the FeedBack and FeedForward (FBFF) Time Delay and Accumulate (TDA) topology, commonly known as the Direct Form-1 IIR filter topology is shown. With properly chosen coefficients, both EF and OF topologies can perform Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters. Thus these topologies provide flexibility by enabling designers to specify the centre frequency, signal bandwidth as well as the passband and stopband attenuation parameters.

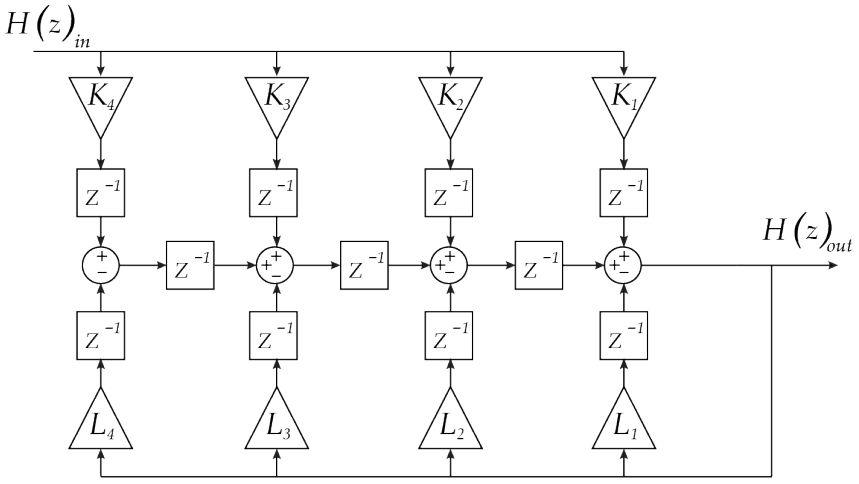



**Figure 97: 4th-order FBFF TDA Loop-filter**

The key point of the designed FBFF TDA topology is that the delay blocks are distributed between adders and multipliers to prevent long combinational delays and to balance the registering [99]. These delayers even the in-coming signal timings to each adder block. As

long as the multiplication operations are performed within a clock interval there is no path delay for the loop-filter.

The transfer function of the FBFF TDA loop-filter is given in (81). The symbolic NTF formulae of the OF and EF topologies are calculated in (82) and (83) respectively.

$$H(z) = \frac{K_1 z^{-1} + K_2 z^{-2} + K_3 z^{-3} + K_4 z^{-4}}{1 + L_1 z^{-1} + L_2 z^{-2} + L_3 z^{-3} + L_4 z^{-4}} \tag{81}$$

$$NTF_{OF}(z) = \frac{1 + L_1 z^{-1} + L_2 z^{-2} + L_3 z^{-3} + L_4 z^{-4}}{1 + (K_1 + L_1) z^{-1} + (K_2 + L_2) z^{-2} + (K_3 + L_3) z^{-3} + (K_4 + L_4) z^{-4}} \tag{82}$$

$$NTF_{EF}(z) = \frac{1 + (L_1 - K_1) z^{-1} + (L_2 - K_2) z^{-2} + (L_3 - K_3) z^{-3} + (L_4 - K_4) z^{-4}}{1 + L_1 z^{-1} + L_2 z^{-2} + L_3 z^{-3} + L_4 z^{-4}} \tag{83}$$

For a 4$^{th}$-order SP Σ-Δ modulator there are supposed to be 4 feedback multiplications for the OF topology. But using the FBFF TDA loop-filter results in only 2 feedback multiplications. Note that in (82), the numerator of the $NTF_{OF}$ is determined directly by the feedback coefficients. Since the numerator of an NTF of a VBP Σ-Δ modulator is composed of resonators as analysed in Section 4.2.1. $L_4$ is unity and $L_1$ equals to $L_3$.The designed 4$^{th}$-order 2P OF Σ-Δ modulator topology saves 4 multiplication blocks and the 4P OF Σ-Δ modulator saves 8 multiplication blocks. To generalize this rule; an L$^{th}$ order P-Path OF Σ-Δ modulator utilizing the FBFF TDA loop-filter saves $P \times L/2$ multiplication blocks.

The 4$^{th}$-order SP OF and EF topologies are depicted in Figure 99. Their 2P and 4P counterparts are also built using the node-equation method and illustrated in Figure 100 and Figure 101 respectively.

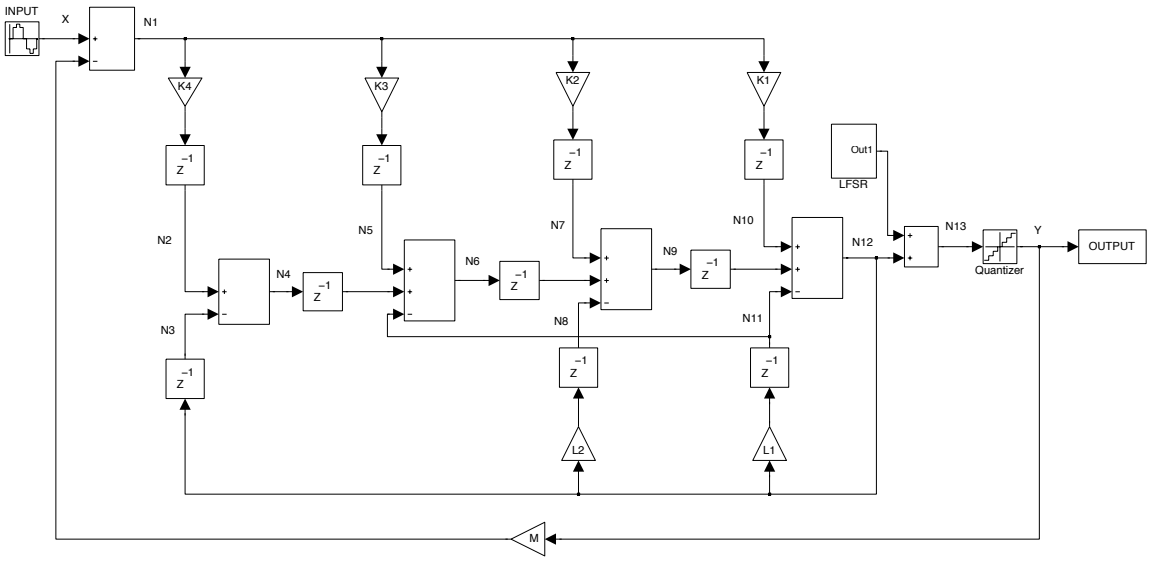



**Figure 98: SP 4th-order OF Topology**

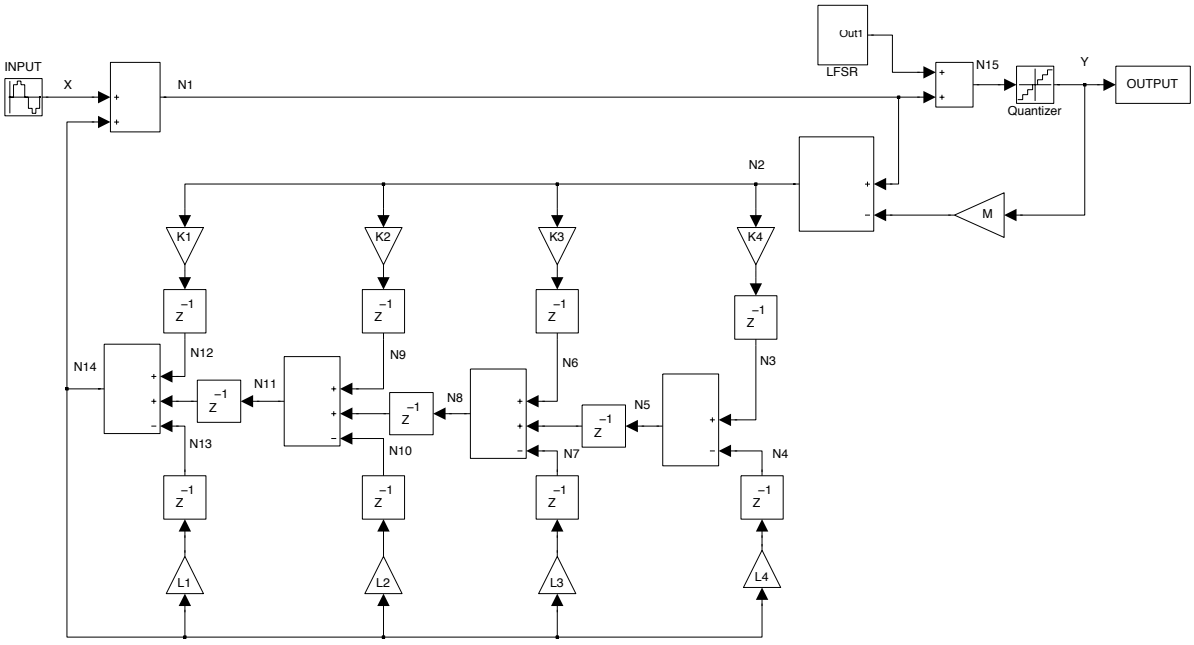



**Figure 99: SP 4th-order EF Topology**

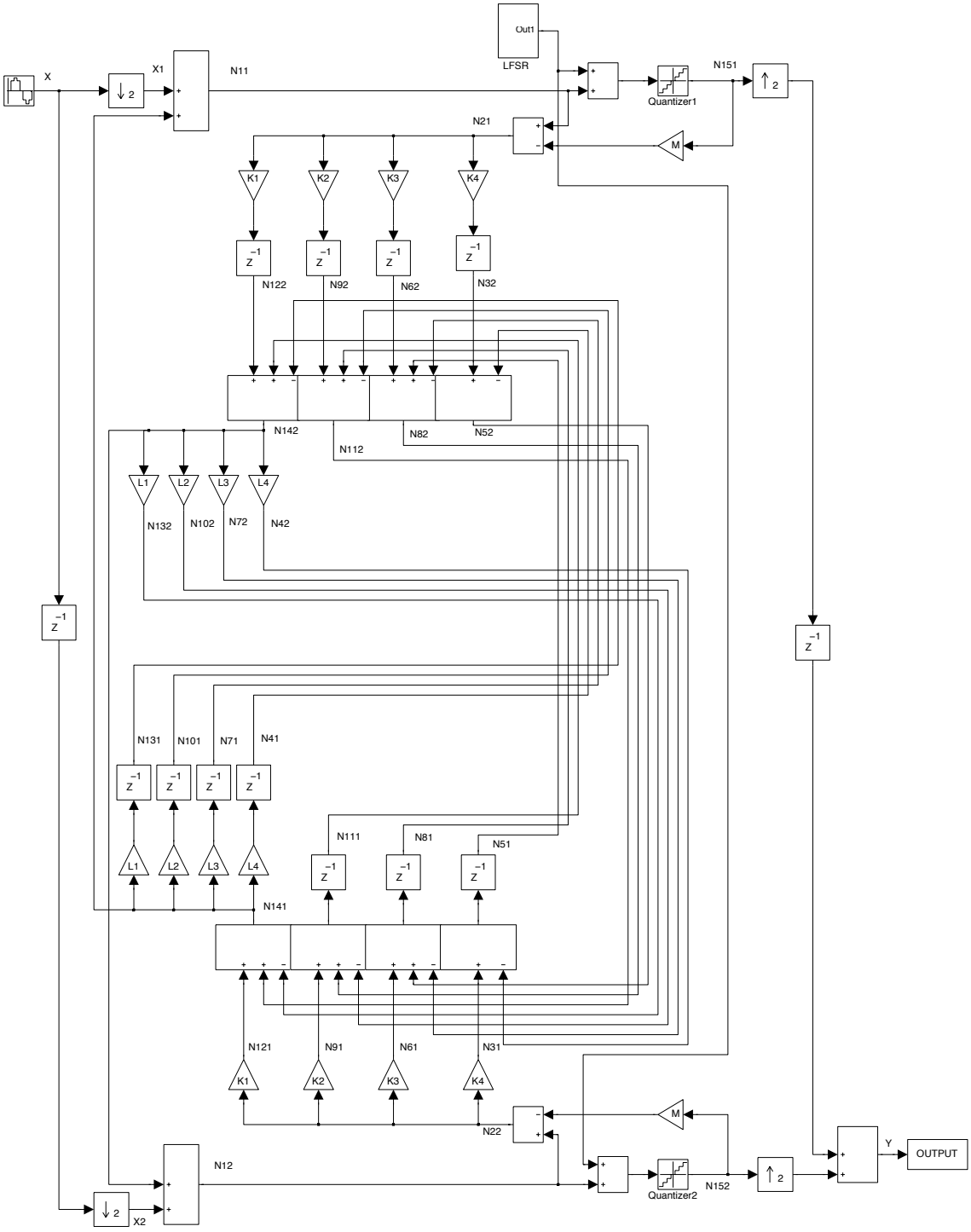



**Figure 100: 2P 4th-order EF Topology**

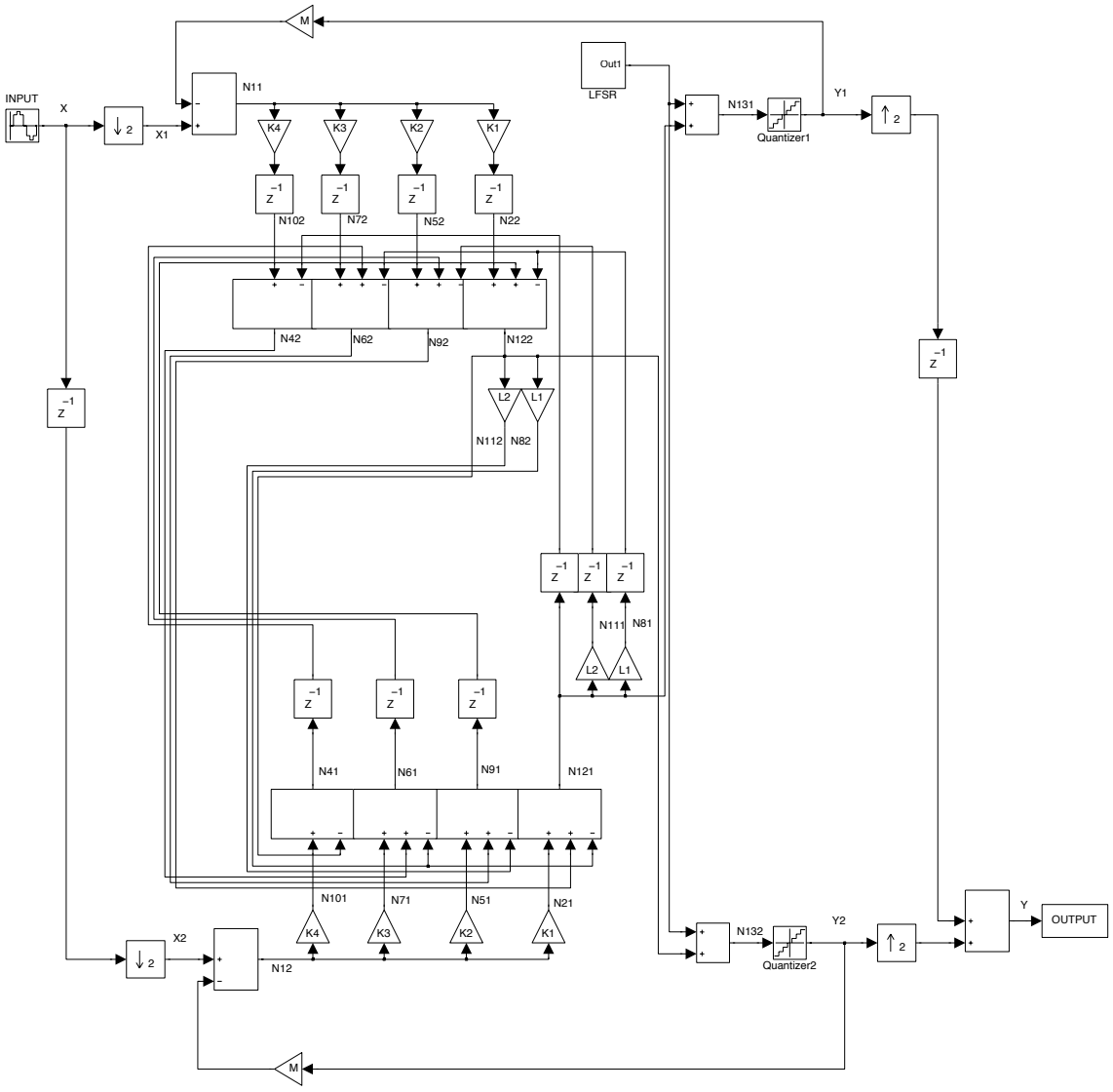



**Figure 101: 2P 4$^{th}$-order EF Topology**

### 4.2.2 Particular Frequencies

Although significant savings have been achieved in the feedback multiplication blocks of the OF topology, there are some particular frequencies at which designers can even save more. These particular normalized frequencies and their corresponding feedback coefficients are listed in Table 17 for the OF topology. When $\nu = 1/6$ and $\nu = 1/3$, the multiplication blocks that perform the $L_1$ and $L_3$ multiplications are replaced with a shifter. When $\nu = 1/4$, there are no multiplication blocks, but only one shifter is needed for the $L_2$ multiplication.

**Table 17: Particular Frequencies and Corresponding Loop-filter's Feedback Coefficients for the OF Topology**

| Normalized Frequency | $L_1$ | $L_2$ | $L_3$ | $L_4$ |
|---|---|---|---|---|
| **1/6** | $-2.0009 = \sim$-2 | $3.0009 = \sim 3$ | $-2.0009 = \sim$-2 | 1 |
| **1/4** | 0 | 2 | 0 | 1 |
| **1/3** | $-2.0009 = \sim$-2 | $3.0009 = \sim 3$ | $-2.0009 = \sim$-2 | 1 |

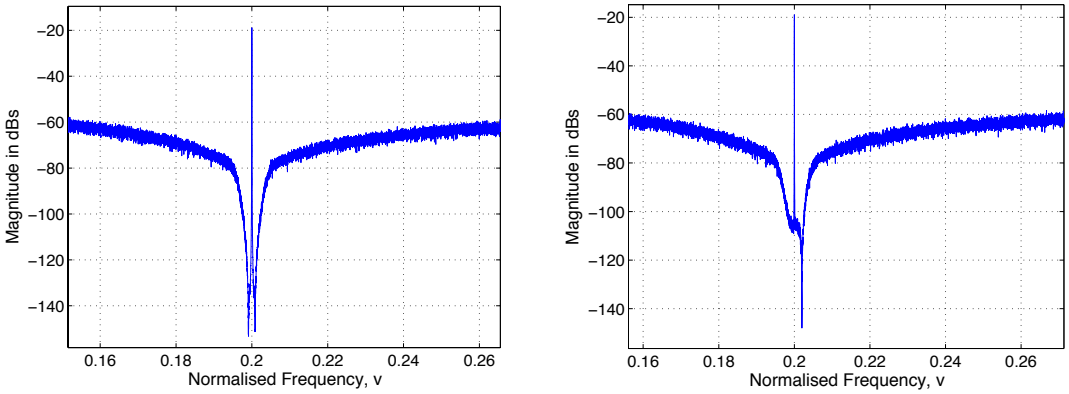
## 4.3 Quantization Tones

In Section 3.11 the quantization tones of a single-bit quantizer were mathematically modeled for a single sinusoidal input signal. In Sections 3.11.2 and 3.11.3 this mathematical model was evaluated for SP and multi-path VBP Σ-Δ modulators respectively. The main findings of this analyses were that the expected tone frequencies could be determined if the input signal frequency were known. The amplitude of these tones depends on the loop-filter, order of the Σ-Δ modulators as well as the frequency of the input signal. However, dither can be used to reduce these tones, but this will be at the expense of an increased noise level.

For the D/A VBP Σ-Δ modulators these characteristics are still applicable. However, D/A VBP Σ-Δ modulators tend to be more tonal. The finite wordlength also behaves as a quantization operation as it truncates the input signal and internal signals. Therefore quantization tones need to be investigated.

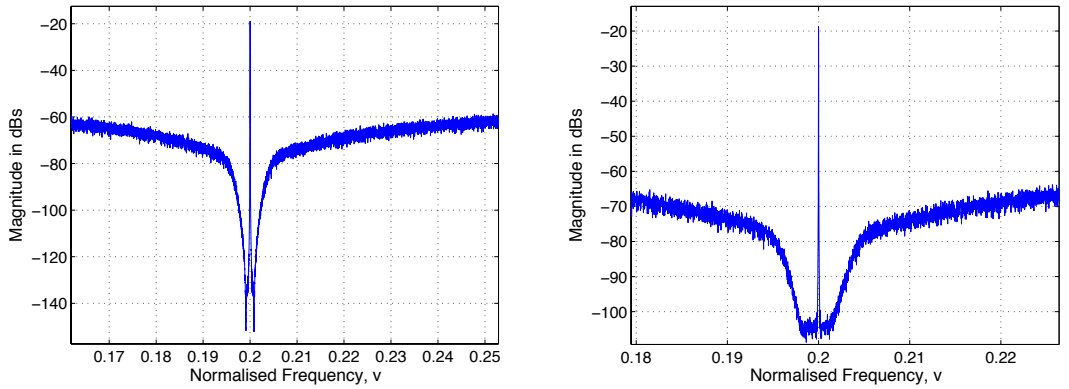
The finite wordlength effect is generally referred to as truncation noise. In [100], [101], finite wordlength errors are assummed to be uniformly distributed, white and uncorrelated. They are added to the existing path whenever a truncation occurs. This assumption serves quite well for internal path, as they are added up together and/or multiplied to each other. Moreover, if the finite worlength effect is thought to be a quantization operation, these internal quantizers are not excited by a single sinusoid. Therefore the quantization noise converges to white noise. In this sense, D/A VBP Σ–Δ modulators tend to have an increased noise floor level when compared to their A/D counterparts. Moreover, for the TI topologies where the number of multipliers and adders is increased, the overall noise floor is increased as well when compared to their SP counterparts. In addition, the finite wordlength of coefficients cause NTF shaping

degradation. The elevated noise floor and degraded noise-shaping can be seen in Figure 102 and Figure 103.




**a) Ideal Case** **b) 15-bits Fractional Wordlength**

**Figure 102: Zoomed Output Plots, D/A 2P 6$^{th}$-order Elliptical NTF, OF Topology, Centre Frequency = 0.2, BW = 0.01, SBA = 1 dB, PBA = 60 dB**




**a) Ideal Case** **b) 15-bits Fractional Wordlength**

**Figure 103: Zoomed Output Plots, D/A 2P 6$^{th}$-order Elliptical NTF, EF Topology, Centre Frequency = 0.2, BW = 0.01, SBA = 1 dB, PBA = 60 dB**

The white noise produced by the finite wordlength of the coefficients diminishes the discrete quantization tones caused by the quantizer.

Note that the EF and OF topologies result in different responses when non-ideal behaviours, finite wordlengths of input signal and coefficients, are applied. The finite wordlength effect on the overall performance of the EF and OF topologies is examined in Section 4.5.1.

Another source of quantization tones is the finite wordlength input signal itself. The mathematical model given in (65) can be recalled and modified for an N-bit fractional finite wordlength acting as a quantizer. If an N-bit fractional resolution is chosen, M equals to $2^{-N}$.

$$Q_{err,TI}[n] = \sum_{i=0}^{P-1} \left\{ \frac{M}{2P} \sin\left[ 2\pi \nu_c n - \frac{2\pi i}{P} \right] - \left( \frac{M}{2\pi P} \sum_{k=1}^{\infty} (-1)^k \left( \frac{\cos\left[ 2\pi \left( \nu_c (2k-1) \right) n - \frac{2\pi i}{P} \right]}{k} - \frac{\cos\left[ 2\pi \left( \nu_c (2k+1) \right) n - \frac{2\pi i}{P} \right]}{k} \right) \right) \right\} \quad (84)$$

The input signal wordlength is chosen to be 16 bits (1-bit for the sign and 15-bits for the decimal part). The resulting quantization tones are displayed in Figure 104. As clearly seen, the resulting quantization tones have quite low amplitudes and can easily be masked by the overall quantization noise produced within the modulator and shaped by the NTF. Note that these tones act as input signals to the Σ–Δ modulator and are shaped by the STF. Yet again, the visible tones at the output are produced by the one-bit quantizer.

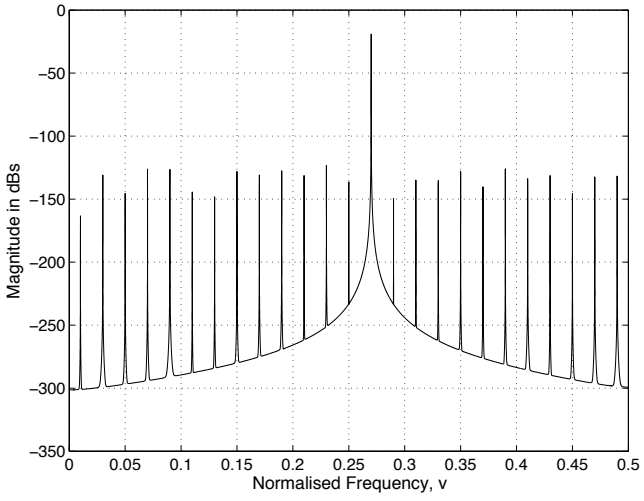



**Figure 104: Finite Wordlength Input Signal and Its Quantization Tones, Freq.=0.27, Amplitude = 0.5, 15-bit Fractional Resolution**

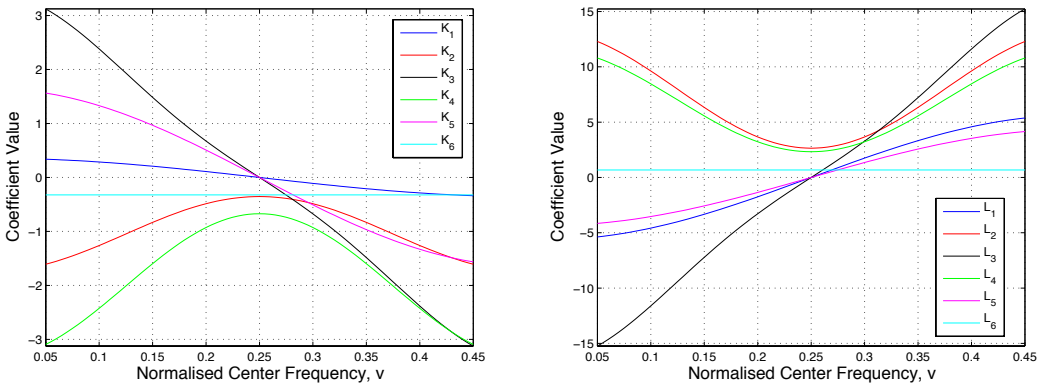
## 4.4 Behavioural Level Simulations

The 2nd-, 4th- and 6th-order D/A VBP Σ-Δ modulators are built using the FBFF TDA loop-filter for both the EF and OF topologies. Moreoever their 2P and 4P TI counterparts are designed using the node equation method. These structures are shown in Appendix C and Appendix D.

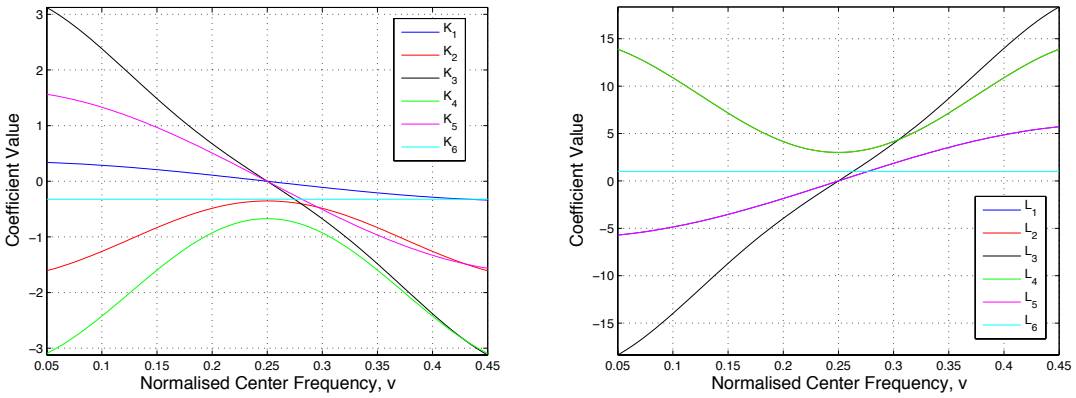
### 4.4.1 Coefficient Comparison

The OF and EF topologies' feedback and feedforward coefficients have comparable amplitudes for a chosen filter type and filter specifications. This is due to the fact that the delayers do not produce any accumulation, hence the feedback and feedforward coefficients are solely dependent on the filter coefficients as given in (82) and (83).

The relationship between these coefficients versus the normalised centre frequency is illustrated Figure 105. Similarly, the relationship between these coefficients versus the normalised bandwidth is shown in Figure 106. The order of the magnitude as well as the actual values of these coefficients can be implemented with relative ease

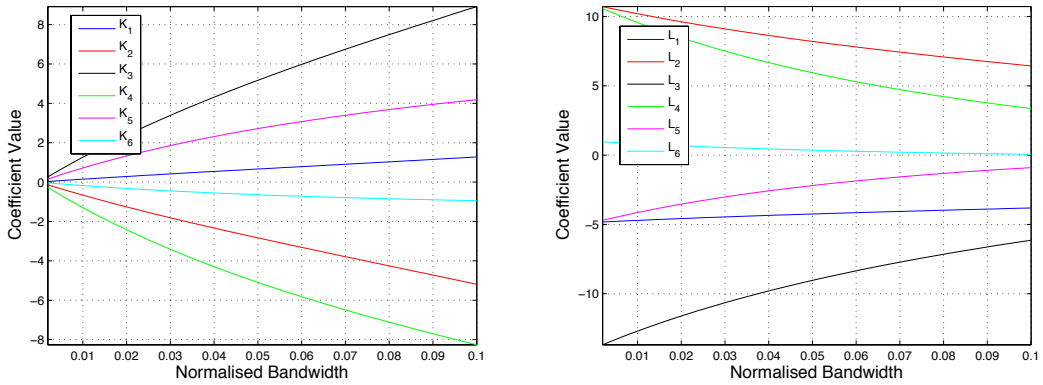



**a) The EF Topology**

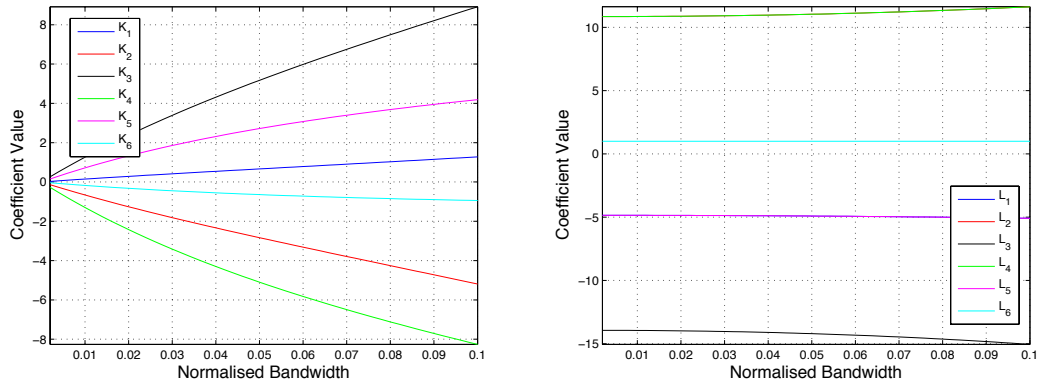



**b) The OF Topology**

**Figure 105: Feedback and Feedforward Coefficients versus Centre Frequency, Elliptical NTF, PBA= 2dB, SBA = 60dB**




**a) The EF Topology**




**b) The OF Topology**

**Figure 106: Feedback and Feedforward Coefficients versus Bandwidth Elliptical NTF, PBA= 2dB, SBA = 60dB**

### 4.4.2 Filtering Performance and Comparison

Behavioural level simulations are performed for the ideal case where finite wordlength is only applied to the input signal. As expected, the behavioural level simulations results are highly similar to the A/D behavioural level simulations given in Section 3.4. To demonstrate some examples, the output plots of some D/A VBP Σ-Δ modulators for different path numbers and orders are illustrated in Figure 107-Figure 109. The quantization tones can be clearly observed for these ideal case simulations especially for the TI topologies.

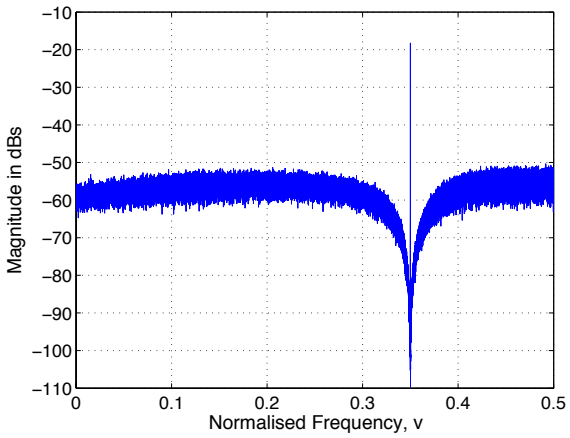



**Figure 107: 2nd- Order SP OF Topology, Butterworth NTF, Centre Frequency = 0.35, BW=0.01**

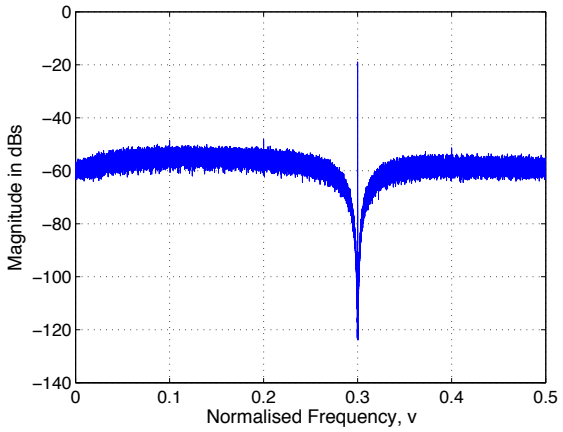



**Figure 108: 4th- Order 2P EF Topology, Chebyshev NTF, Centre Frequency = 0.35, BW=0.01, PBA=1 dB**

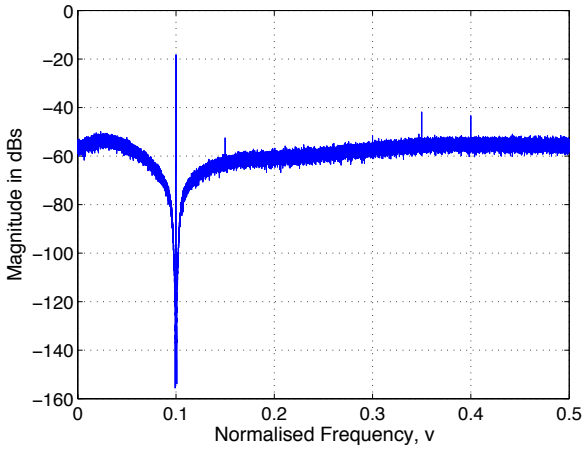



**Figure 109: 6th- Order 4P 0F Topology, Inverse Chebyshev NTF, Centre Frequency = 0.1, BW=0.01, SBA=60 dB**

In Figure 110, the SNR plots for different orders and path numbers are shown. The Inverse-Chebyshev filter yields the highest SNR due to the distribution of its NTF zeros across the entire signal band region.

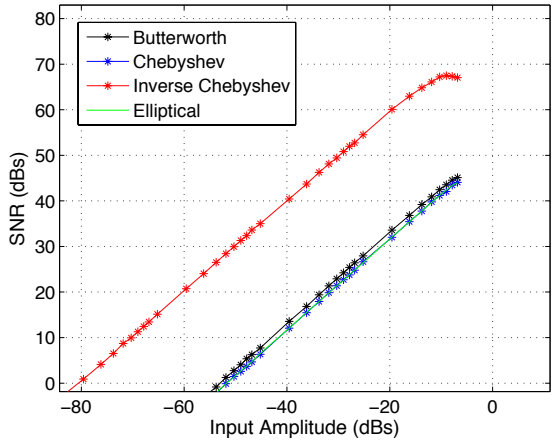



**Figure 110: SNR Plot, 6th-order EF Topology**

## 4.5 Implementation

The designed 4th-order digital VBP Σ–Δ modulators are implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit. The universal clock of the Xilinx® SpartanTM-3 Development Kit is 66 MHz. Hence, the resulting clock frequencies are 33MHz and 16.5MHz for the 2P and 4P modulators' individual paths respectively. In Table

18, the chosen parameters for the designed modulators are listed. The resulting feedforward and feedback coefficients are given in Table 19 and Table 20.

**Table 18: Chosen Design Parameters**

| Design Specs. | Butterworth | Chebyshev | Inv. Chebyshev | Elliptical |
|---|---|---|---|---|
| **Centre-Frequency** | 0.2 | 0.2 | 0.2 | 0.2 |
| **Bandwidth** | 0.02 | 0.02 | 0.004 | 0.02 |
| **PBA** | - | 1 dB | - | 1 dB |
| **SBA** | - | - | 60 dB | 80 dB |

**Table 19: Resulting Feedforward Coefficients**

| Loop-Filter | | $K_1$ | $K_2$ | $K_3$ | $K_4$ |
|---|---|---|---|---|---|
| **Butterworth** | OF | 0.0549 | -0.2099 | 0. 55 | -0.1628 |
| | EF | 0.0549 | -0.2099 | 0.1557 | -0.1628 |
| ***Chebyshev*** | OF | 0.0406 | -0.1548 | 0.1133 | - .1175 |
| | EF | 0.0406 | -0.1548 | 0.1 3 | -0.1175 |
| ***Inv. Chebyshev*** | OF | 0.5753 | 2 1182 | 1.0852 | -0.8250 |
| | EF | 0.5753 | -2.1182 | 1.0852 | -0.8250 |
| ***Elliptical*** | OF | 0.0406 | -0.1548 | 0.1133 | -0.1175 |
| | EF | 0.0406 | -0.1548 | 0.1133 | -0.1175 |

**Table 20: Resulting Feedback Coefficients**

| Loop-Filter | | $L_1$ | $L_2$ | $L_3$ | $L_4$ |
|---|---|---|---|---|---|
| **Butterworth** | OF | -1.2385 | 2.3835 | -1.2385 | 1 |
| | EF | -1.1836 | 2.1736 | -1.0828 | 0.8372 |
| ***Chebyshev*** | OF | -1.2385 | 2.3835 | -1.2385 | 1 |
| | EF | -1.1980 | 2.2287 | -1.1252 | 0.8825 |
| ***Inv. Chebyshev*** | OF | -1.2361 | 2.38 7 | -1.2361 | 1 |
| | EF | -0.6608 | 0.2635 | -0. 5 8 | 0.1750 |
| ***Elliptical*** | OF | -1.2385 | 2.3835 | -1.2385 | 1 |
| | EF | -1.1980 | 2.2287 | -1.1252 | 0.8825 |

Fixed-point arithmetic is chosen and the circuits are excited by a 16-bit single sinusoidal input signal. A one-bit quantizer is employed and the output data of the VBP Σ–Δ modulators are saved in the RAM. Thereafter, the data is read via RS232 connection and processed in Matlab. No decimation filter is built in the FPGA; instead the decimation filter is applied within the Matlab routines. The experimental set-up is shown in Figure 111.

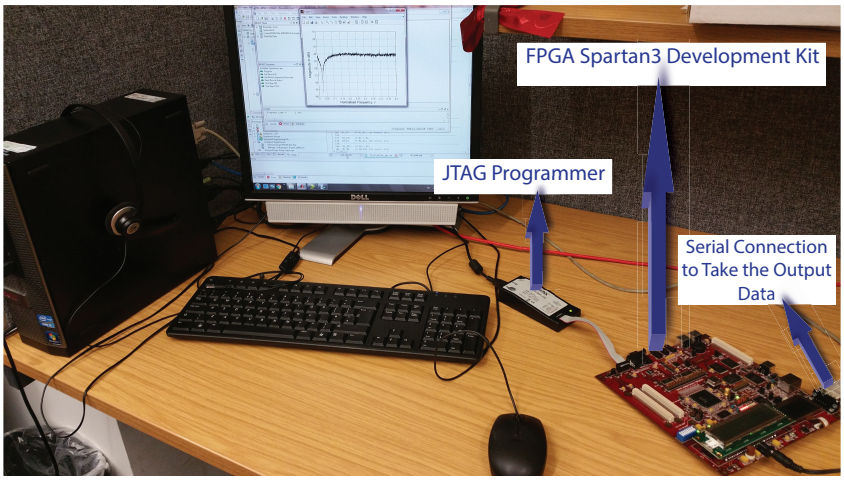



**Figure 111: Experimental Set-up**

Dither is used to randomize the tonal response of the Σ-Δ modulators. A 16-bit Fibonacci Linear Feedback Shift Register (LFSR) is built because of its relatively white output spectrum. As depicted in Figure 112, -70dB of white noise is obtained for normalized frequencies above 0.055.

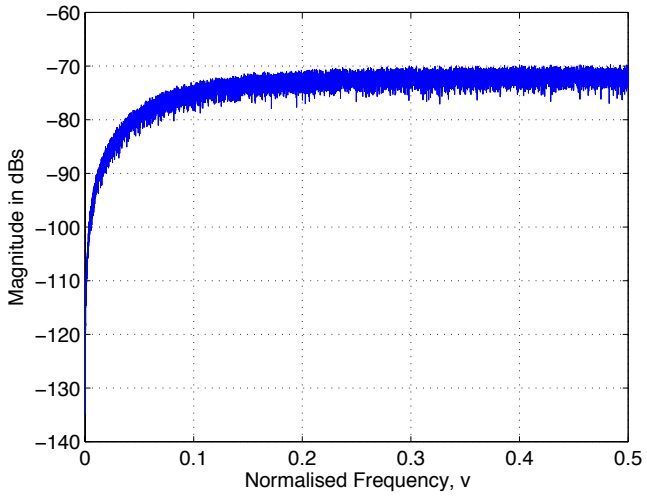



**Figure 112: LFSR Output Plot**

### 4.5.1 Fixed Point Arithmetic

Finite wordlengths are applied to coefficients by rounding. Simulations are iteratively repeated to determine the optimum wordlength in order to acquire loop-filters with suitable noise-shaping characteristics. The fractional resolution is chosen to be 16-bits. Note that the decimal part of the number is represented by extra bits such as *sD.15-bits* where *s* is the sign bit, *D* is

the number of the decimal bits and the 15-bits represent the fractional part of the number. As seen in Figure 113, the use of 15-bits of fractional resolution provides very comparable results with the ideal case for both the EF and OF topologies.

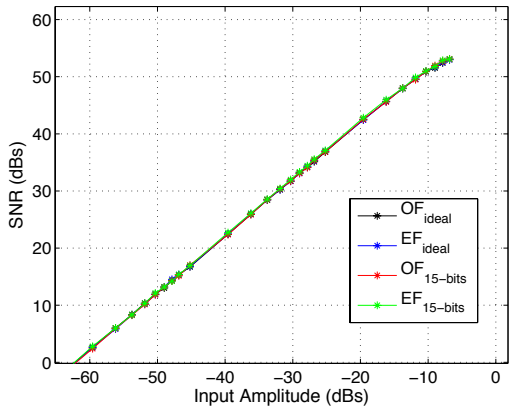



**Figure 113: SNR Plot, 4th-order SP Σ–Δ modulators, Butterworth NTF, Centre Frequency = 0.2, BW =0.02, OSR = 64**

### 4.5.2 Design Bottleneck

In the design of any digital circuits, the multipliers require quite large areas and lead to long propagation delays. Therefore, any attempt to discard or minimize the multiplication blocks will end up in faster Σ-Δ modulators. Substantial savings from the feedback multipliers have already been achieved for the OF topology. This is accomplished with the proper design of the loop-filter such that the numerator of the NTF is only feedback coefficient dependent.

On the other hand, the SNR of the Σ-Δ modulator highly depends on the in-band noise that is suppressed by the NTF numerator. At the system level, it is obvious that the feedforward coefficients, $K_m$s, do not affect the resonant performance of the NTF of the OF topology. They only affect the location of the poles. If their wordlengths are reduced to a number where the poles remain within the unit-circle, namely in the stable region, the feedforward multipliers will result in faster circuits. However for the EF topology both the feedback and feedforward coefficients determine the zeros. Therefore any attempt to further reduce the wordlength of the feedback and/or feedforward coefficients leads to poor SNR as depicted in Figure 114.

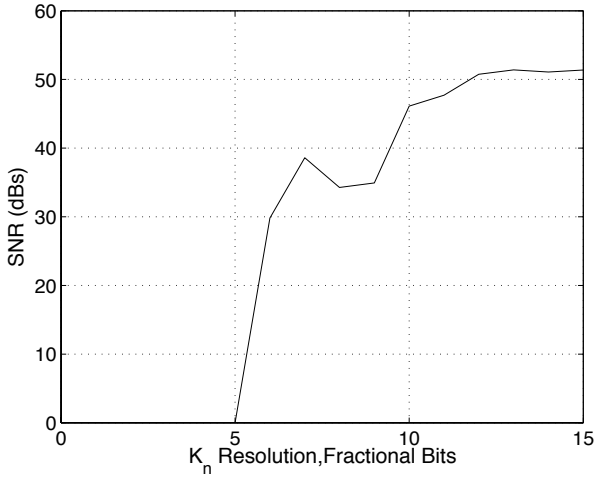



**Figure 114: SNR Plot versus Feedforward Coefficient Resolution, EF Topology, 4th-order SP Σ–Δ modulator Butterworth NTF, Centre Frequency = 0.2, BW =0.02 OSR = 64**

Again, iterative simulations are performed to decide the resolution of these coefficients for the OF topology. After all, it is observed that 8-bits of resolution for the feedforward coefficients of the OF topology gives fairly good results. Simulations revealed that fractional resolution below 7-bits may cause strong in-band tones and can lead up to instability even if the poles are still in the stable region. The relationships between the SNR and feedforward coefficients for different multi-path topologies are given in Figure 115-Figure 118. In Figure 115-Figure 118 SNR versus feedforward coefficient resolution plot is shown.

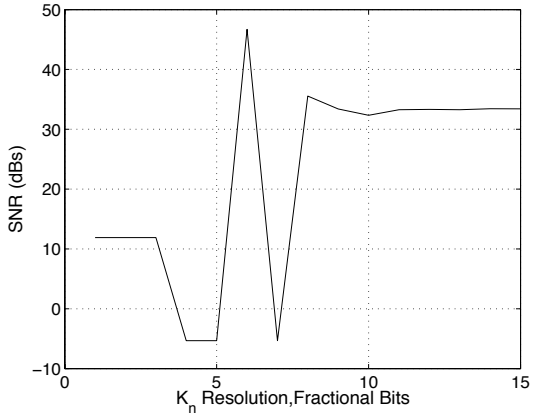



**Figure 115: SNR Plot versus Feedforward Coefficient Resolution, OF Topology, 4th-order SP Σ–Δ modulator Butterworth NTF, Centre Frequency = 0.2, BW =0.02 OSR = 64**

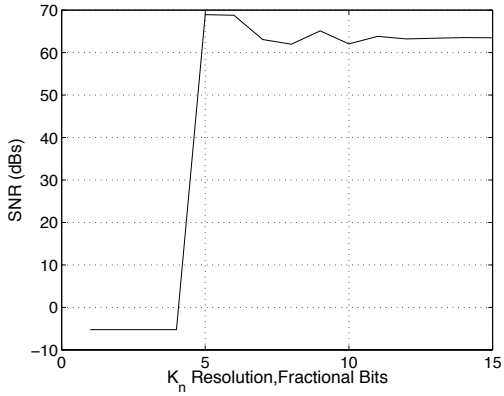



**Figure 116: SNR Plot versus Feedforward Coefficient Resolution, OF Topology, 4th-order 2P Σ–Δ Modulator, Chebyshev NTF, Centre Frequency = 0.2, BW =0.02, PBA = 1 dB OSR = 64**

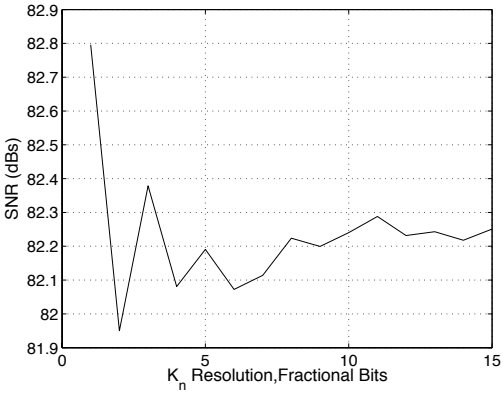



**Figure 117: SNR Plot versus Feedforward Coefficient Resolution, OF Topology, 4th-order 4P Σ–Δ Modulator, Inverse-Chebyshev NTF, Centre Frequency = 0.2, BW =0.02, SBA = 80 dB OSR = 64**

In Figure 118 and Figure 119, the pole zero locations are shown for the ideal case and for various resolution values. The zeros of the OF topology are not affected by the $K_m s$ whereas the poles clearly change their locations specifically for fractional resolution values below 7-bits. Moreover, one of the poles moves out of the unit-circle and may cause instability. This depends on the size of the shift outside the unit-circle as the modulator stability depends on the overall closed-loop transfer function.

In Figure 120, the pole-zero patterns of the EF topology to the various fractional resolution values is seen, again for the feedforward coefficients. As expected the feedforward coefficients alter the locations of the poles and zeros. It should be noted that if the chosen filter specifications are changed, the resolution of the feedback and feedforward coefficients needs to be reinvestigated.

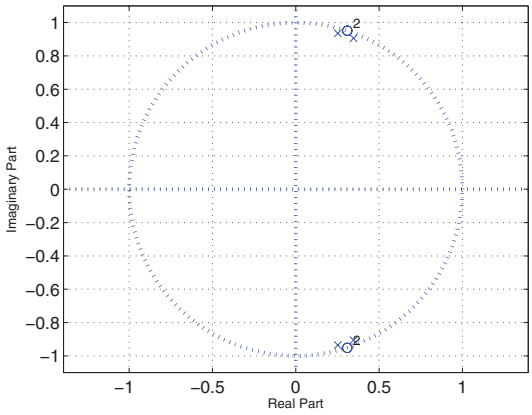
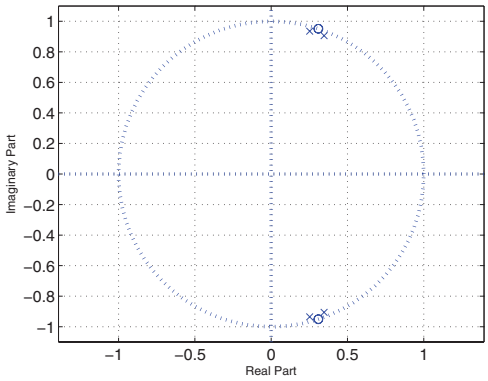
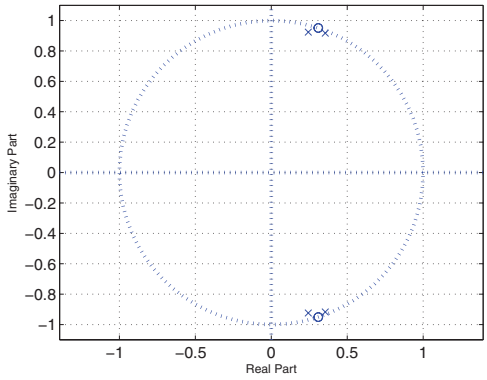


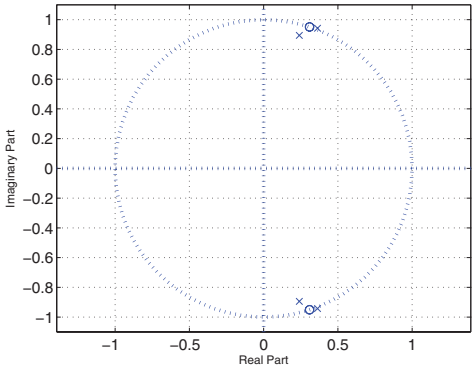

**Figure 118: Pole Zero Map, Ideal Case, 4th-order SP Σ–Δ modulator Chebyshev NTF, Centre Frequency = 0.2, BW =0.02, PBA = 1dB**




**a) 15-bits Fractional Resolution**

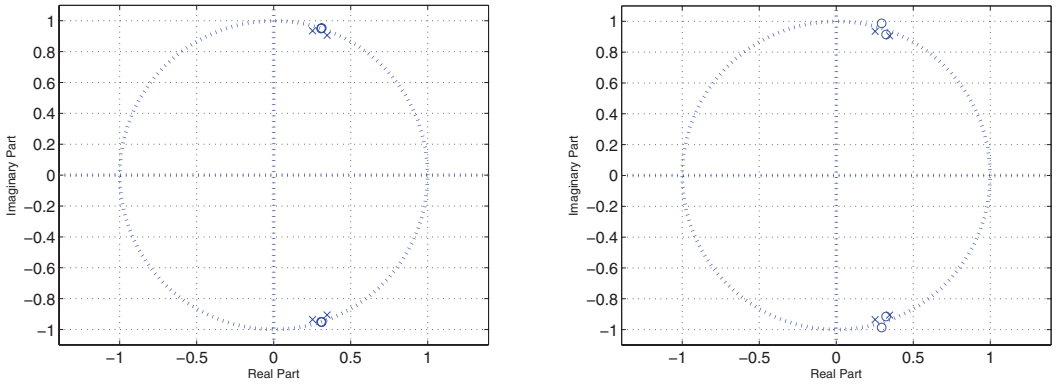



**b) 7-bits Fractional Resolution**

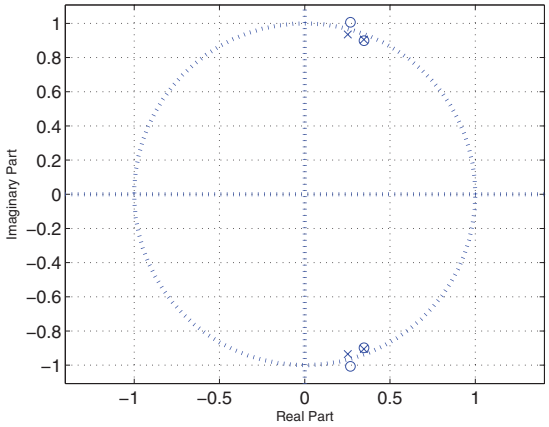



**c) 5-bits Fractional Resolution**

**Figure 119: Pole Zero Map for Various Resolution Values of Feedforward Coefficients ($K_s$), OF Topology, Chebyshev NTF, Centre Frequency = 0.2, BW =0.02, PBA = 1dB**




**a) 15-bits Fractional Resolution** **b) 7-bits Fractional Resolution**



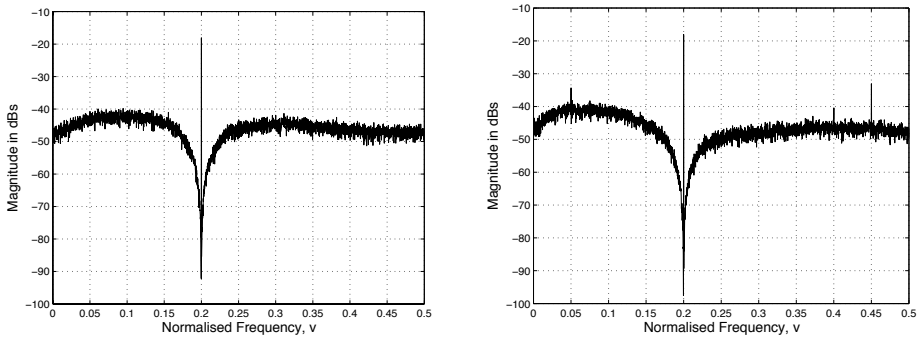

**b) 5-bits Fractional Resolution**

**Figure 120: Pole Zero Map for Various Resolution Values of Feedforward Coefficients ($K_s$), EF Topology, Chebyshev NTF, Centre Frequency = 0.2, BW =0.02, PBA = 1dB**

The Spartan-3 family has a dedicated array of 18x18 multipliers. Reducing the wordlength of the coefficients unfortunately does not affect the performance of the overall topology. Because the coefficients are actually inputs to the multipliers and they allocate the 18x18 multiplier blocks. Therefore the effects of reduced wordlength coefficients on the overall propagation delay and hardware reduction cannot be observed. A slight increase in speed may be achieved since the MSBs of the multipliers are not in calculation, as the MSBs require the longest calculation delay in a multiplier. Nevertheless, the universal clock frequencies of the Spartan-3 are fixed and the multiplier outputs are registered at every clock cycle. Therefore, the circuit speed cannot be improved in the VHDL implementations. The advantage of reduced wordlengths of the feedforward coefficients would be a huge benefit when it comes to integrated circuit implementations.

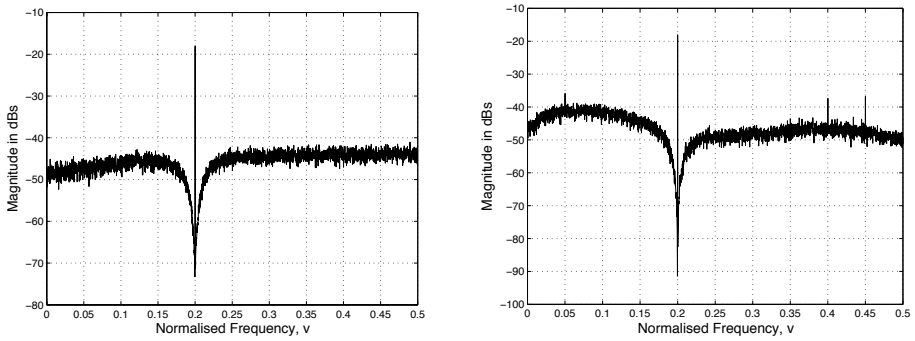
### 4.5.3 Implementation Results

The implementation results not only verify the node-equation method, but also support the behavioural-level analysis of the designed modulators. The output plots for some of the circuits are shown in Figure 121 and Figure 122. This data is saved in RAM and read through the RS232. The time-domain output data is processed within the MATLAB routines and its frequency spectrum is obtained.




**a)2P** **b)4P**

**Figure 121: The OF Topology, Butterworth Loop-Filter**




**a)SP** **b)4P**

**Figure 122: The EF Topology, Chebyshev Loop-Filter**

As clearly observed, the 4P topologies have deeper notches in comparison to their SP and 2P counterparts. Obviously, the 2P topologies' notches are deeper when compared to their SP counterparts. This is due to the relaxed path frequencies. All the multipliers and adders of the TI topologies are clocked with a lower clock frequency; hence the propagation delay does not affect the circuit performance. However, for the SP-topologies, the propagation delay causes data-loss therefore degrading the noise-shaping performance.

Moreover, the provided mathematical model of the quantization tones for the TI topologies clearly works. Generally, the 4P topologies are more likely to produce these quantization tones.

In Table 21 and Table 22, the behavioural-level simulations and implementation results for the SNR values are compared. These tables are for an overall OSR of 64. Note that for the 2-path topologies, the individual path OSR is 32 and for the 4-topologies the individual path OSR is 16.

**Table 21: Simulated SNRs, Behavioural Results**

| Loop-Filter | Topology | SP | 2-Path | 4-Path |
|---|---|---|---|---|
| **Butterworth** | OF-16 bits | 42 dB | 55 dB | 67 dB |
| | OF- 8 bits | 41 dB | 56 dB | 67 dB |
| | EF-16 bits | 41 dB | 55 dB | 65 dB |
| ***Chebyshev*** | OF-16 bits | 40 dB | 55 dB | 67 dB |
| | OF- 8 bits | 42 dB | 57 dB | 68 dB |
| | EF-16 bits | 41 dB | 54 dB | 67 dB |
| ***Inv. Chebyshev*** | OF-16 bits | 64 dB | 72 dB | 72 dB |
| | OF- 8 bits | 64 dB | 72 dB | 72 dB |
| | EF-16 bits | 64 dB | 72 dB | 72 dB |
| ***Elliptical*** | OF-16 bits | 40 dB | 55 dB | 67 dB |
| | OF- 8 bits | 42 dB | 57 dB | 68 dB |
| | EF-16 bits | 40 dB | 55 dB | 64 dB |

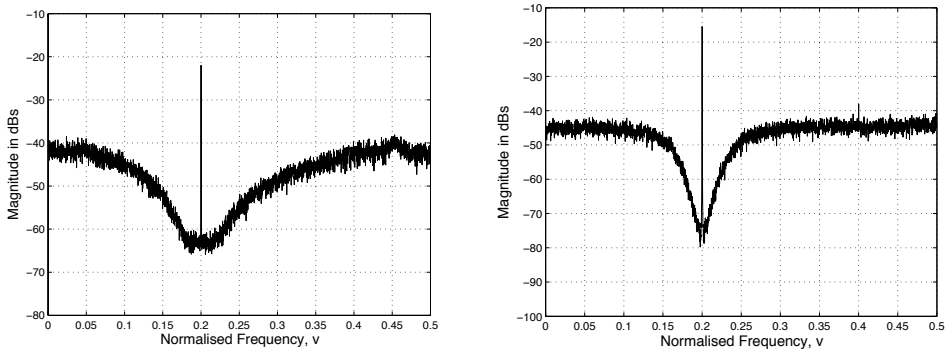
**Table 22: Measured SNRs, Behavioural Results**

| Loop-Filter | Topology | SP | 2-Path | 4-Path |
|---|---|---|---|---|
| **Butterworth** | OF-16 bits | 41 dB | 58 dB | 69 dB |
| | OF- 8 bits | 45 dB | 57 dB | 50 dB |
| | EF-16 bits | 45 dB | 58 dB | 67 dB |
| ***Chebyshev*** | OF-16 bits | 40 dB | 54 dB | 65 dB |
| | OF- 8 bits | 42 dB | 58 dB | 62 dB |
| | EF-16 bits | 40 dB | 55 dB | 60 dB |
| ***Inv. Chebyshev*** | OF-16 bits | 63 dB | 64 dB | 68 dB |
| | OF- 8 bits | 60 dB | 42 dB | 66 dB |
| | EF-16 bits | 22 dB | 4 dB | 6 dB |
| ***Elliptical*** | OF-16 bits | 40 dB | 55 dB | 60 dB |
| | OF- 8 bits | 42 dB | 58 dB | 59 dB |
| | EF-16 bits | 42 dB | 55 dB | 52 dB |

Another substantial finding from the implementation results is that the Inverse-Chebyshev filter causes low-quality notches for the EF topology as depicted in Figure 123-Figure 125. As seen, the out-of band noise level matches well with the OF topology. However the in-band noise floor is elevated. It is attributed to the aggressive nature of the designed Inverse-

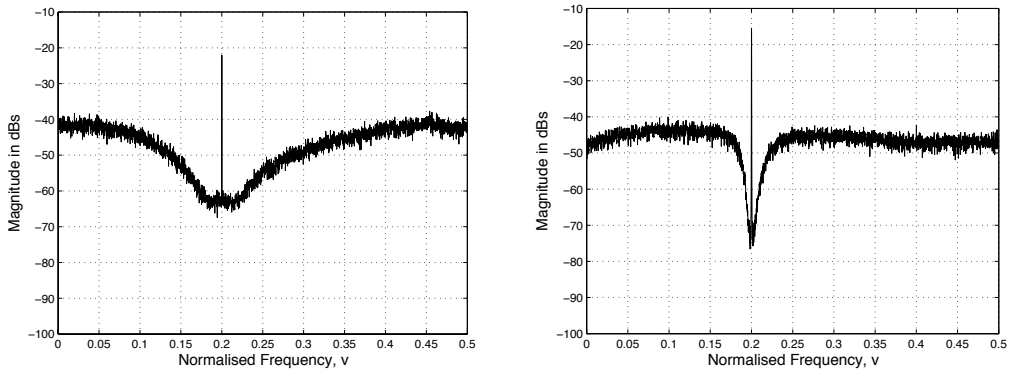
Chebyshev filter. The Inverse-Chebyshev NTF is designed for a bandwidth of 0.04 to acquire high resolution. As it has the narrowest bandwidth when compared to the other filters, the finite wordlength deteriorates its resonant frequencies more than the other filters.

It should be reminded that the finite wordlength of feedback and feedforward coefficients of the EF topology have a combined effect on the resonant frequency. While the OF topology's resonant frequencies are independent of its feedforward coefficients' resolution. As seen from Figure 123 - Figure 125, 4P and 2P topologies result in deeper notch for the OF topology compared to their SP counterparts due to the relaxed internal clocks. However, the finite wordlength of the feedback and feedforward coefficients of the EF topology impairs all SP, 2P and 4P topologies' resonant behaviour of the EF topology. Once again, it is shown that the designed OF topology is more appropriate to implement VBP Σ–Δ modulators.



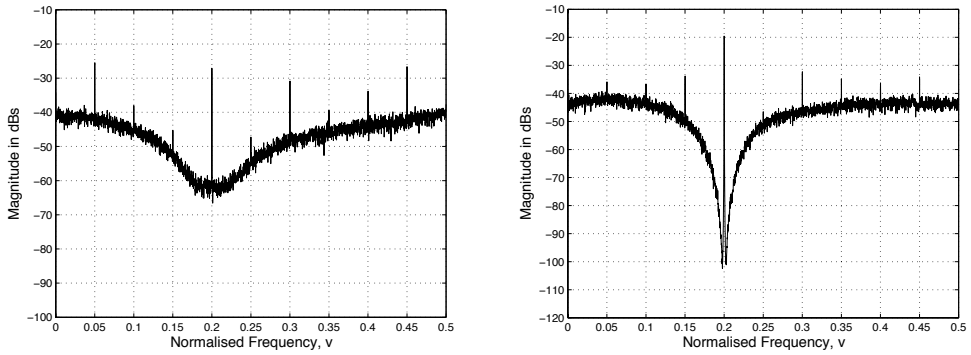

**a)EF** **b)OF**

**Figure 123:Output Plots of the SP topology for Inverse- Chebyshev Loop-Filter**




**a)EF** **b)OF**

**Figure 124:Output Plots of the 2P topology for Inverse- Chebyshev Loop-Filter**




**a)EF** **b)OF**

**Figure 125:Output Plots of the 4P topology for Inverse- Chebyshev Loop-Filter**

## 4.6 Hardware Complexity of the D/A VBP Σ–Δ Modulators

In Section 3.4, the hardware complexity of the A/D VBP Σ–Δ modulators is discussed comparing the topologies and the implementation techniques. The general rule is that the TI topologies utilize $P$x$N_{ad}$ adders and $P$x$N_{mul}$ multipliers where $N_{ad}$ is the number of the adders and $N_{mul}$ is the number of the multipliers of the SP counterpart of the TI topology. It was also mentioned in Section 3.4 that designers could save all of the $P$x$N_{ad}$ adders if the TI topology is implemented using current-mode circuits for A/D VBP Σ–Δ modulators. However in digital world this advice does not apply. Therefore, the OF and EF topologies are investigated to save coefficients as well as the wordlength of the coefficients of the D/A VBP Σ–Δ modulators.

To summarize the outcomes of hardware reduction of the D/A VBP Σ–Δ modulators, using the FBFF TDA loop-filter the OF topology saves $P$x$L/2$ feedback coefficients where $L$ is the order of the modulator. Moreover, depending on the NTF coefficients' values feedforward coefficients' resolution can be reduced by simulations. For detailed explanations please go to Sections 4.2.1, 4.2.2 and 4.5.2.

In Table 23 and Table 24 the allocated FPGA sources are listed for the 4$^{th}$-order OF and EF topologies. As expected, the utilized LUTs and flip-flop slices are around the same range. This is due to the fact that, both topologies employ the same loop-filter structure and their coefficients do not exceed 18-bits of resolution. However, the OF topology uses 4x$L/2$ less multipliers when compared to the EF topology.

**Table 23: The Allocated FPGA Sources for The EF Topologies**

| | FPGA Sources | Butterworth | Chebyshev | Inverse Chebyshev | Elliptical |
|---|---|---|---|---|---|
| **SP** | # Slice Flip Flops | 87 / 40,960 ~ 1% | 87 / 40,960 ~ 1% | 124 / 40,960 ~ 1% | 86 / 40,960 ~ 1% |
| | # LUTs | 168 / 40,960 ~ 1% | 168 / 40,960 ~ 1% | 175 / 40,960 ~ 1% | 164 / 40,960 ~ 1% |
| | # Multipliers 18x18 | 8 / 40 = 20% | 8 / 40 = 20% | 8 / 40 = 20% | 8 / 40 = 20% |
| **2P** | # Slice Flip Flops | 234 / 40,960 ~ 1% | 232 / 40,960 ~ 1% | 247 / 40,960 ~ 1% | 215 / 40,960 ~ 1% |
| | # LUTs | 501 / 40,960 ~ 1% | 499 / 40,960 ~ 1% | 666 / 40,960 ~ 1% | 448 / 40,960 ~ 1% |
| | # Multipliers 18x18 | 16/ 40 = 40% | 16/ 40 = 40% | 16/ 40 = 40% | 16/ 40 = 40% |
| **4P** | # Slice Flip Flops | 278 / 40,960 ~ 1% | 276 / 40,960 ~ 1% | 294 / 40,960 ~ 1% | 276 / 40,960 ~ 1% |
| | # LUTs | 833 / 40,960 ~ 2% | 831 / 40,960 ~ 2% | 2501 / 40,960 ~ 6% | 831 / 40,960 ~ 2% |
| | # Multipliers 18x18 | 32/ 40 = 80% | 32/ 40 = 80% | 32/ 40 = 80% | 32/ 40 = 80% |

**Table 24: The Allocated FPGA Sources for The OF Topologies**

| | FPGA Sources | Butterworth | Chebyshev | Inverse Chebyshev | Elliptical |
|---|---|---|---|---|---|
| **SP** | # Slice Flip Flops | 107 / 40,960 ~ 1% | 99 / 40,960 ~ 1% | 149 / 40,960 ~ 1% | 101 / 40,960 ~ 1% |
| | # LUTs | 156 / 40,960 ~ 1% | 140 / 40,960 ~ 1% | 198 / 40,960 ~ 1% | 147 / 40,960 ~ 1% |
| | # Multipliers 18x18 | 6 / 40 = 15% | 6 / 40 = 15% | 6 / 40 = 15% | 6 / 40 = 15% |
| **2P** | # Slice Flip Flops | 215 / 40,960 ~ 1% | 213 / 40,960 ~ 1% | 213 / 40,960 ~ 1% | 215 / 40,960 ~ 1% |
| | # LUTs | 448 / 40,960 ~ 1% | 446 / 40,960 ~ 1% | 446 / 40,960 ~ 1% | 448 / 40,960 ~ 1% |
| | # Multipliers 18x18 | 12/ 40 = 30% | 12 / 40 = 30% | 12/ 40 = 30% | 16/ 40 = 30% |
| **4P** | # Slice Flip Flops | 259 / 40,960 ~ 1% | 257 / 40,960 ~ 1% | 284 / 40,960 ~ 1% | 257 / 40,960 ~ 1% |
| | # LUTs | 725 / 40,960 ~ 1% | 723 / 40,960 ~ 1% | 994 / 40,960 ~ 2% | 723 / 40,960 ~ 1% |
| | # Multipliers 18x18 | 24/ 40 = 60% | 24 / 40 = 60% | 24/ 40 = 60% | 24 / 40 = 60% |

## 4.7 A Tunable and Reconfigurable D/A VBP Σ–Δ Modulator

A second-order tunable and reconfigurable D/A VBP Σ–Δ modulator is designed and implemented. The topology is highly flexible providing a set of choices for designers. In Figure 126, the block diagram of the designed modulator is given. Basically it is a second order 2P OF topology and is built using the developed design methodology in Section 3.3.6.

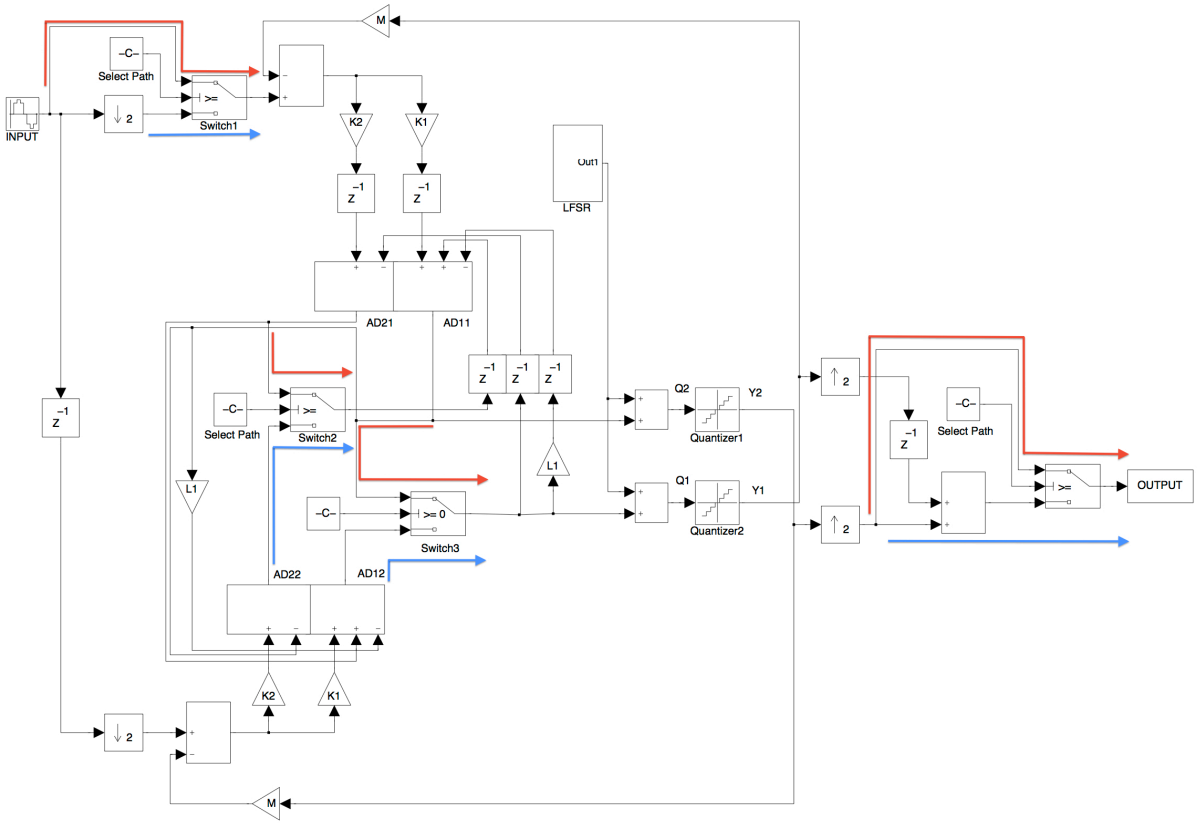



**Figure 126: 2nd-order Tunable and Reconfigurable D/A VBP Σ–Δ modulator**

By programming the switches, the topology can either operate as a SP VBP Σ–Δ modulator or as a 2P TI VBP Σ–Δ modulator. If the red route is selected, the topology is a SP VBP Σ–Δ modulator, whereas if the blue route is selected, the topology is a 2P VBP Σ–Δ modulator. The configurability of the SP and 2P options makes the circuit suitable for multi-band systems. For instance, if a narrow-band operation is required the user can select the SP option hence saving power. On the other hand, the 2P option can double the conversion band without doubling the clock frequency therefore enabling relatively wider band signal conversion. It should be noted that both SP and 2P options perform the same symbolic NTF given in (85).

$$NTF_{flex}(z) = \frac{1 + L_1 z^{-1} + z^{-2}}{1 + (K_1 + L_1) z^{-1} + (K_2 + L_2) z^{-2}} \tag{85}$$

As mentioned earlier, the node-equation method shares the data samples between the subsequent and/or adjacent channels. Hence, the required delayers are reduced by half for a 2P design. The switches in the configurable topology basically determine which path utilizes the delayers. It should be noted that, in Simulink the sample time is set internally for each block. However when implemented in VHDL, the clock frequencies of the cross-connected delayers and the LFSR block are also determined by switches. Since the circuit is implemented on Xilinx® SpartanTM-3 Development Kit, the universal clock frequency of 66 MHz is applied to the SP topology. When the 2P option is activated, each internal path is clocked at 33 MHz resulting in an overall clock frequency of 66 MHz. If more clock options are available within the overall system, the designer can implement them as needed by using multiplexers [102]. At the present, clock glitches due to switches are not an issue. This is because the Σ–Δ modulator resets itself, if an on-going path-mode is changed. If the modulator does not reset but continues to operate when the path-mode is changed, stability issues may occur. This is due to the fact that the D/A Σ–Δ modulators' stability is highly affected by the initial conditions [103]. Moreover, the transient response of the newly selected path-topology will be influenced by the steady state response of the formerly operating path-topology. The state-space equations need to be analysed if path selection is needed without reseting the circuit.

The NTF given in (85**)** is applied to Butterworth coefficients. The normalised bandwidth of the NTF is selected to be 0.02. The centre frequency is swept between [0.03-0.47] with a 0.01 step size. This results in 45 different centre frequencies, hence 45 different filter coefficients. The fractional resolution of the coefficients is chosen to be 15-bits. These filter coefficients $K_1$, $K_2$ and $L_1$ are saved in a look up table in VHDL. At the moment the designer can select the centre-frequency from this look up table and synthesize the circuit. However, for future work the Σ–Δ modulator can calculate the coefficients itself as the Butterworth function can be solved by VHDL coding. This in return will enable the user to enter the centre-frequency and bandwidth of the modulator from a chosen peripheral.

To sum-up, the user can select the path-mode and centre-frequency of the Σ–Δ modulator modulator by external signals that can be determined by peripherals. At the moment, these control signals are attained internally within the VHDL code as the output data is being saved in the RAM. Therefore for a chosen path-mode and centre frequency, the circuit is synthesized on the board. The output data is saved in the RAM and read through RS232. The read output data is processed by MATLAB routines. The resulting output plots of the second-order tunable and reconfigurable D/A Σ–Δ modulator for different centre frequencies are depicted in Figure 127 and Figure 128. The outputs are obtained when the Σ–Δ modulators are excited by zero input. The limit cycle tones observed at 0.2 and 0.4 result from the repetitive output responses of Σ–Δ modulators as they are being excited by a steady input. DC inputs tend to produce limit cycle tones since the Σ–Δ modulators are actually finite-state machines.

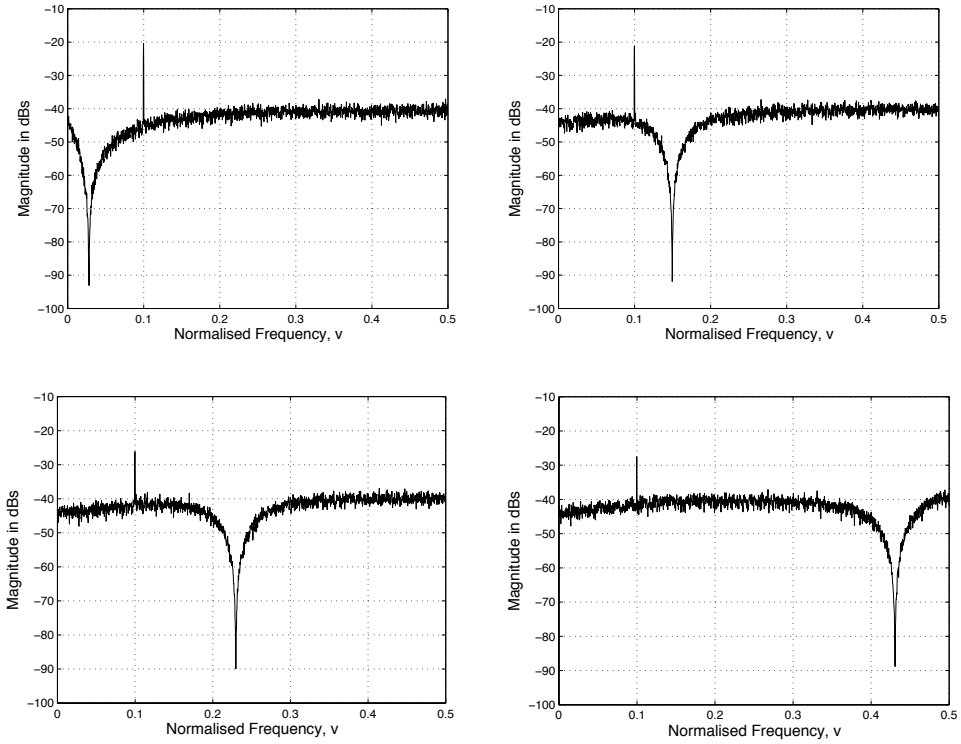



**Figure 127: Output Plots for Different Centre Frequencies, SP Topology is Activated**

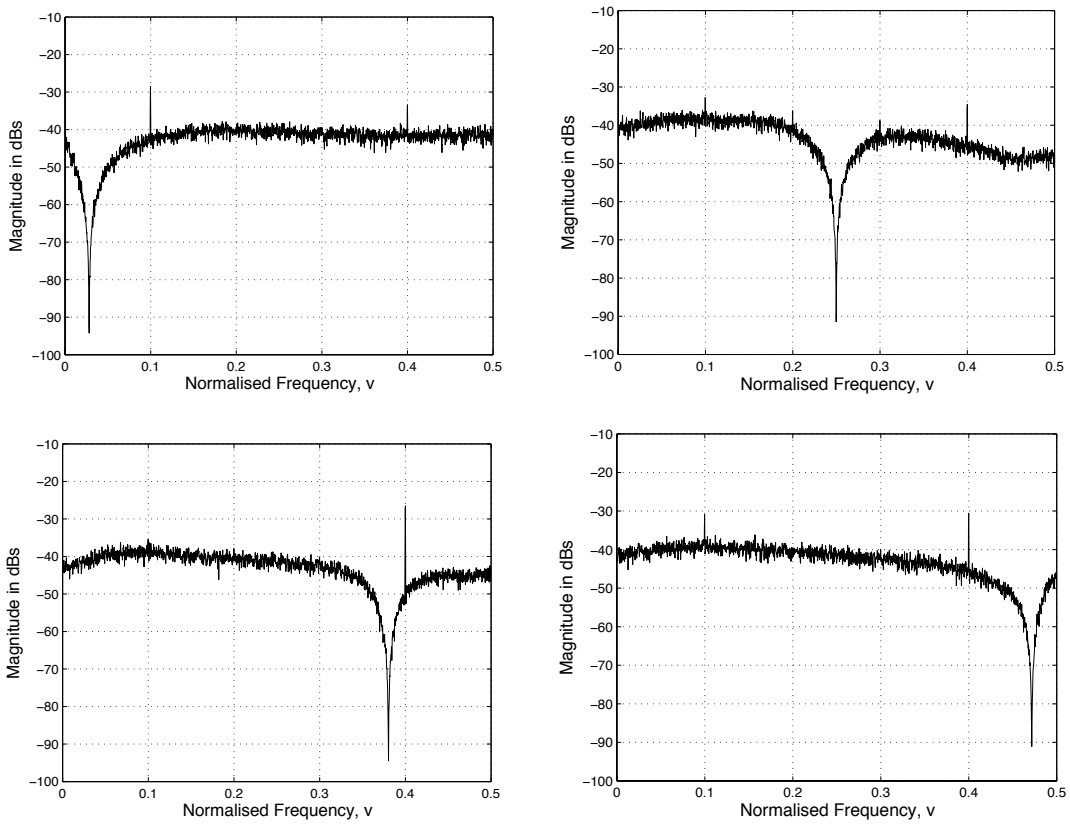



**Figure 128: Output Plots for Different Centre Frequencies, 2P Topology is Activated**

In conclusion a flexible, tunable and reconfigurable topology is designed and implemented. This circuit supports the main theme of this thesis which involved the design, evaluation and implementation of generalized TI VBP Σ–Δ modulators. Moreover, the inherent flexibility of the topology made it possible for designers to utilise different types of filters in order to maintain stable outputs for a wide range of centre frequencies.

## 4.8 Conclusion

The node equation method was applied in this chapter to the design and implement of D/A VBP Σ–Δ modulators that can accomplish noise-shaping for any centre frequency and bandwidth.

Two fundamental Σ-Δ modulator topologies are discussed. Contrary to the LP Σ-Δ modulator applications, it is shown that the OF topology is well suited for BP Σ-Δ modulators due to the BS NTF resonant behaviour. The OF topology not only discards some of the feedback

multipliers of the loop-filter but also works relatively well with lower resolution of the feedforward coefficients.

In addition, the developed mathematical model for quantization tones produced in A/D VBP Σ–Δ modulators is further extended to the D/A VBP Σ–Δ modulators. Since these topologies' input signal is also quantized, tones caused by the input-amplitude's finite wordlength are investigated. It is concluded that the resulting tones are masked by the NTF therefore they do not cause any stability and/or SNR deterioration. In the meantime, the internal path finite wordlength is also examined. Rather than causing distinct tones at the output spectrum, internal path truncation causes increased noise floor or noise-shaping degradation. The recursive nature of Σ–Δ modulators whitens the expected distinct quantization tones as they are being added up and multiplied to each other.

The $2^{nd}$-, $4^{th}$- and $6^{th}$-order of SP, 2P and 4P generalized D/A VBP Σ–Δ modulators are designed for the OF and EF topologies. These structures are capable of employing Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters. The filter performances and resulting SNR values are also discussed. Once again, detailed behavioural-level simulations show that Inverse-Chebyshev filters provide the highest SNR values.

The $4^{th}$-order SP, 2P and 4P topologies are implemented on the Xilinx® SpartanTM-3 Development Kit. The output plots of these circuits and the behavioural-level design simulations are compared. However, it is observed that the EF topology does not support high SNR values when Inverse-Chebyshev filters are employed.

A second order tunable and reconfigurable VBP Σ–Δ modulator is designed and implemented. The topology can operate either on a SP mode or a 2-path mode enabling multi-band operation through the same D/A converter. Moreover the designer can select 45 different centre-frequencies each being placed with a step size of 0.01 to each other and within a normalised frequency range of [0.03 0.47]. This design supports the idea of highly flexible and tunable VBP Σ–Δ modulators are realisable. To the best knowledge of the author, this is the first reconfigurable TI topology reported in the open literature.

# Chapter 5. Graphical User Interface

A user-friendly design tool created in the MATLAB/Simulink environment has been developed to accelerate the design, analysis and evaluation of single-stage and TI VBP Σ-Δ modulators.

Σ-Δ modulators' mathematical analysis depends on white-noise assumption and extensive simulations examine the stability. Hence, from the designer perspective, it is very handy to have a toolbox or GUI for the intended work. A toolbox or GUI helps users to design a wide range of TI VBP Σ-Δ modulators. It helps them to evaluate these modulators and make fairly swift comparisons. The GUI also motivates the users in the area who do not have any expertise of code writing.

There are various design tools in the literature focusing on different problems. In [104], the pole-zero optimization of LP modulator's NTF is applied to obtain stable Σ-Δ modulators that are capable to produce higher SNRs. In [105], LP and bandpass Σ-Δ modulators' behavioural level analysis are combined in a single GUI. In [106], a toolbox is constructed to speed up the design of continuous-time bandpass Σ-Δ modulators.

In this study, a novel GUI is built where the designed A/D and D/A SP and TI VBP Σ-Δ modulators' Simulink models cooperate with the Matlab simulation codes. This GUI is the first example of its kind as it enables users to study not only SP but also 2-path and 4path TI structures. The user can select conversion type, topology, loop-filter type, order, path number and OSR to plot the output frequency and SNR responses. The GUI is constructed using Matlab R2010b 64-bit.

## 5.1 Installation

Since the GUI is built in a Matlab environment there is no need to install an application to the computer. The provided *"VBP SDMs"* folder should be copied somewhere in the computer, preferably to the root directory as it is faster for Matlab to compute. The folder's size is 2.6 MB.

Thereafter the *"GUI_VBP.fig"* file should be executed with Matlab GUIDE. This can be done easily by following the steps listed below.

1. Open Matlab.
2. Open the directory of the folder in Matlab.
3. Double click on *"GUI_VBP.fig"*.

Or simply right click on *"GUI_VBP.fig"* and select Open in Matlab. The GUI menu should be seen on screen as depicted in Figure 129.

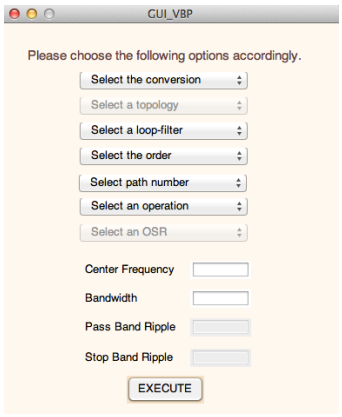



**Figure 129: GUI Menu**

## 5.2 The Menu Bar

The menu is designed to be as basic as possible. The user selects the conversion type by *'Select the conversion'* bar in the first place. If the *'Analog to Digital'* conversion is selected, the GUI simulates the CR-RFB topologies only for the ideal-case. If the '*Digital to Analog'* conversion is selected, the GUI can simulate both the EF and OF topologies for 15-bits of fractional resolution.

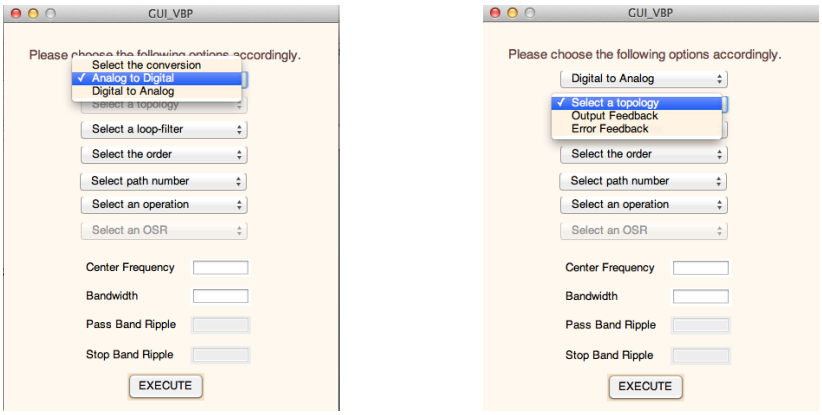



**Figure 130: Selecting the Conversion**

Thereafter, the loop-filter needs to be selected from the options: Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical. Once the order and path number are also chosen, the GUI is able to decide on the overall structure.

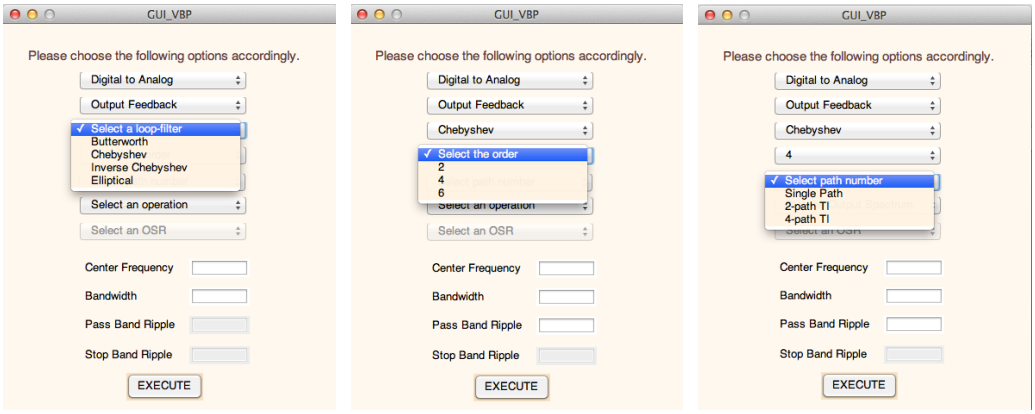



**Figure 131: Selecting the Specifications**

There are four editable text boxes within the GUI where the user can input data and determine the NTF centre frequency, bandwidth and pass-band/stop-band attenuation parameters. The GUI calculates the filter coefficients depending on these data.

The GUI performs two operations. It can plot the output response in the frequency domain or the SNR versus input amplitude response of the selected modulator. If the SNR plot is selected, the user must choose an OSR within the specified values of 8, 16, 32, 64,128 and 256.

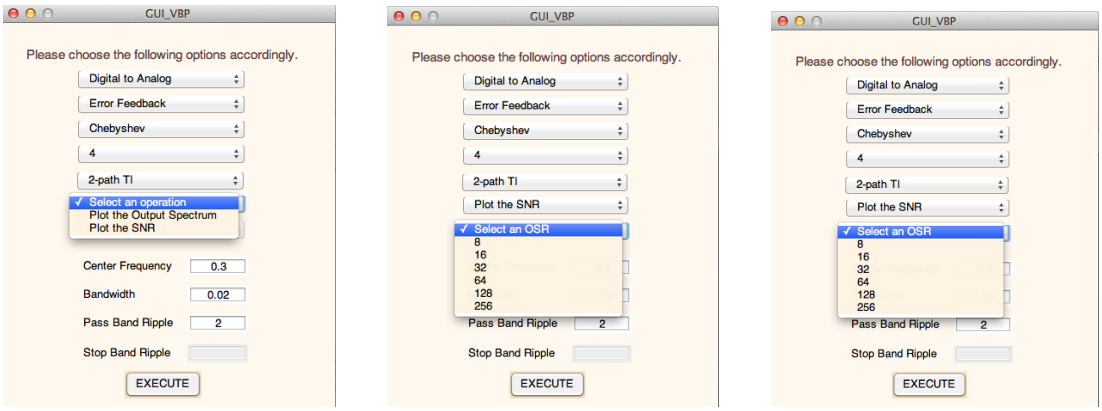



**Figure 132: Selecting the Specifications**

If all the inputs are provided for the GUI the *'EXECUTE'* push button functions properly. Otherwise an error message appears on the screen saying *'You must enter all required inputs'* as shown in Figure 133. Note that the Matlab Command Window also produces an error summary as the GUI does not function properly in the case of a missing input.

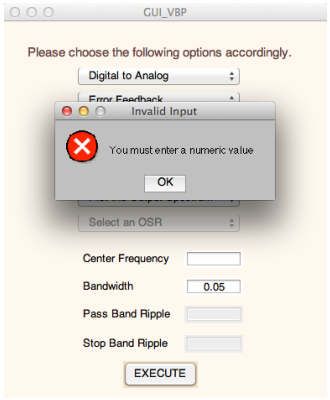



**Figure 133: Error Message**

## 5.3 Outputs

The output spectrum is plotted within a frequency interval of [0 0.5]. If A/D conversion is chosen, the input amplitude equals to 0.5 and the dithering amplitude equals to 0.05. The *'Plot the Output Spectrum'* simulation takes around 15 seconds of running time. The selected topology's Simulink model opens during simulation and it closes when the simulation is completed. In this way the user can also confirm that the chosen topology is being simulated.

If the user wishes to display the determined coefficients of the selected topology, this can be done by simply using the *'display (variable)'* command of MATLAB. For instance, to display the $K_1$ coefficient, the user needs to write *'display (K1)'* on the command window.

The Simulink blocks' names are generated such as:

*'Conversion_TI.Path_Topology_Order.mdl'*.

Refer to

Table 25 for all Simulink blocks' names. Moreover, one of the GUI output plot is given in Figure 134. Note that the title of the plot is set such that the selected conversion, topology, order and filter are defined.

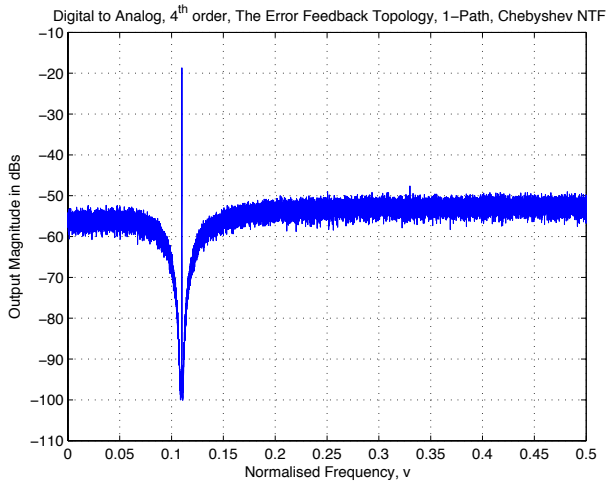



**Figure 134: GUI Output Plot**

The SNR calculation takes around 40 minutes of running time. Depending on the order and topology, the simulation time varies. The generation of the SNR plot takes considerably more time when compared to the production of the output spectrum. This is due to the fact that the SNR values are calculated individually for 48 input amplitude values. Therefore the DR of the modulator, maximum and minimum achievable SNR values are depicted in a single plot. In Figure 135, an SNR plot is given. Again the title of the plot is set such that the selected conversion, topology, order and filter are defined.

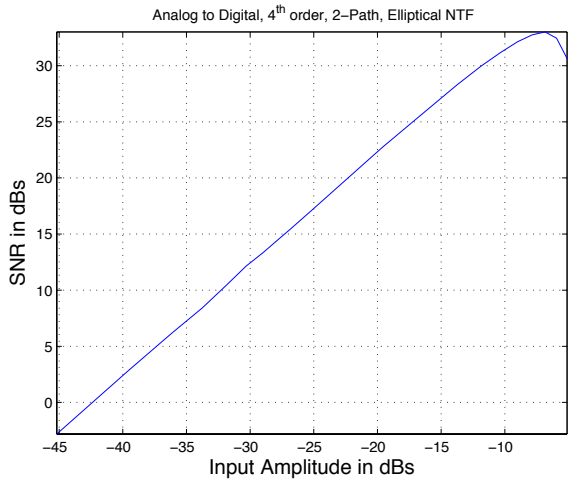



**Figure 135: GUI SNR Plot**

**Table 25: Simulink Blocks' Names**

| Simulink Block Name | Conversion | Path | Topology | Order |
|---|---|---|---|---|
| **DAC_SP_OF_2nd.mdl** | D/A | SP | OF | 2 |
| **DAC_SP_OF_4th.mdl** | D/A | SP | OF | 4 |
| **DAC_SP_OF_6th.mdl** | D/A | SP | OF | 6 |
| **DAC_SP_EF_2nd.mdl** | D/A | SP | EF | 2 |
| **DAC_SP_EF_4th.mdl** | D/A | SP | EF | 4 |
| **DAC_SP_EF_6th.mdl** | D/A | SP | EF | 6 |
| **AD_SP_RESFB_2nd.mdl** | A/D | SP | CR-RFB | 2 |
| **AD_SP_RESFB_4th.mdl** | A/D | SP | CR-RFB | 4 |
| **AD_SP_RESFB_4th.mdl** | A/D | SP | CR-RFB | 6 |
| **DAC_TI2_OF_2nd.mdl** | D/A | 2P | OF | 2 |
| **DAC_TI2_OF_4th.mdl** | D/A | 2P | OF | 4 |
| **DAC_TI2_OF_6th.mdl** | D/A | 2P | OF | 6 |
| **DAC_TI2_EF_2nd.mdl** | D/A | 2P | EF | 2 |
| **DAC_TI2_EF_4th.mdl** | D/A | 2P | EF | 4 |
| **DAC_TI2_EF_6th.mdl** | D/A | 2P | EF | 6 |
| **AD_TI2_RESFB_2nd.mdl** | A/D | 2P | CR-RFB | 2 |
| **AD_TI2_RESFB_4th.mdl** | A/D | 2P | CR-RFB | 4 |
| **AD_TI2_RESFB_4th.mdl** | A/D | 2P | CR-RFB | 6 |

| | | | | |
|---|---|---|---|---|
| **DAC_TI4_OF_2nd.mdl** | D/A | 4P | OF | 2 |
| **DAC_ TI4_OF_4th.mdl** | D/A | 4P | OF | 4 |
| **DAC_ TI4_OF_6th.mdl** | D/A | 4P | OF | 6 |
| **DAC_ TI4_EF_2nd.mdl** | D/A | 4P | EF | 2 |
| **DAC_ TI4_EF_4th.mdl** | D/A | 4P | EF | 4 |
| **DAC_ TI4_EF_6th.mdl** | D/A | 4P | EF | 6 |
| **AD_ TI4_RESFB_2nd.mdl** | A/D | 4P | CR-RFB | 2 |
| **AD_ TI4_RESFB_4th.mdl** | A/D | 4P | CR-RFB | 4 |
| **AD_ TI4_RESFB_4th.mdl** | A/D | 4P | CR-RFB | 6 |

## 5.4 Programmer Guide

This section covers some of the basics of the GUI's software hence providing an opportunity to the programmers to further develop the GUI and/or to build up their own simulation environment.

The GUI is formed from several subprograms. The main body of the GUI is the *'GUI.VBP.m'* file where all the input data are collected, the related loop-filter transfer function is calculated and the output is plotted. Moreover, if there is any missing input data or invalid input values, the error messages are produced in this file. The *'GUI.VBP.m'* file has its own comments inside the programmers guide, such that they have better understanding of the variable names and control flags.

**Loop-filter Transfer Function Calculation:** The noise transfer function is calculated by Matlab using the input data. The NTF calculation is performed regardless of the selected topology. The given codes below are for the four different NTFs.

```
%Butterworth NTF
[num, den] = butter(order, [freq1, freq2], 'stop');
%Chebyshev NTF
[num, den] = cheby1(order, PBA, [freq1, freq2], 'stop');
%Inverse-Chebyshev NTF
[num, den] = cheby2(order, SBA, [freq1, freq2], 'stop');
%Elliptical NTF
[num, den] = ellip(order, PBA, SBA, [freq1, freq2], 'stop');
```

Once the NTF is obtained, it is normalized for causality of the loop-filter. Thereafter the loop-filter's transfer function is calculated accordingly. Since the CR-RFB topology is also an OF structure, there are two different loop-filter transfer functions regardless of the conversion selection. The loop-filter transfer function is calculated using the AWGN model and resulting equations are given in (87) and (89).

$$NTF_{OF}(z) = \frac{1}{1 + LF_{OF}(z)} \tag{86}$$

$$LF_{OF}(z) = \frac{1 - NTF_{OF}(z)}{NTF_{OF}(z)} = \frac{num_{NTF} - den_{NTF}}{num_{NTF}} \tag{87}$$

$$NTF_{EF}(z) = 1 - LF_{EF}(z) \tag{88}$$

$$LF_{EF}(z) = 1 - NTF_{EF}(z) = \frac{den_{NTF} - num_{NTF}}{den_{NTF}} \tag{89}$$

The Matlab functions to calculate the loop-filter transfer function are listed in Table 26.

**Table 26: Functions for Loop-filter Transfer Function Calculation**

| Function File | Corresponding Operation |
|---|---|
| **butter_BP_Hz.m** | Butterworth, the EF topology's loop-filter |
| **cheb_BP_Hz.m** | Chebyshev, the EF topology's loop-filter |
| **cheb2_BP_Hz.m** | Inverse-Chebyshev, the EF topology's loop-filter |
| **ellip_BP_Hz.m** | Elliptical, the EF topology's loop-filter |
| **butter_BP_LF.m** | Butterworth, the OF topology's loop-filter |
| **cheb_BP_LF.m** | Chebyshev, the OF topology's loop-filter |
| **cheb2_BP_LF.m** | Inverse-Chebyshev, the OF topology's loop-filter |
| **ellip_BP_LF.m** | Elliptical, the OF topology's loop-filter |

**det_block.m :** This function returns the selected Simulink block's name. The block name is not global, so the user cannot display it on the command window. However, as mentioned earlier, the selected topology is opened during simulation and is closed before the plot appears.

**det_variables.m:** The input and dither amplitude values for the output spectrum plot and fractional wordlength of the D/A modulators' coefficients are set by this function. If the programmer is interested in investigating the finite wordlength effect of the D/A modulator blocks or the modulators' responses to different input and dither amplitudes, the variables inside this function need to be changed. Variable names are listed in Table 27. Note that dither noise amplitude only affects the A/D modulators' performance since a LFSR block with fixed amplitude of output noise is employed for the D/A modulators as covered in Section 4.5. To understand the fixed-point arithmetic used for the D/A modulators go to Section 4.5.1.

**Table 27: Variable Names Used in det_variables.m**

| Variable Name | Corresponding Datum |
|---|---|
| **INPUT** | Input signal's amplitude |
| **KDit** | Dither Noise amplitude |
| **R** | Input signal's fractional wordlength |
| **RK** | Feedforward Coefficients' fractional wordlength |
| **RL** | Feedback Coefficients' fractional wordlength |

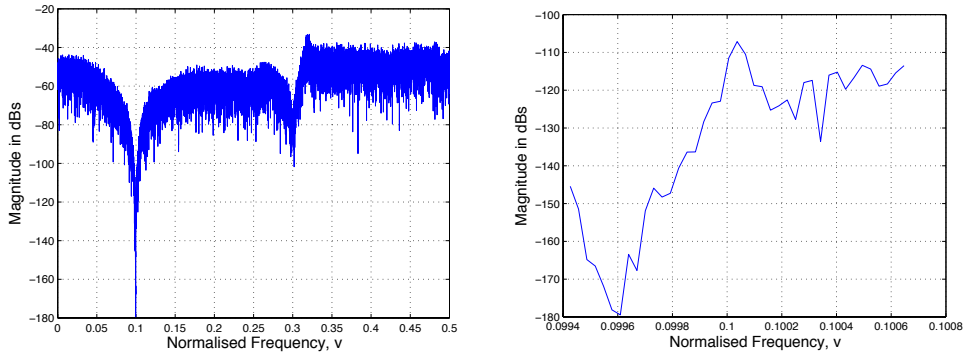
**det_coef.m:** This function does not return any value. All the coefficients are calculated within this function and are set to be global for the Simulink blocks to use, Hence the user can display them on the command window. This function calls nine different functions. Those are responsible for calculating the individual topology's coefficients. These functions are listed in Table 28. Note that the employed coefficient equations are given in appendices and calculated using the AWGN model for the quantizer behaviour.

**Table 28: Functions called by det_coef.m**

| Function Name | Corresponding Operation |
|---|---|
| `ad_resfb_2nd_coef.m` | A/D, 2nd-order, the CR-RFB Topology coefficients' calculation |
| `ad_resfb_4th_coef.m` | A/D, 4th-order, the CR-RFB Topology coefficients' calculation |
| `ad_resfb_6th_coef.m` | A/D, 6th-order, the CR-RFB Topology coefficients' calculation |
| `dac_OF_2nd_coef.m` | D/A, 2nd-order, the OF Topology coefficients' calculation |
| `dac_OF_4th_coef.m` | D/A, 4th-order, the OF Topology coefficients' calculation |
| `dac_OF_6th_coef.m` | D/A, 6th-order, the OF Topology coefficients' calculation |
| `dac_EF_2nd_coef.m` | D/A, 2nd-order, the EF Topology coefficients' calculation |
| `dac_EF_4th_coef.m` | D/A, 4th-order, the EF Topology coefficients' calculation |
| `dac_EF_6th_coef.m` | D/A, 6th-order, the EF Topology coefficients' calculation |

**PlotOut.m:** This function is called if the *'Plot the Output Spectrum'* operation is chosen. Basically the function simulates the chosen Simulink block. A Hanning window is applied to the time-domain output data for $2^{20}$ FFT points. The negative frequency of the output spectrum is excluded and the remaining positive frequency output spectrum is plotted on the screen. The comments within the function provide easy-to-follow explanations for the programmers.

**SNRplot.m:** This function is called if the *'Plot the SNR'* operation is chosen. First of all, the function calculates the noise floor within the signal-band by simply applying zero-input to the selected modulator. The noise floor is then averaged around the input signal's frequency for a very narrow band; around 0.0012. Thereafter the iterative simulations start.




**a) Zero-Input Response** **b) The in-band Noise To Be Averaged**

**Figure 136: Average Noise Calculation Plots**

**Iterative Simulations of SNR Values:**

**1.** The input amplitude is increased in every iteration. The selected input amplitude interval is [0.00001 1.2]. This interval covers the DR of the all modulators.

**2.** The input and output signals' spectrums are calculated in every iteration. Once again, a Hanning window for $2^{20}$ FFT points is employed.

**3.** The averaged noise floor obtained with zero-input signal is replaced with the input signal. Finally, the overall in-band noise is calculated according to the chosen OSR and path-number.

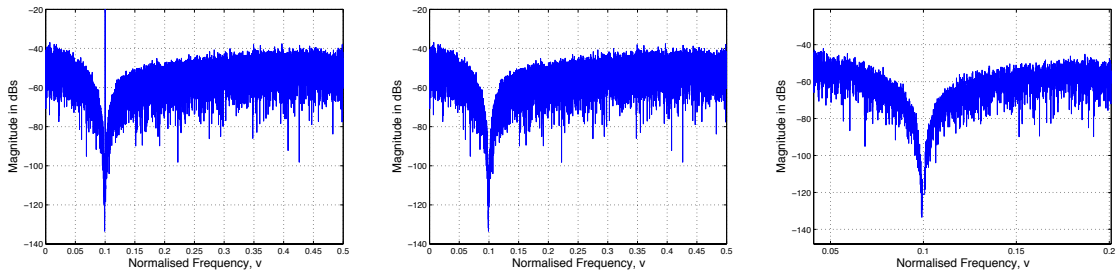



**Figure 137: Clearing The Input Signal**

**4.** The SNR value is calculated since the in-band noise and signal amplitude values are known.

Once iterations are completed, the SNR array is put through another process where the negative SNR values are excluded hence providing the user to observe the positive SNR values versus input signal amplitude plot. In this way it is easy to distinguish the overall DR value as well.

**set_title.m:** This function returns the title of the plot where the selected conversion type, topology, order and the filter are written.

## 5.5 Conclusion

As a final product of the overall work, 27 topologies are wrapped up in a single GUI environment. The GUI enables the users to specify the centre frequency, bandwidth, pass-band/ stop-band attenuation parameters as well as the OSR value for a selected topology. The GUI combines 1857 lines of code to operate in the same environment.

The GUI serves the purpose of this thesis, as it enables the analysis of VBP Σ–Δ modulators for any centre frequency and bandwidth. It does not require any detailed knowledge of Σ–Δ modulators therefore enabling the beginners to simulate VBP Σ–Δ modulators. It also helps users to further their understanding of the TI VBP Σ–Δ modulators. In addition, for those who are willing to develop their own simulation routines and/or GUI environment, it has a well-structured code that is composed of sub-functions.

This GUI is a unique environment for the analysis of VBP Σ–Δ modulators. Moreover it is promising that the GUI itself can be extended to a toolbox where the user can employ different functions to form their own models and codes.

# Chapter 6. CONCLUDING REMARKS and RECOMMENDATIONS FOR FUTURE WORK

In this work, single-path and multi-path VBP Σ–Δ modulators are studied. The main motivation of the thesis was to design, evaluate and implement generalized TI VBP Σ–Δ modulators that can accomplish noise-shaping for a chosen design specifications such as the centre frequency, bandwidth, pass-band and stop-band attenuations. These generalized TI VBP Σ–Δ modulators have the ability to provide flexible structures where multi-band and/or multi-frequency systems can achieve data conversion through a single A/D and/or D/A converter. Moreover, their capacity to perform noise-shaping at the required centre frequency eliminates the passive circuitry of the conventional superheterodyne and homodyne receivers that use LP and BP Σ–Δ modulators. Excluding the passive circuitry such as mixers and filters makes it possible for the receiver to be integrated to the overall system at a higher level.

The study resulted in four publications listed below.

[1] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, *"Design and Evaluation of Time-Interleaved Variable Center-Frequency Sigma-Delta Modulators," DSP 2013,* Greece, July 2013

[2] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, *"Novel time-interleaved variable-center frequency sigma-delta modulators - design, analysis and critical evaluation," I2MTC 2013,* USA, May 2013

[3] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, *"Novel Time-Interleaved Variable Centre-Frequency, Single-Bit A/D and D/A Sigma-Delta Modulator Topologies," IMEKO 2013*, Spain, July 2013

[4] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, "*Design and implementation of novel FPGA based time- interleaved variable centre-frequency digital sigma-delta modulators", in ACTA IMEKO on,* vol. 4, no.1, pp.68-75, Feb 2015

In addition to the already published papers, three more papers are being written.

[5] I. Kalafat Kızılkaya, M. Al-Janabi, and I. Kale, "Hardware Reduction in The Implementation of Digital Variable-Banspass Time-Interleaved Sigma Delta Modulators", is ready to be submitted.

[6] A GUI paper is in progress.

[7] A paper on the reconfigureable and tunable 2nd-order D/A TI Sigma-Delta modulator will be written afterwards.

## 6.1 Concluding Remarks

In *Chapter 1*, the benefits of VBP Σ–Δ modulators were discussed. In addition, the fundamental aims of the thesis were explained as well as the limitations of conventional LP and BP Σ–Δ modulators. It was stated that Σ–Δ modulators utilize high OSRs to obtain higher SNRs. However, the use of high OSRs restricted the conversion bandwidth of conventional LP and BP Σ–Δ modulators to narrow-band applications. Hence, it was shown that the TI topologies offered an elegant situation as they employ P mutually cross-connected Σ–Δ modulators operating together in order to obtain a sampling frequency of $Pxf_s$, where $f_s$ is the individual path sampling frequency. Therefore, it was concluded that building generalized TI VBP Σ–Δ modulators not only provides flexibility but also offers a suitable solution to the narrow-band limitation of LP and BP Σ–Δ modulators.

It was demonstrated that noise-shaping at frequencies close to Nyquist or DC resulted in unequal shoulder gain levels if resonator-based NTFs were used. This may cause instability and/or ear-detectable noise. The unequal shoulder gain levels of the mid-band BP Σ–Δ modulators were overcome by applying different filtering types to the loop-filter such as the Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters. These filters also enable the designer to control the bandwidth, stop-band and pass-band attenuation parameters of the NTF.

In *Chapter 2*, the basic principles of data converters were explained. The sampling and the quantization operations were explained and their mathematical analysis was given. These two

blocks were deemed important as they formed the basis for conventional PCM converters. The underpinning principles of the Σ–Δ modulation technique as well as the noise-shaping and oversampling were explained and were shown to achieve high resolution i.e., high SNRs and high DRs. The system-level diagrams of single-path A/D and D/A based Σ–Δ modulators were also presented and discussed in Chapter 2.

After explaining the fundamentals of LP and BP Σ–Δ modulators, the motivations to design TI VBP Σ–Δ modulators were discussed. To do so, a detailed up-to-date literature review and discussion were given. The TI VBP Σ–Δ modulators were presented as suitable candidates for today's emerging technologies as they offered high resolution and relatively simple hardware whilst providing flexibility and higher integration-levels. The novelties and the developed contributions of this thesis were listed and detailed in Chapter 2. Finally Chapter 2 covered the performance metrics of evaluating the SNR, DR, stability and tonality of Σ–Δ modulators.

In *Chapter 3*, the detailed design, analysis, evaluation and comparison of A/D TI VBP Σ–Δ modulator topologies with possible applications in superheterodyne and homodyne receivers were presented. Generalised yet flexible TI VBP Σ–Δ modulator modulators were developed where the designer is able to specify the centre frequency bandwidth, stop-band and pass-band attenuations from a menu of filters. This in return provided:

a. More stable Σ-Δ modulator topologies,
b. Improved integration for IC circuits,
c. Improved SNR and DR.

The narrow band restriction was overcome by the time-interleaving technique thus enabling higher frequency conversion.

Thereafter, a step-by-step design method was provided that enables the design of generalized TI VBP Σ–Δ modulators. The main points are summarised below:

a. The user is able to select a generalized NTF that can accomplish $L^{th}$-order Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical noise shaping, where the NTF is applied

to a block filter in Simulink before choosing a topology. Therefore the filter coefficients and orders are determined to ensure adequate SNR and as well as stability.

b. A topology is selected to map the chosen NTF.
c. The node equation technique is applied accordingly for a chosen path-number.

In [20], the node-equation method to design TI LP Σ–Δ modulators developed. The node-equation method is an easy to apply technique resulting in simpler hardware when compared to the polyphase decomposition method. Therefore the node equation method was chosen for this work and was applied to VBP Σ–Δ modulators. This extension of the node-equation method enabled the design of multi-path VBP Σ–Δ modulators. It should be noted that polyphase decomposition of VBP Σ–Δ modulators especially for orders four and above is cumbersome and quite hard to solve. Even if done properly, each design specification would result in different TI topologies as their NTFs are changed. However, the node-equation method is relatively easy to apply to build-up generalized TI VBP Σ–Δ modulators. By simply changing the feedback and feedforward coefficients of the designed TI VBP Σ–Δ modulators, the designers can accomplish noise-shaping at a desired centre-frequency with the chosen design specifications.

In this thesis, the node-equation method was applied to two different topologies; the CI-FBFF and the CR-RFB. The main rationale for choosing these topologies was to compare the integrator-based and resonator-based structures. The CI-FBFF topology is formed of cascaded integrators with feedback and feedforward coefficients, whereas the CR-RFB topology is formed of cascaded resonators with local feedback coefficients. Both topologies were built for $2^{nd}$-, $4^{th}$-, $6^{th}$- and $8^{th}$- orders as well as for different path numbers such as the SP, 2-path and 4-path structures. Moreover Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical filters were applied to these generalized topologies. In Chapter 3, all structures are given. The CI-FBFF and the CR-RFB were compared in terms of their coefficients, SNRs, DRs and tonality.

The cascaded nature of the CI-FBFF topology resulted in signal accumulation at the internal nodes. Hence, the feedback and feedforward coefficients inevitably increase to balance this accumulation. Extensive simulations revealed that the CI-FBFF topology is not realizable for centre-frequencies [0.25 0.5] especially for $6^{th}$-order and above. However, the local feedbacks

of the CR-RFB topology prevent signal accumulation at the internal nodes therefore the coefficients do not exponentially increase.

Butterworth-based VBP Σ–Δ modulators were able to provide stable frequency responses for relatively wider bandwidths i.e., 0.1 of normalized bandwidth. On the other hand, Inverse-Chebyshev-based VBP Σ–Δ modulators with orders higher than 4 could easily go unstable for normalized bandwidths larger than 0.08. Elliptical and Chebyshev-based VBP Σ–Δ modulators actually produced stable outputs with quite strong out-of-band tones for relatively larger bandwidths when compared to Inverse-Chebyshev filters. Despite their narrow band restriction, Inverse-Chebyshev filters presented the highest SNR values due to their spread zeros over the signal band.

Moreover, the SP, 2-path and 4-path structures were compared in terms of their immunity to non-idealities. First of all, their non-idealities were defined and modelled at the behavioural level. Thereafter simulations were run to identify the tolerable percentage of non-idealities for each structure. The SP CI-FBFF and the CR-RFB topologies were investigated for non-ideal conditions by using non-ideal integrators and resonators. Higher-order SP CI-FBFF topologies were more sensitive to non-idealities as they could tolerate 0.1 % of non-idealties. On the other hand, the CR-RFB topologies were shown to be more immune to non-ideal resonators. The TI structures were investigated by using non-ideal adders as the node-equation method distributed the resonators and integrators over the interleaving paths. It was reported that due to their cross-connectivity, non-ideal adders resulted in an increased level of noise floor. Hence the TI structures' immunity to non-idealities is not dependent on the SP topology they are derived from. The path-number and filter order are the defining parameters for the TI structures.

Finally, the tonal behaviour of quantizers when excited by single-sinusoids was mathematically modelled to calculate the amplitudes and frequencies of the tones. This mathematical model was named as the sawtooth quantization noise model. The calculated results were compared with the simulation results. It was shown that, the derived model can calculate the amplitudes and the frequencies of these tones if the input signal's frequency is not irrational. A summary of the sawtooth quantization noise model can be found in Page 88.

Moreover, the SP and multi-path structures' tonal behaviour was investigated separately. The sawtooth quantization noise model was applied to SP VBP Σ–Δ modulators and further extended for the TI VBP Σ–Δ modulators.

The quantization tones seen in the SP topologies were also observed in TI topologies. Yet the shifted copies of these tones were also observed. More importantly, they were folded back into the signal band thereby resulting in in-band tones. In [81], these tones were observed and referred to as limit-cycle tones caused by the path mismatches. However, it was proved that these tones could be observed even for the ideal-case simulations. These tones' frequencies were also calculated by the sawtooth quantization noise model that was extended for the TI topologies.

In *Chapter 4*, generalized D/A TI VBP Σ–Δ modulators were designed, built and simulated. The provided design technique in Chapter 3 was applied to $2^{nd}$-, $4^{th}$- and $6^{th}$-order EF and OF topologies. Their 2-path and 4-path counterparts were also built. Once again these D/A TI VBP Σ–Δ modulators could perform Butterworth, Chebyshev, Inverse-Chebyshev and Elliptical noise-shaping.

Firstly, the EF and the OF topologies were compared. With the proper design of the loop-filter, the multipliers of the OF topology can be reduced by $P \times L/2$ where $P$ is the path number and $L$ is the order of the loop-filter. The mathematical analysis of this reduction was also given in Chapter 4. It was demonstrated that half of the feedback coefficients of the EF topology were eliminated. In addition, some particular frequencies are listed in Table 17 where a further reduction in the number of multipliers for the EF topology is possible.

Secondly, the developed sawtooth quantization noise model was applied to D/A SP and TI VBP Σ–Δ modulators. The results differed from the A/D VBP Σ–Δ modulators as the finite coefficients of the D/A VBP Σ–Δ modulators caused noise-floor elevation. It was also depicted that the discrete tones caused by the input signal's finite wordlength were masked by the NTF. In conclusion, the quantization tones' frequencies can be calculated as in A/D VBP Σ–Δ modulators since the 1-bit quantizer is the only source of these tones. However, it must be realised that the increased noise floor may diminish some of these expected tones.

Thereafter the designed $4^{th}$-order topologies were implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit for a chosen set of design spesifications. These spesifications and the resulting filter coefficients were listed in Table 18, Table 19 and Table 20. The universal clock of the Xilinx® SpartanTM-3 Development Kit was 66 MHz. Hence, the resulting clock frequencies were 33MHz and 16.5MHz for the 2-path and 4-path modulators' individual paths respectively.

Fixed-point arithmetic was applied to the implemented circuits. The fractional resolution of the coefficients was chosen to be 15-bits. Moreover, it was shown that the OF topology's feedforward coefficients' resolution could be reduced to 8-bits, where the SNR and DR varied by 2-4 dBs whilst maintaining modulator stability.

The implemented circuit performance and simulation results were listed in Table 21 and Table 22. The Inverse-Chebyshev filter could not perform high SNR values for the EF circuits whilst providing the expected SNRs for the OF circuits. It was attributed to the aggressive nature of the designed Inverse-Chebyshev filter. The feedback and feedforward coefficients of the EF topology had a combined effect on the resonant frequency resolution. Hence, the narrow-band design of the Inverse-Chebyshev filter is more likely to deteriorate in noise-shaping performance when non-idealties apply.

Finally, a tunable and reconfigurable $2^{nd}$-oder 2P VBP $\Sigma$–$\Delta$ modulator was designed and implemented. The topology offered a highly flexible set of choices for designers. It could either operate either in SP mode or 2-path mode enabling multi-band implementations on a single D/A VBP $\Sigma$–$\Delta$ modulator. Moreover, the NTF can be tuned to 45 different centre frequencies in intervals of 0.01 within the normalised frequency range [0.03 0.47]. Therefore, the designed circuits can be utilized for multi-band and multi-frequency systems.

In *Chapter 5*, a novel GUI was built where the designed A/D and D/A SP and TI VBP the $\Sigma$-$\Delta$ modulators' Simulink models could work with with the Matlab simulation routines developed by the author. The user can select conversion type, topology, loop-filter type, order, path number and OSR to plot the output frequency and SNR responses. A user guide was given in Chapter 5 for the designed GUI in which the installation and user options were explained.

Moreover, the sub-functions and overall Matlab code was clarified for those who are interested in adding more functions to this tool.

## 6.2 Recommendations for Future Work

A wide range of VBP Σ–Δ modulators were designed and evaluated in this study. The comparisons were made to cover the fundamental design aspects of the Σ–Δ modulators such as the building block type, applied filter type, loop-filter order and topology type. Based on the experience of this research, the following suggestions are presented for future work.

- Implement the A/D TI VBP Σ–Δ modulators in SC circuits to realize fully tunable and reconfigurable circuits.
- Apply the provided design methodology of the TI VBP Σ–Δ modulators to MASH topologies to build up higher-order Σ–Δ modulators. Hence, the accumulation resulting from the cascaded nature of the CI-FBFF topology can be avoided.
- Implement higher-orders tunable and reconfigurable D/A VBP Σ–Δ modulators.
- Design and implement higher path numbers for the configurable D/A VBP Σ–Δ modulators. This is to switch from single- to P-path for the same topology.
- Mathematically analyse the tunable and reconfigurable D/A VBP Σ–Δ modulators. Hence switching without reset may be possible.

## Appendix A

The designed A/D CI-FBFF VBP Σ-Δ modulators are depicted in this Appendix. Their symbolic NTFs are also provided.

### Symbolic NTF for 2nd-order CI-FBFF Topology:

$$NTF_{CI-FBFF,2^{nd}}(z) = \frac{1+(K_1-2)z^{-1}+z^{-2}}{1+L_1z^{-1}+L_2z^{-2}} \quad (90)$$

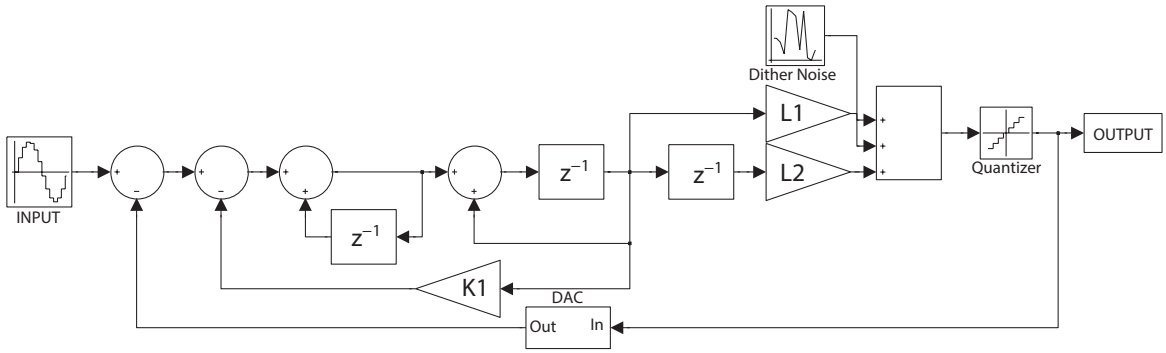



**Figure 138: 2nd-order, SP CI-FBFF Topology**

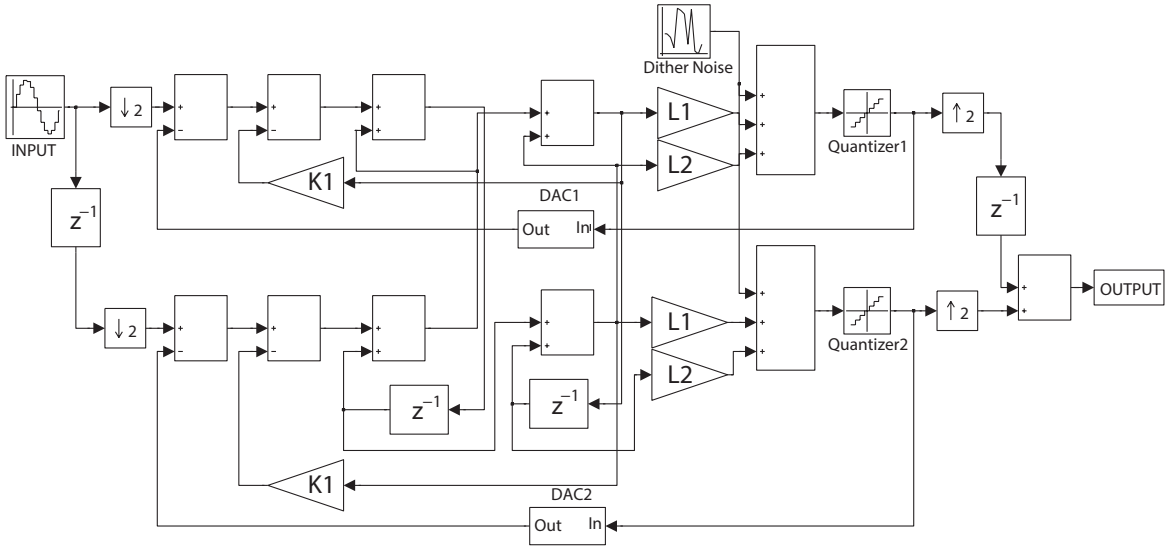



**Figure 139: 2nd-order, 2-path CI-FBFF Topology**

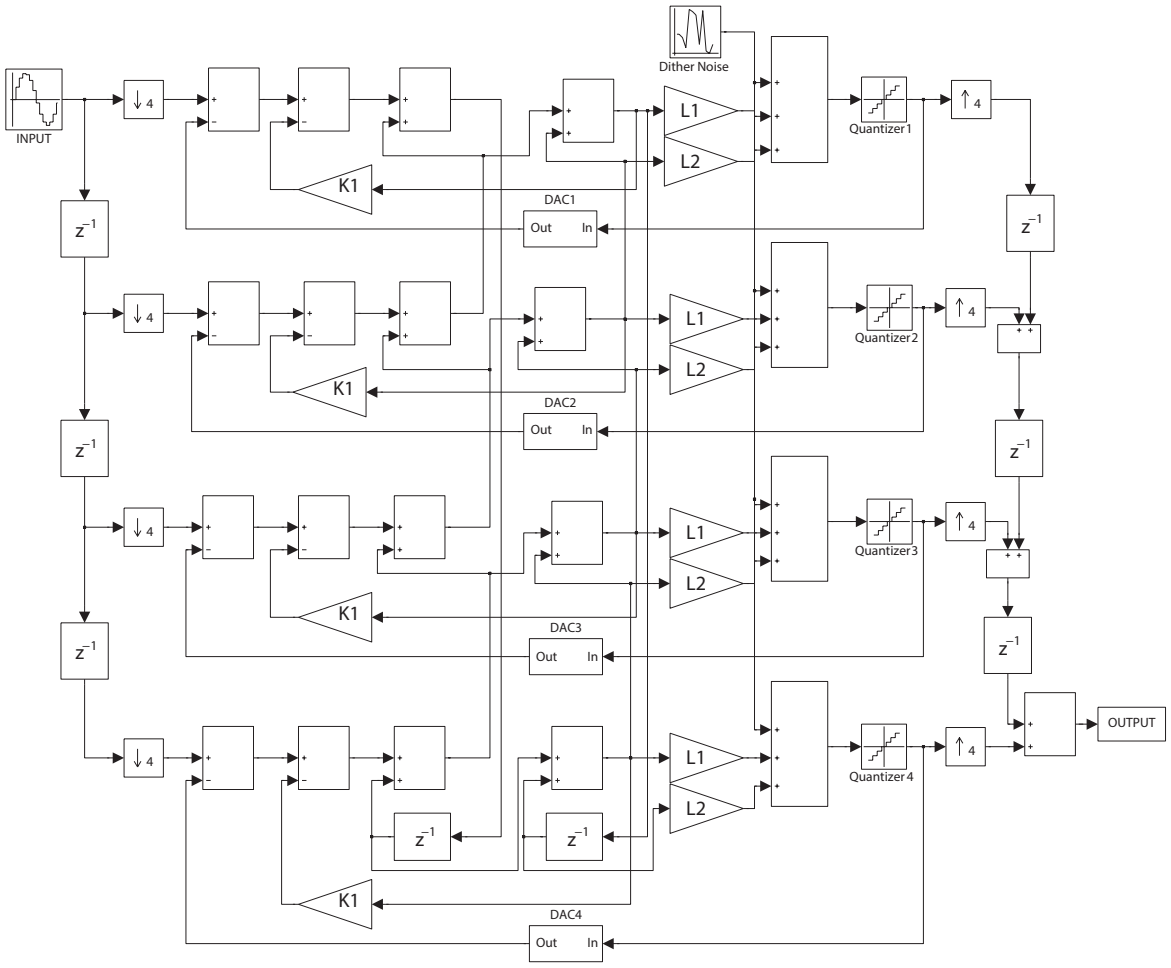



**Figure 140: 2nd-order, 4-path CI-FBFF Topology**

**Symbolic NTF for 4th-order CI-FBFF Topology:**

$$NTF_{CI-FBFF,4^{th}}(z)=\frac{1+(K_1-4)z^{-1}+(K_2-2K_1+6)z^{-2}+(K_3+K_1-K_2-4)z^{-3}+z^{-4}}{1+L_1z^{-1}+(L_2-2L_1)z^{-2}+(L_3+L_1-L_2)z^{-3}+L_4z^{-4}} \quad (91)$$

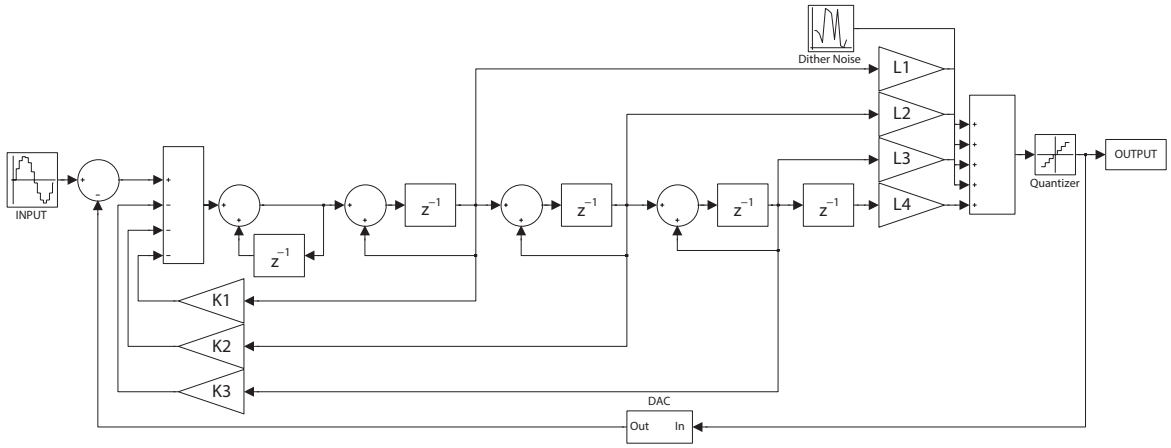



**Figure 141: 2nd-order, SP CI-FBFF Topology**

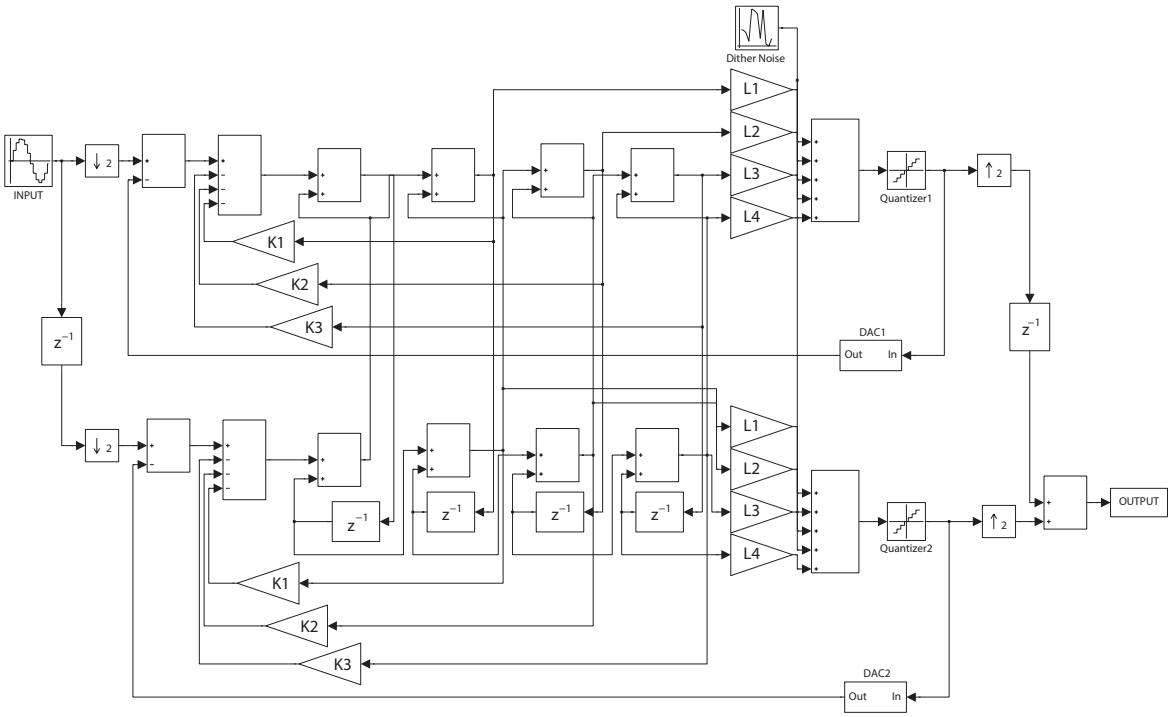



**Figure 142: 4th-order, 2-path CI-FBFF Topology**

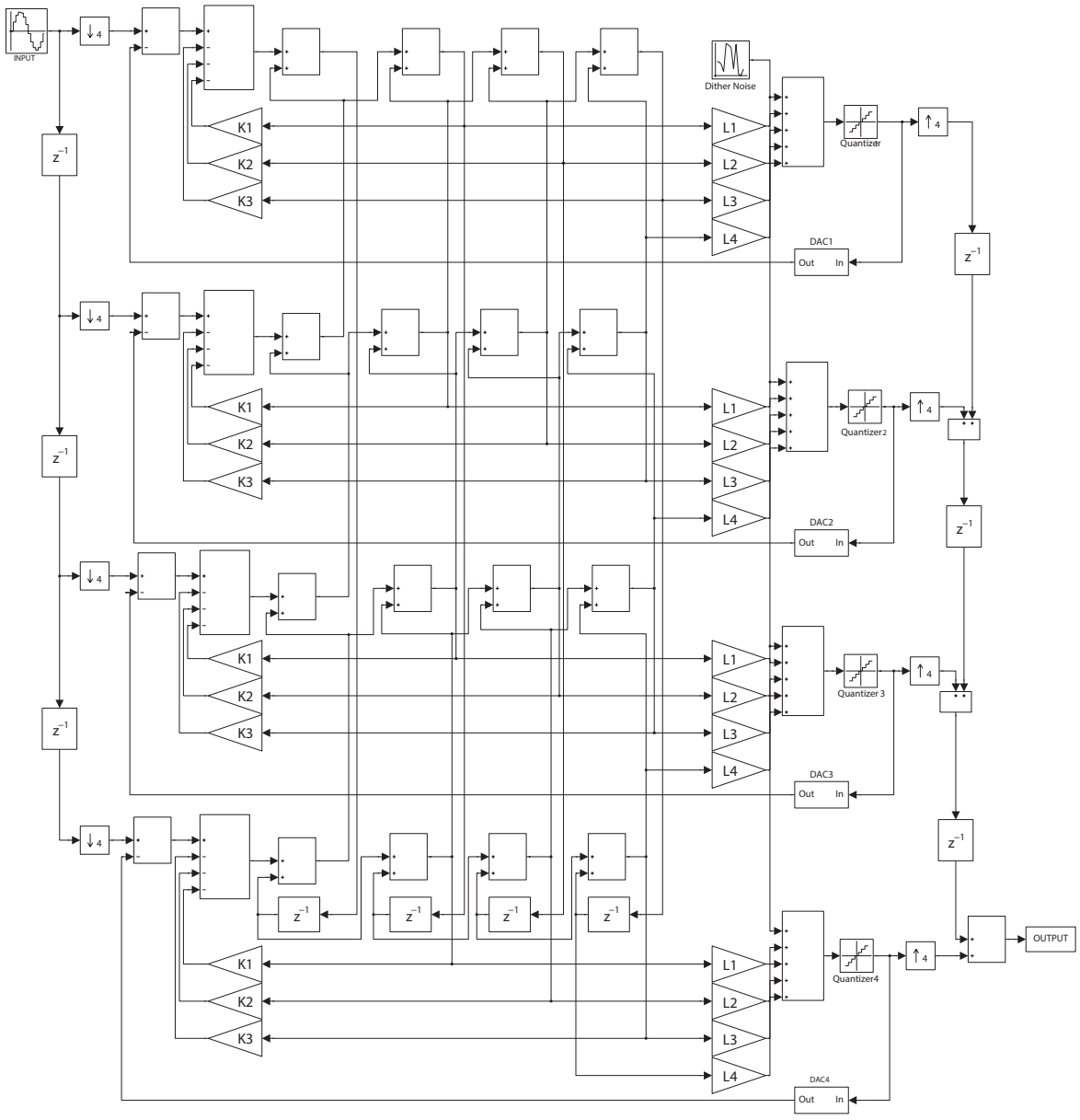



**Figure 143: 4th-order, 4-path CI-FBFF Topology**

**Symbolic NTF for 6$^{th}$-order CI-FBFF Topology:**

$$NTF_{CI-FBFF,6^{th}}(z)=\frac{1+n_2z^{-1}+n_3z^{-2}+n_4z^{-3}+n_5z^{-4}+z^{-5}}{1+d_2z^{-1}+d_3z^{-2}+d_4z^{-3}+d_5z^{-4}+d_6z^{-5}} \tag{92}$$

$$n_2 = K_1 - 6 \tag{93}$$

$$n_3 = K_2 - 4K_1 + 15 \tag{94}$$

$$n_4 = K_3 + 6K_1 - 3K_2 - 20 \tag{95}$$

$$n_5 = K_4 - 4K_1 + 3K_2 - 2K_3 + 15 \tag{96}$$

$$n_6 = K_5 + K_1 - K_2 + K_3 - K_4 - 6 \tag{97}$$

$$d_2 = L_1 \tag{98}$$

$$d_3 = L_2 - 4L_1 \tag{99}$$

$$d_4 = L_3 + 6L_1 - 3L_2 \tag{100}$$

$$d_5 = L_4 - 4L_1 + 3L_2 - 2L_3 \tag{101}$$

$$d_6 = L_5 + L_1 - L_2 + L_3 - L_4 \tag{102}$$

$$d_7 = L_7 \tag{103}$$

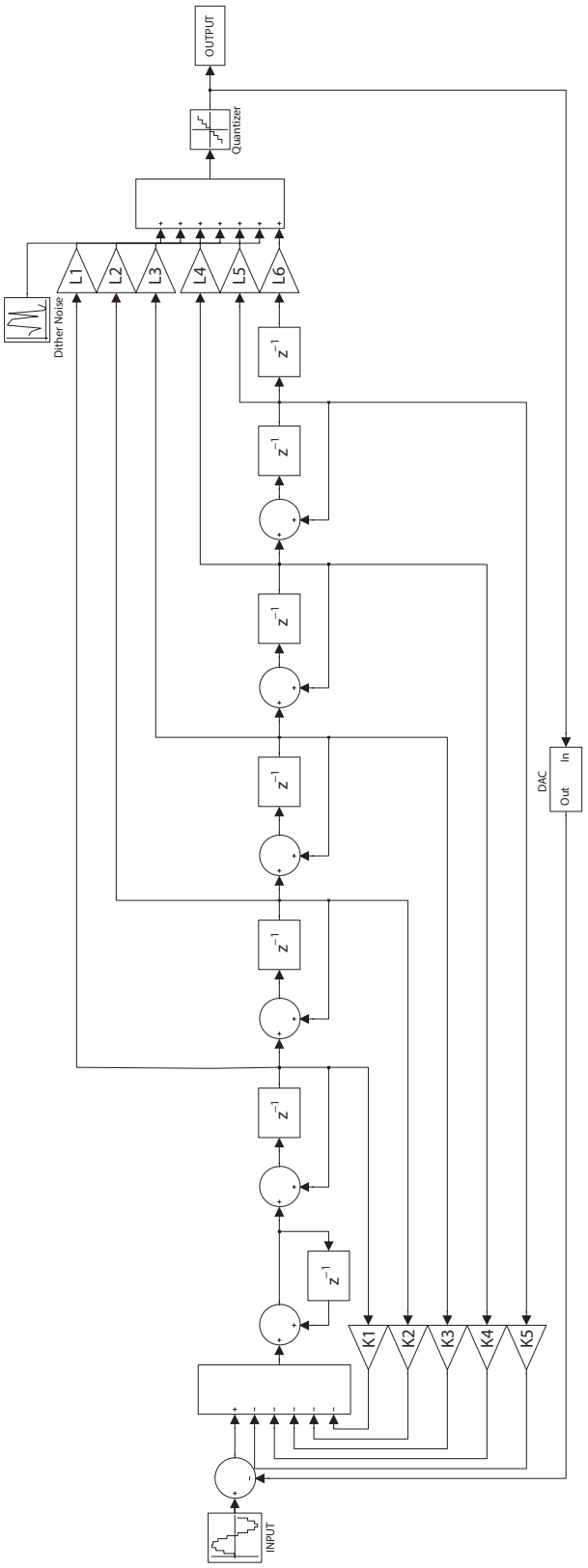



**Figure 144: 6th-order, SP CI-FBFF Topology**

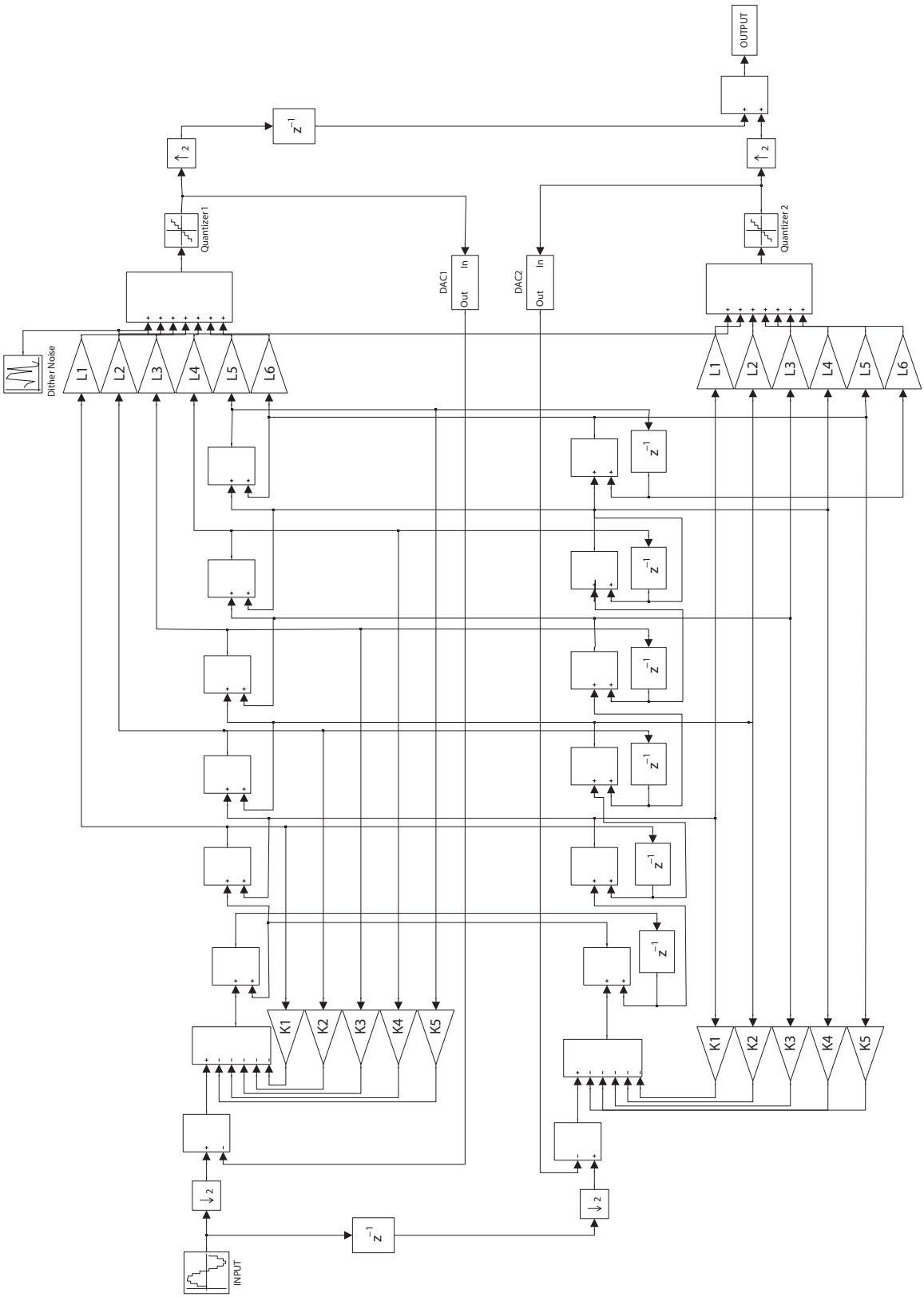



**Figure 145: 6th-order, 2-path CI-FBFF Topology**

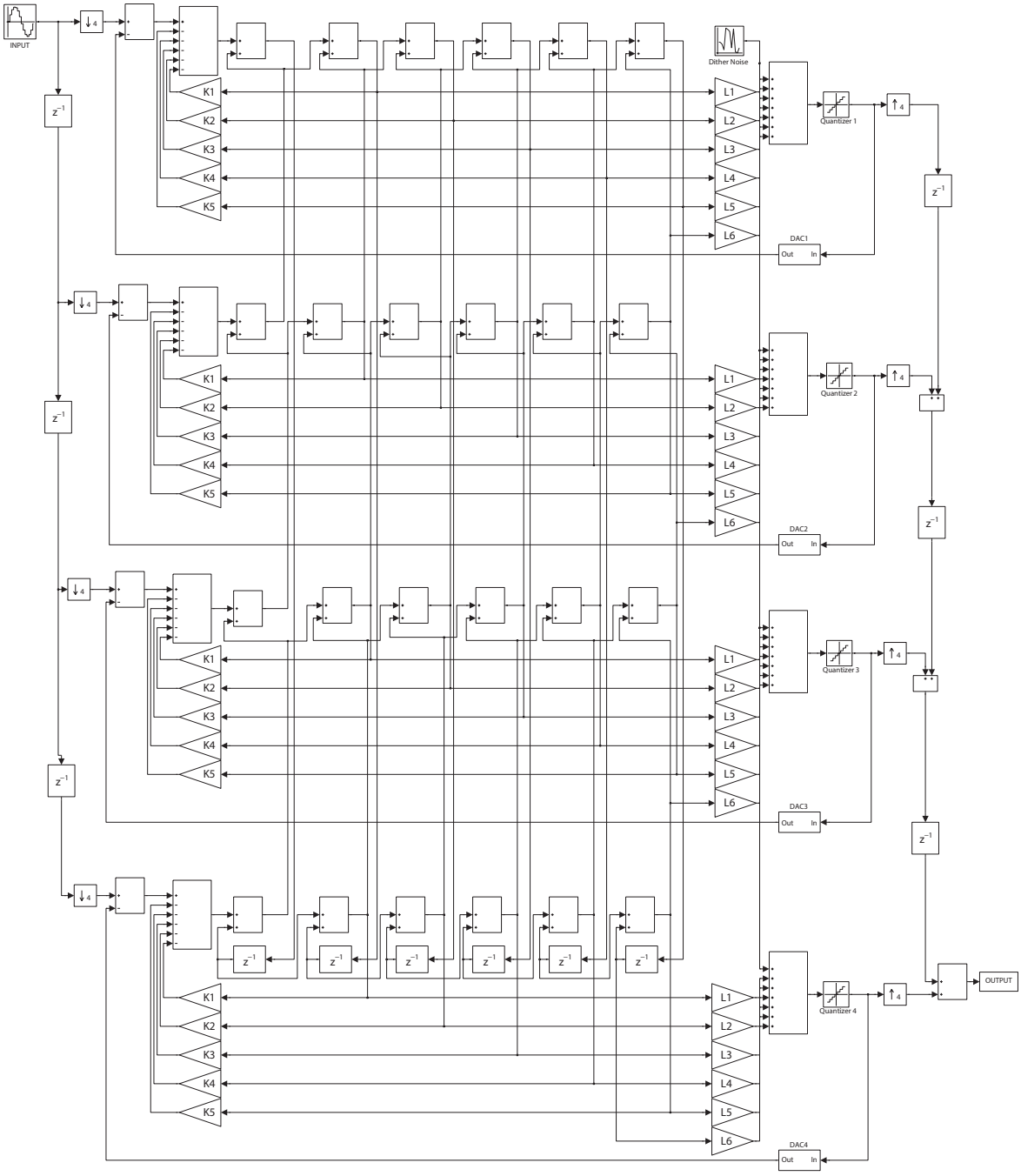



**Figure 146: 6th-order, 4-path CI-FBFF Topology**

**Symbolic NTF for 8th-order CI-FBFF Topology:**

$$NTF_{CI-FBFF,8^{th}}(z)=\frac{1+n_2z^{-1}+n_3z^{-2}+n_4z^{-3}+n_5z^{-4}+n_6z^{-5}+n_7z^{-6}+n_8z^{-7}+z^{-8}}{1+d_2z^{-1}+d_3z^{-2}+d_4z^{-3}+d_5z^{-4}+d_6z^{-5}+d_7z^{-6}+d_8z^{-7}+d_9z^{-8}} \quad (104)$$

$$n_2 = K_1 - 8 \quad (105)$$

$$n_3 = K_2 - 6K_1 + 28 \quad (106)$$

$$n_4 = K_3 + 15K_1 - 5K_2 - 56 \quad (107)$$

$$n_5 = K_4 - 20K_1 + 10K_2 - 4K_3 + 70 \quad (108)$$

$$n_6 = K_5 + 15K_1 - 10K_2 + 6K_3 - 3K_4 \quad (109)$$

$$n_7 = K_6 - 6K_1 + 5K_2 - 4K_3 + 3K_4 - 2K_5 + 28 \quad (110)$$

$$n_7 = K_7 + K_1 - K_2 + K_3 - K_4 + K_5 - K_6 - 8 \quad (111)$$

$$d_2 = L_1 \quad (112)$$

$$d_3 = L_2 - 6L_1 \quad (113)$$

$$d_4 = L_3 + 15L_1 - 5L_2 \quad (114)$$

$$d_5 = L_4 - 20L_1 + 10L_2 - 4L_3 \quad (115)$$

$$d_6 = L_5 + 15L_1 - 10L_2 + 6L_3 - 3L_4 \quad (116)$$

$$d_7 = L_6 - 6L_1 + 5L_2 - 4L_3 + 3L_4 - 2L_5 \quad (117)$$

$$d_8 = L_7 + L_1 - L_2 + L_3 - L_4 + L_5 - L_6 \quad (118)$$

$$d_8 = L_8 \quad (119)$$

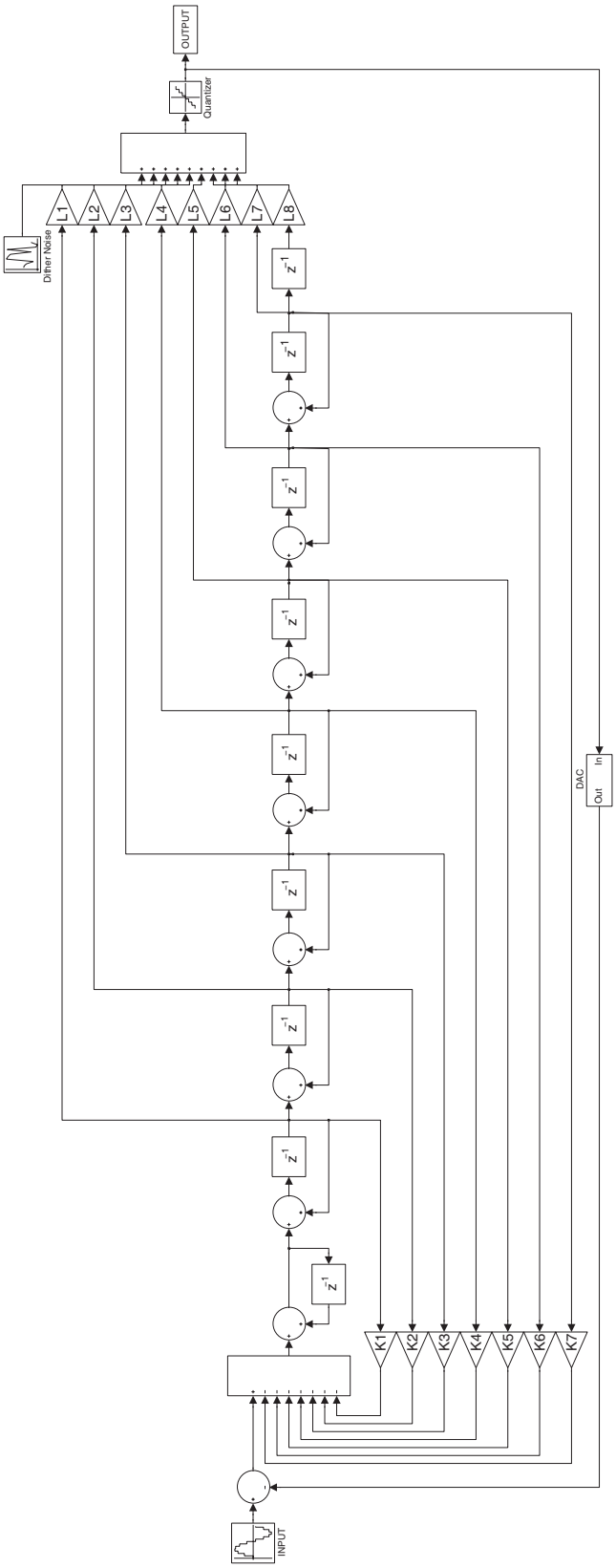



**Figure 147: 8th-order, SP CI-FBFF Topology**

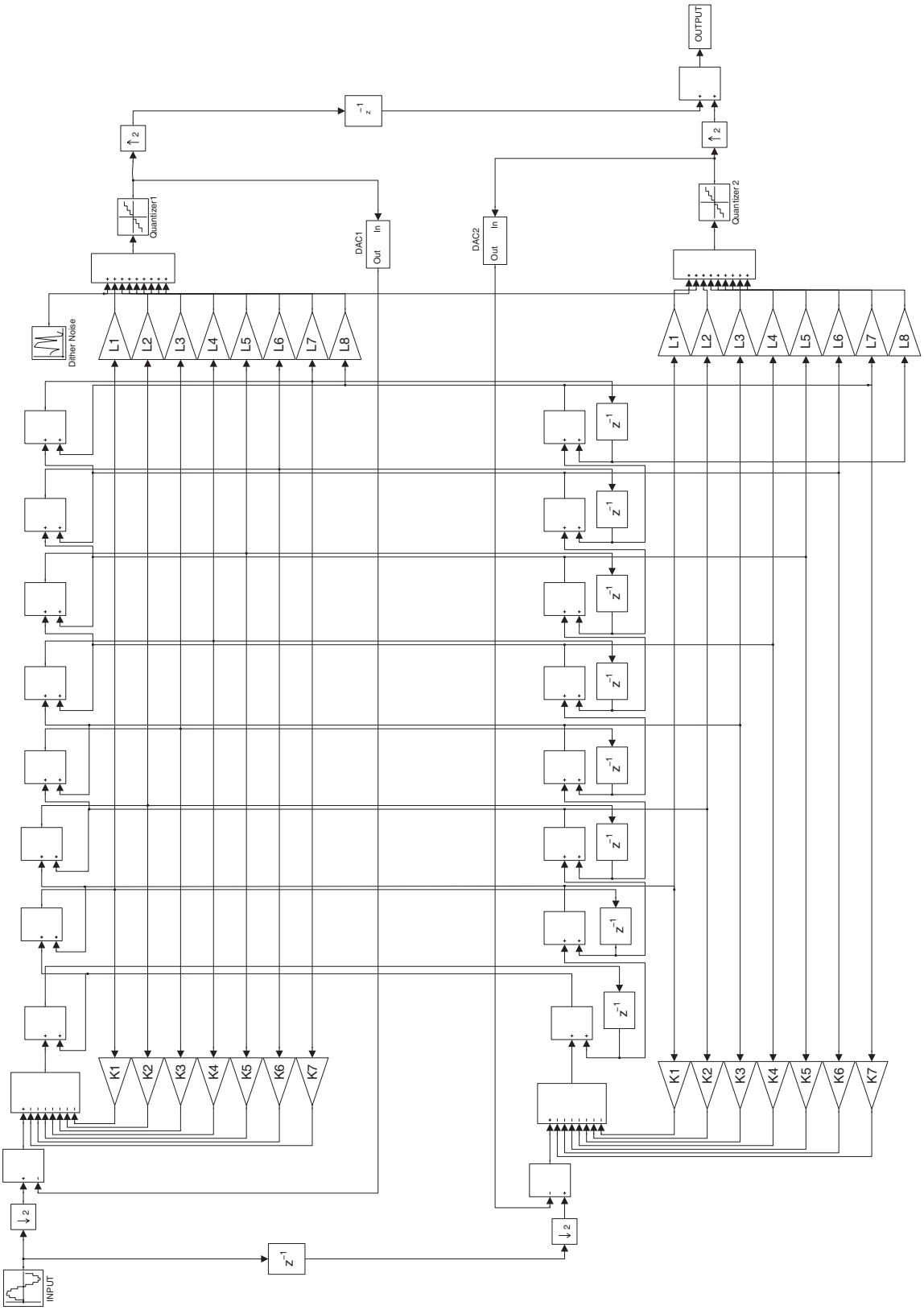



**Figure 148: 8th-order, 2-path CI-FBFF Topology**

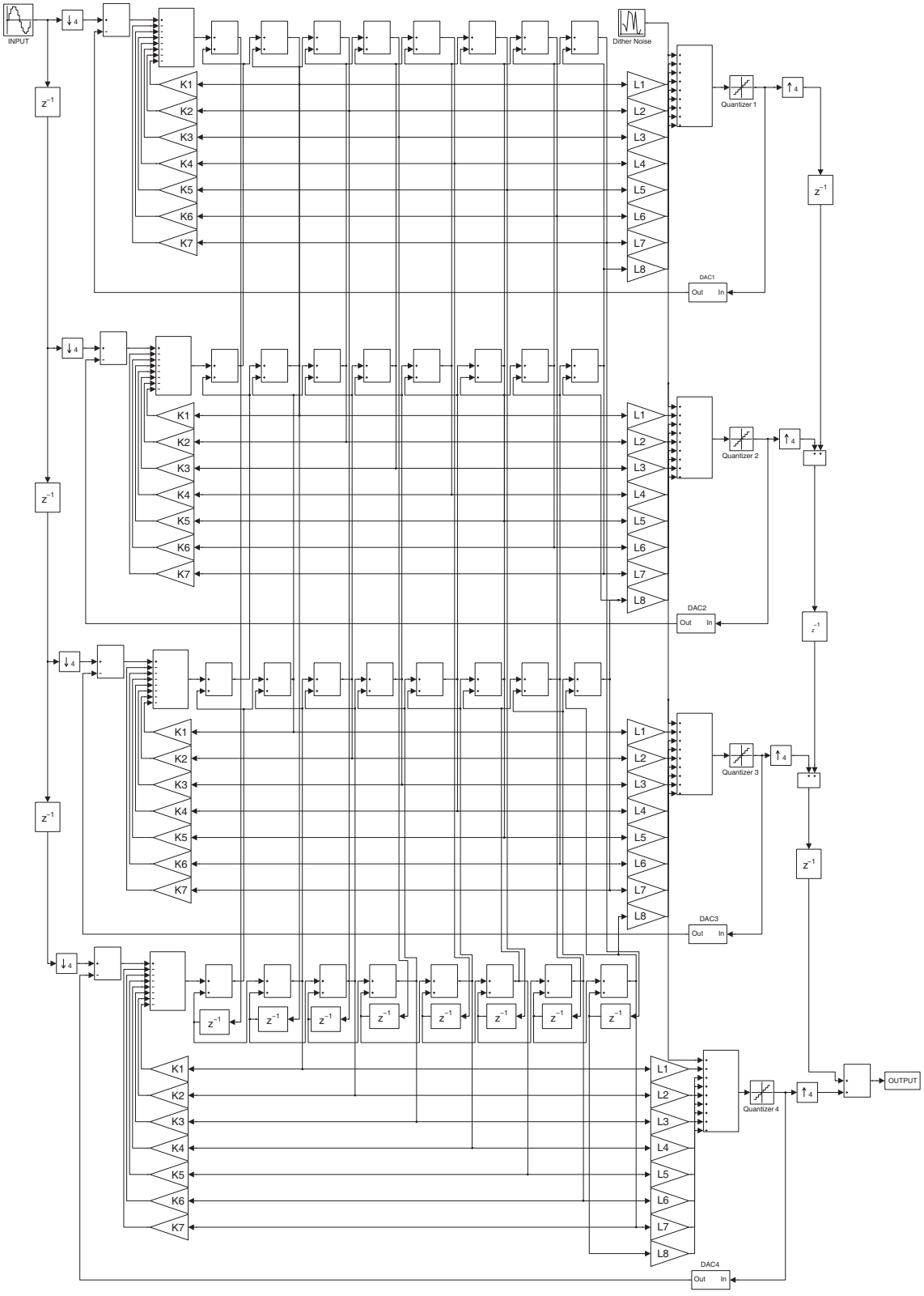



**Figure 149: 8th-order, 4-path CI-FBFF Topology**

## Appendix B

The designed A/D CI-RFB VBP Σ-Δ modulators are depicted in this Appendix. Their symbolic NTFs are also provided.

### Symbolic NTF for 2nd-order CR-RFB Topology:

$$NTF_{CR-RFB,2^{nd}}(z) = \frac{1 + K_1 z^{-1} + z^{-2}}{1 + (L_1 + K_1) z^{-1} + (L_2 + 1) z^{-2}} \tag{120}$$

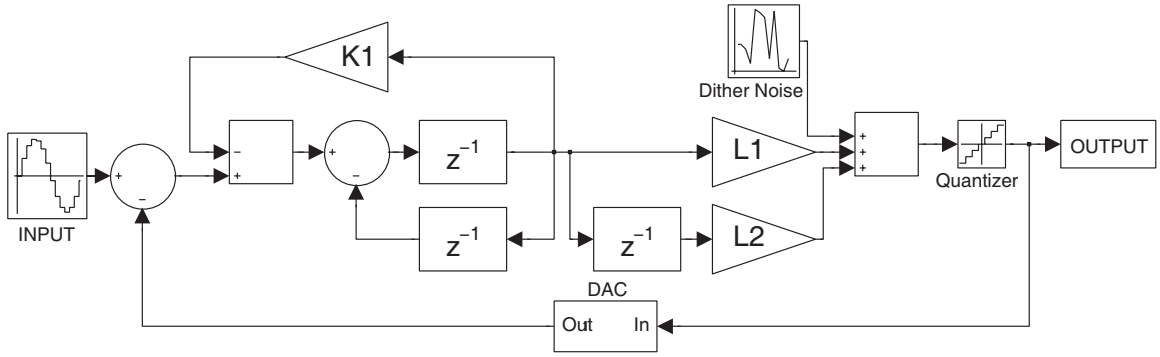



**Figure 150: 2nd-order, SP CR-RFB Topology**

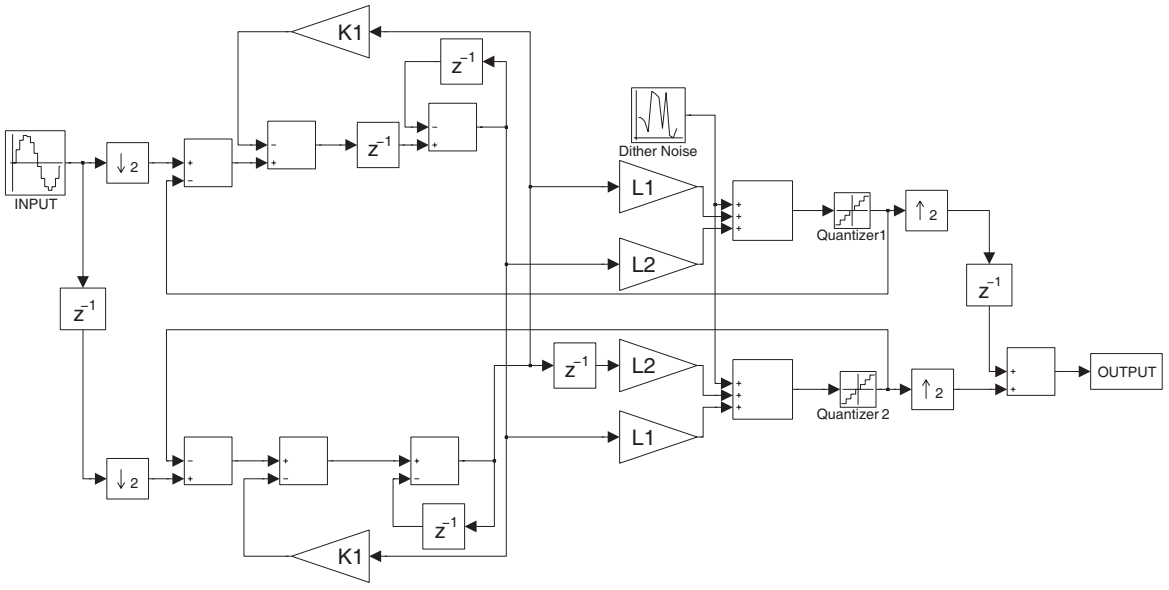



**Figure 151: 2nd-order, 2-path CR-RFB Topology**

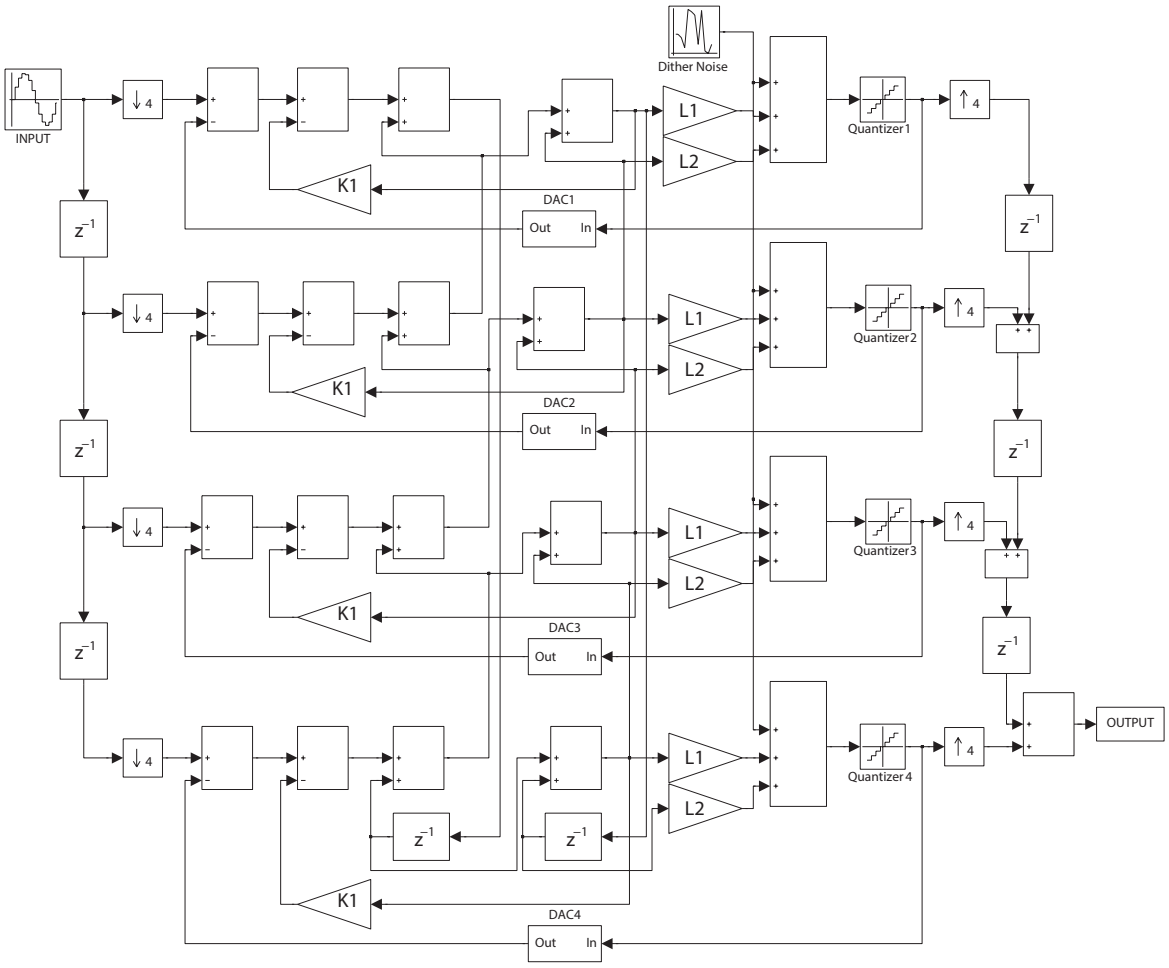



**Figure 152: 2nd-order, 4-path CR-RFB Topology**

**Symbolic NTF for 4th-order CR-RFB Topology:** For the 4th-, 6th- and 8th-orders of the CR-RFB topologies, the MATLAB codes are provided those are used to calculate the NTFs' coefficients.

$$NTF_{CR-RFB,4^{th}}(z) = \frac{\left(1+K_1 z^{-1}+z^{-2}\right)\left(1+K_2 z^{-1}+z^{-2}\right)}{1+d_2 z^{-1}+d_3 z^{-2}+d_4 z^{-3}+d_5 z^{-4}} \tag{121}$$

***

```
[num1, den1] = butter(order1, [freq1*2, freq2*2], 'stop');
num1=num1/num1(1);
num=num1;
den=den1;

Z1=roots(num);
Z1_1=[Z1(1),Z1(2)];
Z1_2=[Z1(3),Z1(4)];
zer_pol1=poly(Z1_1);
zer_pol2=poly(Z1_2);
K1=zer_pol1(2);
K2=zer_pol2(2);

A=[0 1 0 0; 1 K2 0 1; K2 1 1 0; 1 0 0 0];
B=[(den(5)-1); (den(4)-K1-K2); (den(3)-K1*K2-2); (den(2)-K1-K2)];
C=linsolve(A,B);
L1=C(1);
L2=C(2);
L3=C(3);
L4=C(4);
```

***

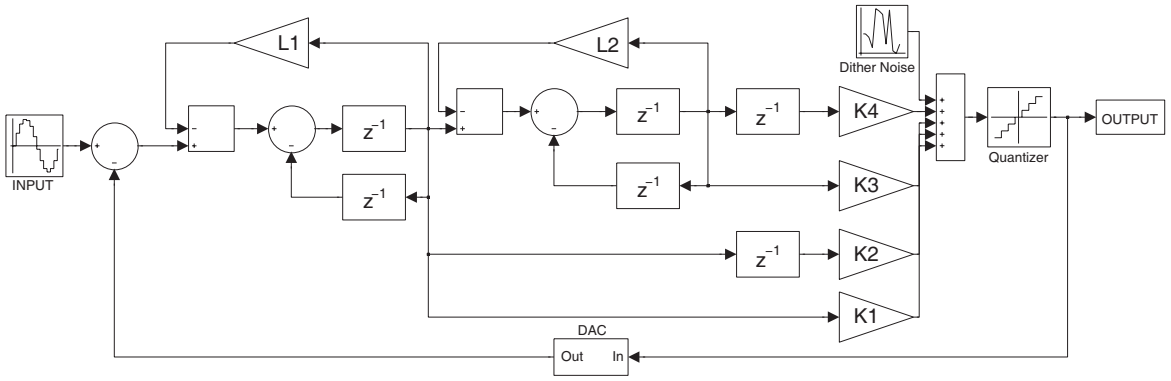



**Figure 153: 4th-order, SP CR-RFB Topology**

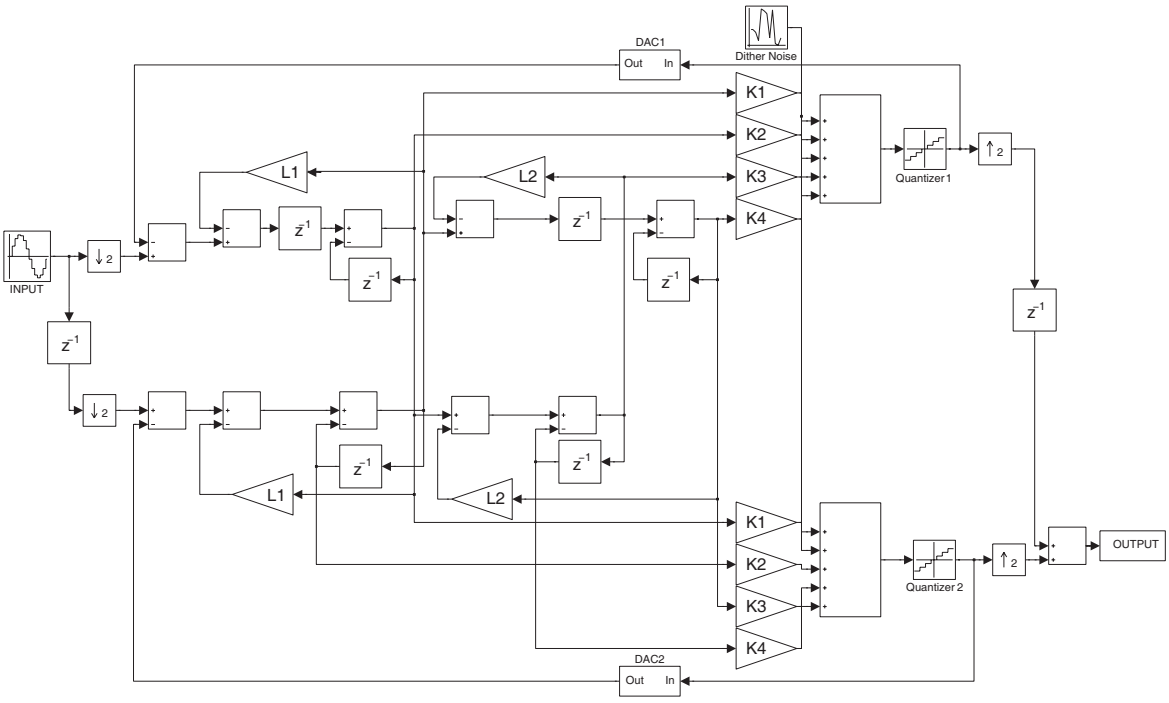



**Figure 154: 4th-order, 2-path CR-RFB Topology**

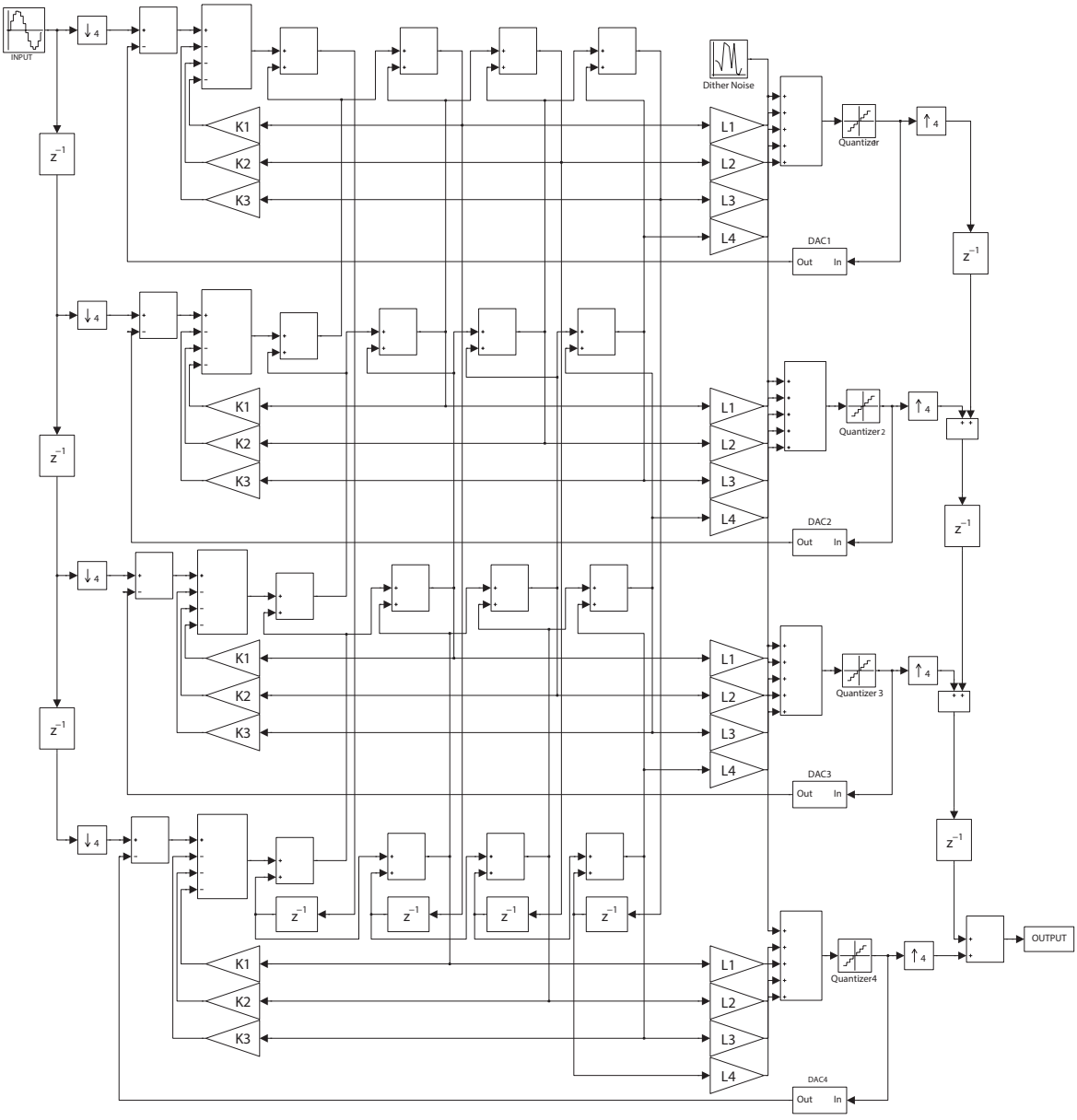



**Figure 155: 4th-order, 4-path CR-RFB Topology**

**Symbolic NTF for 6th-order CR-RFB Topology:**

$$NTF_{CR-RFB,6^{th}}(z)=\frac{\left(1+K_1z^{-1}+z^{-2}\right)\left(1+K_2z^{-1}+z^{-2}\right)\left(1+K_3z^{-1}+z^{-2}\right)}{1+d_2z^{-1}+d_3z^{-2}+d_4z^{-3}+d_5z^{-4}+d_6z^{-5}+d_7z^{-6}} \quad (122)$$

***

```
[num1, den1] = butter(order1, [freq1*2, freq2*2], 'stop');
num1=num1/num1(1);
num=num1;
den=den1;
Z1=roots(num);
Z1_1=[Z1(1),Z1(2)];
Z1_2=[Z1(3),Z1(4)];
Z1_3=[Z1(5),Z1(6)];
zer_pol1=poly(Z1_1);
zer_pol2=poly(Z1_2);
zer_pol3=poly(Z1_3);
K1=zer_pol1(2);
K2=zer_pol2(2);
K3=zer_pol3(2);
A=[0 1 0 0 0 0; 1 K2+K3 0 1 0 0;
K2+K3 K2*K3+2 1 K3 0 1;
2+K2*K3 K2+K3 L3 1 1 0 ;
K2+K3 1 1 0 0 0;
1 0 0 0 0 0];
B=[(den(7)-1);(den(6)-K1-K2-K3);
(den(5)-K1*K2-K1*K3-K2*K3-3);
(den(4)-2*K1-2*K2-2*K3-K1*K2*K3);
(den(3)-K1*K2-K1*K3-K2*K3-3);
(den(2)-K1-K2-K3)];
C=linsolve(A,B);
L1=C(1);
L2=C(2);
L3=C(3);
L4=C(4);
L5=C(5);
L6=C(6);
```

***

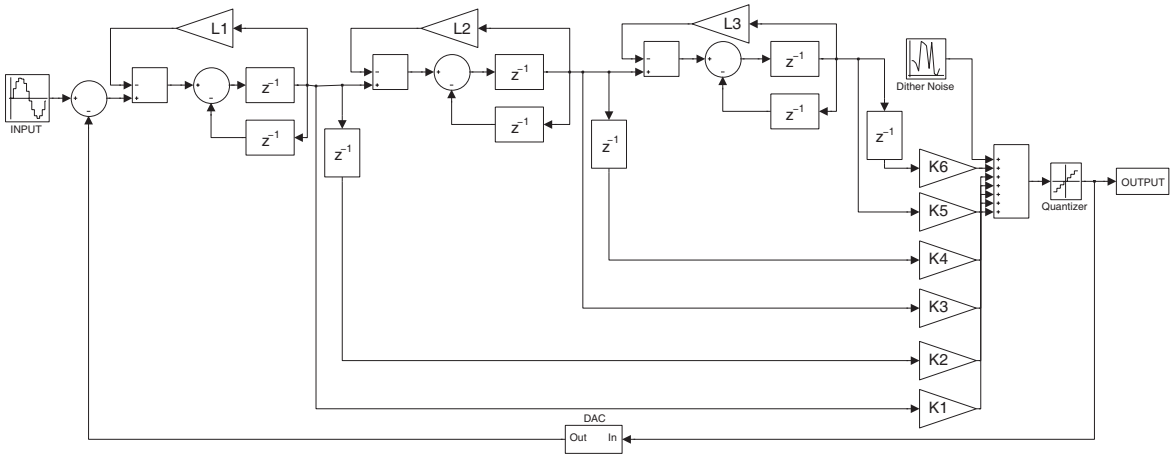



**Figure 156: 6th-order, SP CR-RFB Topology**

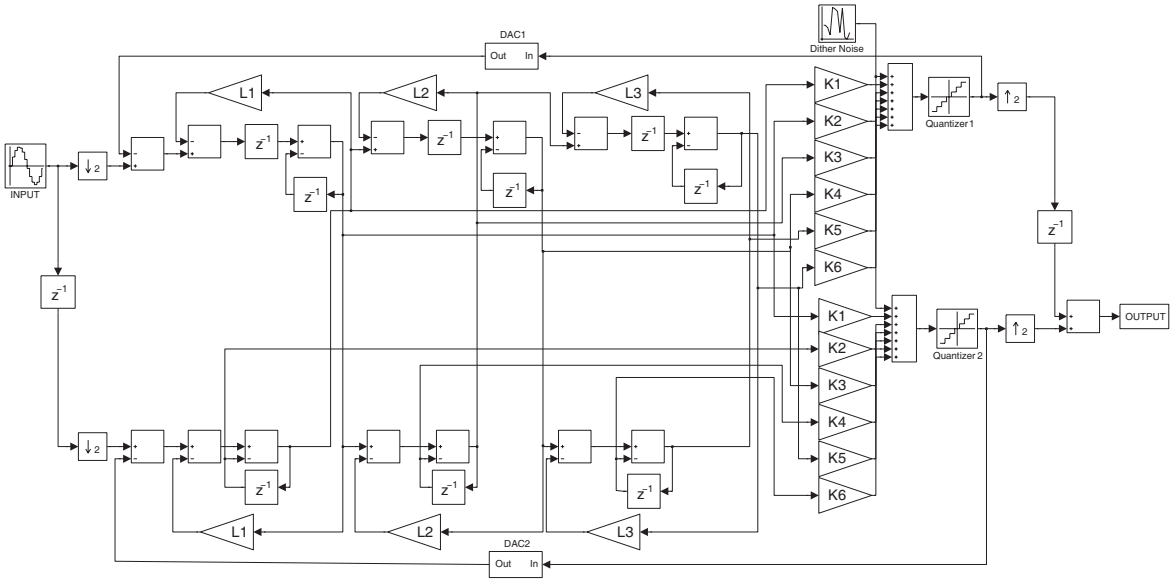



**Figure 157: 6th-order, 2-path CR-RFB Topology**

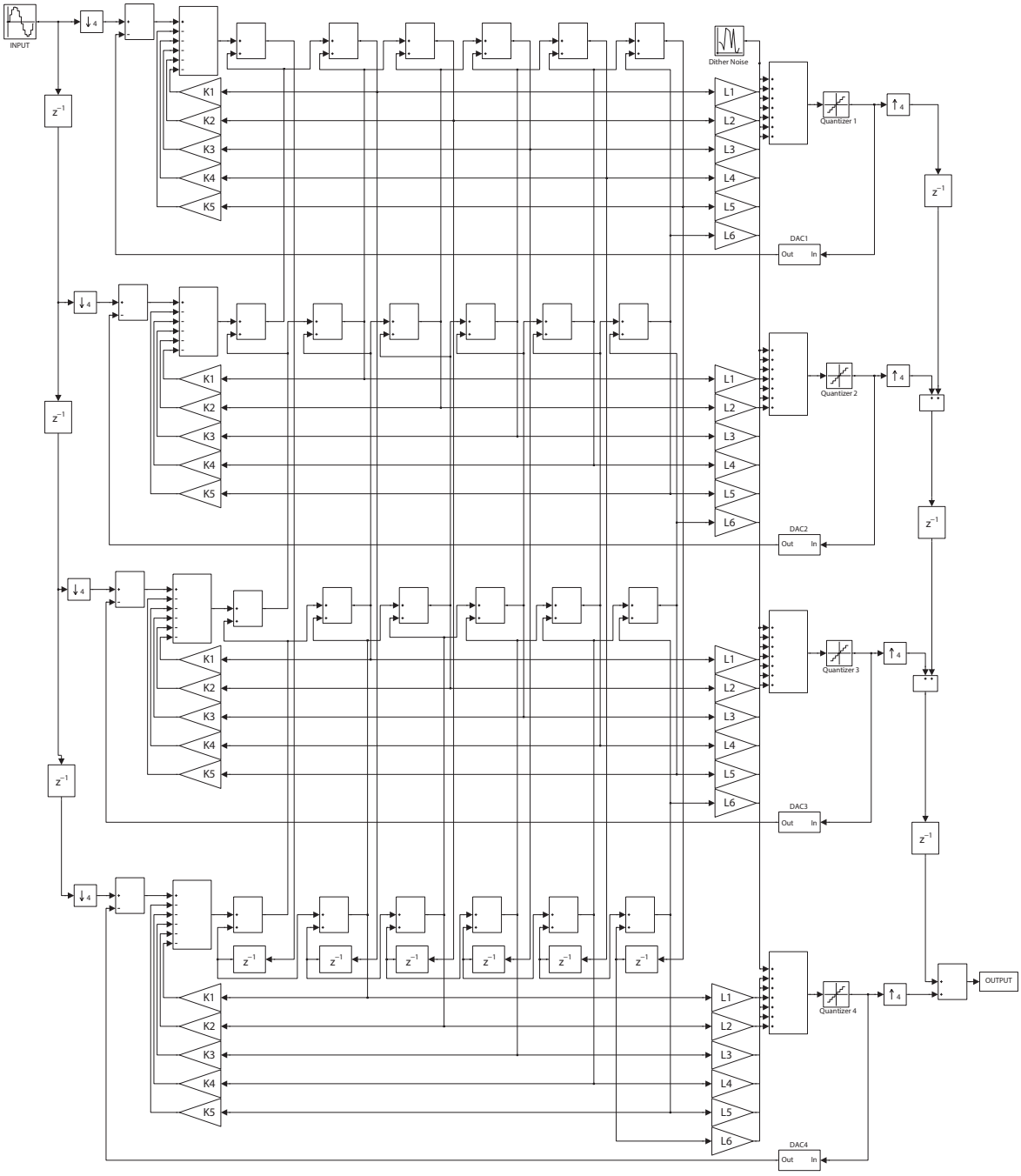



**Figure 158: 6$^{th}$-order, 4-path CR-RFB Topology**

**Symbolic NTF for 8th-order CR-RFB Topology:**

$$NTF_{CR-RFB,8^{th}}(z)=\frac{\left(1+K_1z^{-1}+z^{-2}\right)\left(1+K_2z^{-1}+z^{-2}\right)\left(1+K_3z^{-1}+z^{-2}\right)\left(1+K_3z^{-1}+z^{-2}\right)}{1+d_2z^{-1}+d_3z^{-2}+d_4z^{-3}+d_5z^{-4}+d_6z^{-5}+d_7z^{-6}+d_8z^{-7}+d_9z^{-8}} \tag{123}$$

***

```
[num1, den1] = butter(order1, [freq1*2, freq2*2], 'stop');
num1=num1/num1(1);
num=num1;
den=den1;

Z1=roots(num);
Z1_1=[Z1(1),Z1(2)];
Z1_2=[Z1(3),Z1(4)];
Z1_3=[Z1(5),Z1(6)];
Z1_4=[Z1(7),Z1(8)];

zer_pol1=poly(Z1_1);
zer_pol2=poly(Z1_2);
zer_pol3=poly(Z1_3);
zer_pol4=poly(Z1_4);

K1=zer_pol1(2);
K2=zer_pol2(2);
K3=zer_pol3(2);
K4=zer_pol3(2);

A=[0 1 0 0 0 0 0 0;
1 (K2+K3+K4) 0 1 0 0 0 0;
(K2+K3+K4)  (K2*K3+K2*K4+K3*K4+3) 1 (K3+K4) 0 1 0 0; (K2*K3+K2*K4+K3*K4+3)
(2*K2+2*K3+K2*K3*K4+2*K4) (K3+K4) (K3*K4+2) 1 K4 0 1;
(2*K2+2*K3+2*K4+K2*K3*K4) (K2*K3+K2*K4+K3*K4+3) (K3*K4+2) (K3+K4) K4 1 1 0;
(K2*K3+K2*L4+K3*K4+3) (K2+K3+K4) (K3+K4) 1 1 0 0 0; (K2+K3+K4) 1 1 0 0 0 0
0;
1 0 0 0 0 0 0 0];
```

```
B=[(den(9)-1);
(den(8)-K1-K2-K3-K4);
(den(7)-K1*K2- K1*K3-K1*K4-K2*K3-K2*K4-K3*K4-4);
(den(6)-3*K1 - 3*K2 - 3*K3 - 3*K4 - K1*K2*K3 - K1*K2*K4 - K1*K3*K4 -
K2*K3*K4);
(den(5)-2*K1*K2-2*K1*K3-2*K1*K4-2*K2*K3-2*K2*K4-2*K3*K4-6-K1*K2*K3*K4);
(den(4)-3*K1-3*K2-3*K3-3*K4-K1*K2*K3-K1*K2*K4-K1*K3*K4-K2*K3*K4  );
(den(3)-K1*K2-K1*K3-K1*K4-K2*K3-K2*K4-K3*K4-4); (den(2)-K1-K2-K3-K4)];

C=linsolve(A,B);
L1=C(1);
L2=C(2);
L3=C(3);
L4=C(4);
L5=C(5);
L6=C(6);
L7=C(7);
L8=C(8);
```

***

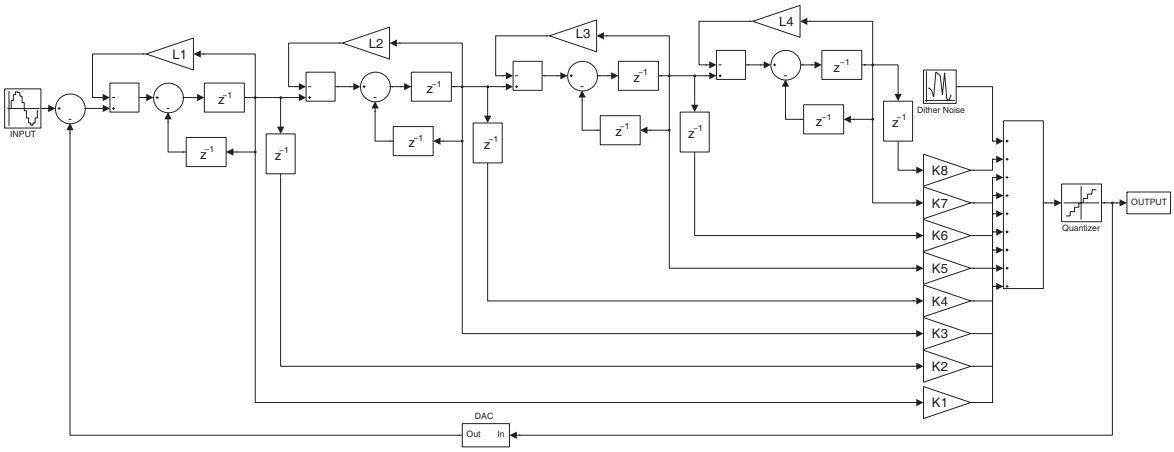



**Figure 159: 8th-order, SP CR-RFB Topology**

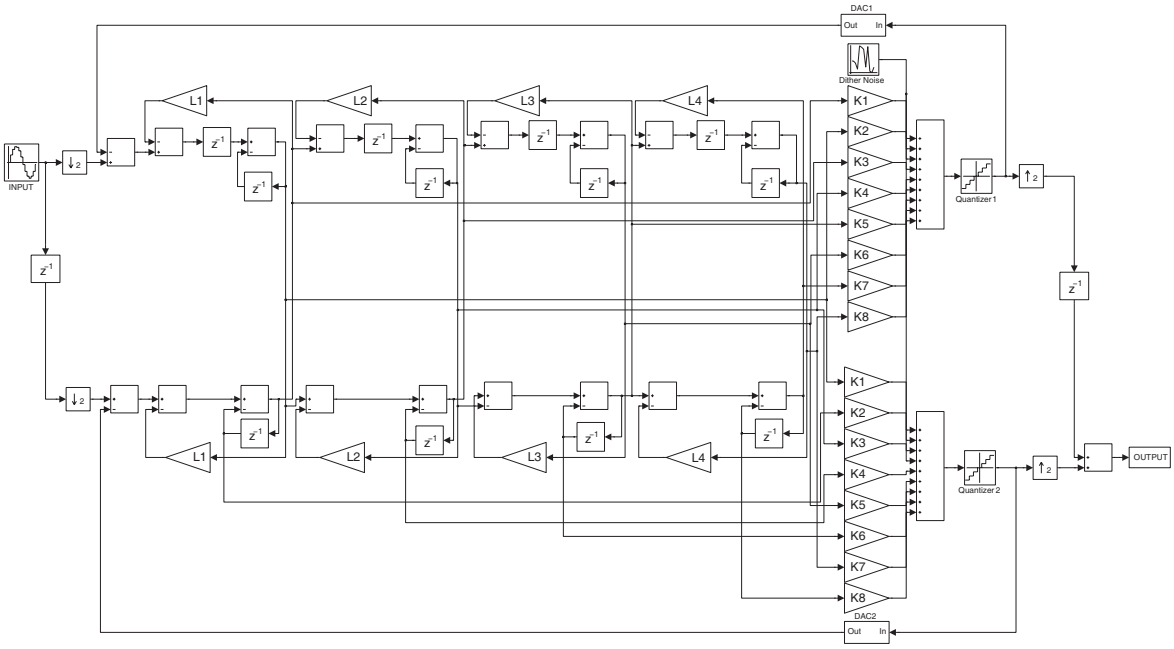



**Figure 160: 8th-order, 2-path CR-RFB Topology**

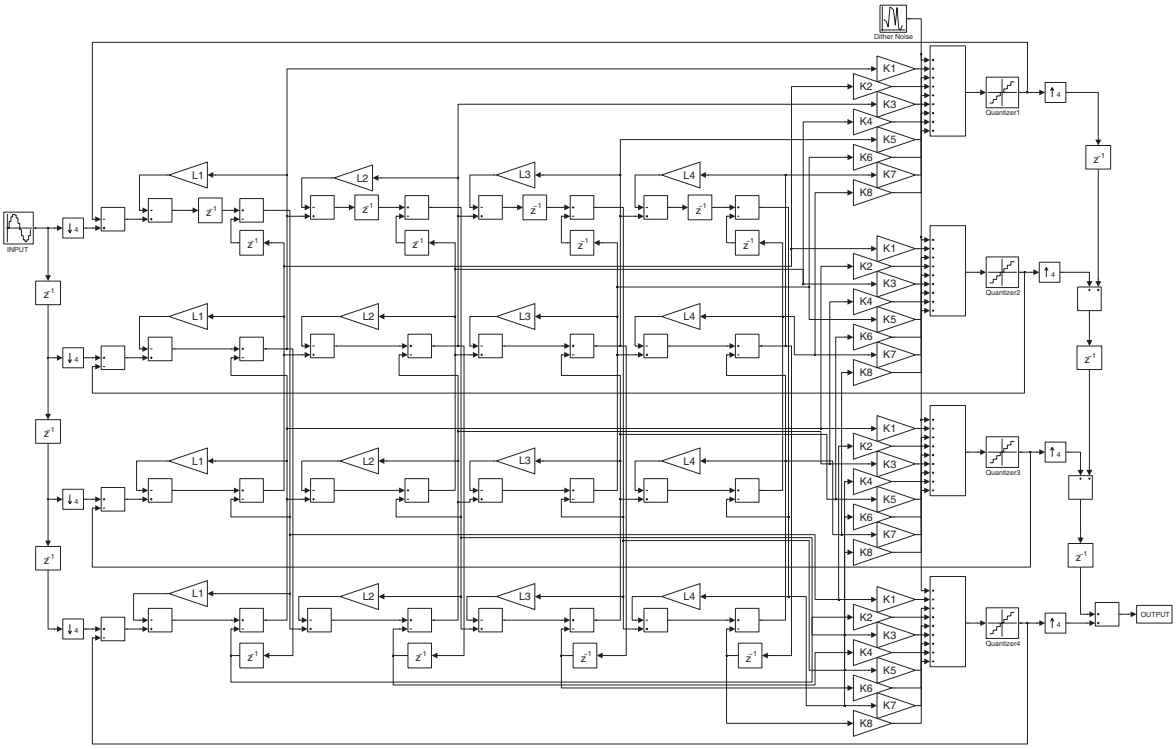



**Figure 161: 8th-order, 4-path CR-RFB Topology**

## Appendix C

The designed D/A VBP Σ-Δ modulators of the EF topology are depicted in this Appendix. Their symbolic NTFs are also provided.

**Symbolic NTF for 2nd-order EF Topology:**

$$NTF_{EF,2^{nd}}(z) = \frac{1+(L_1-K_1)z^{-1}+(L_2-K_2)z^{-2}}{1+L_1z^{-1}+L_2z^{-2}} \tag{124}$$

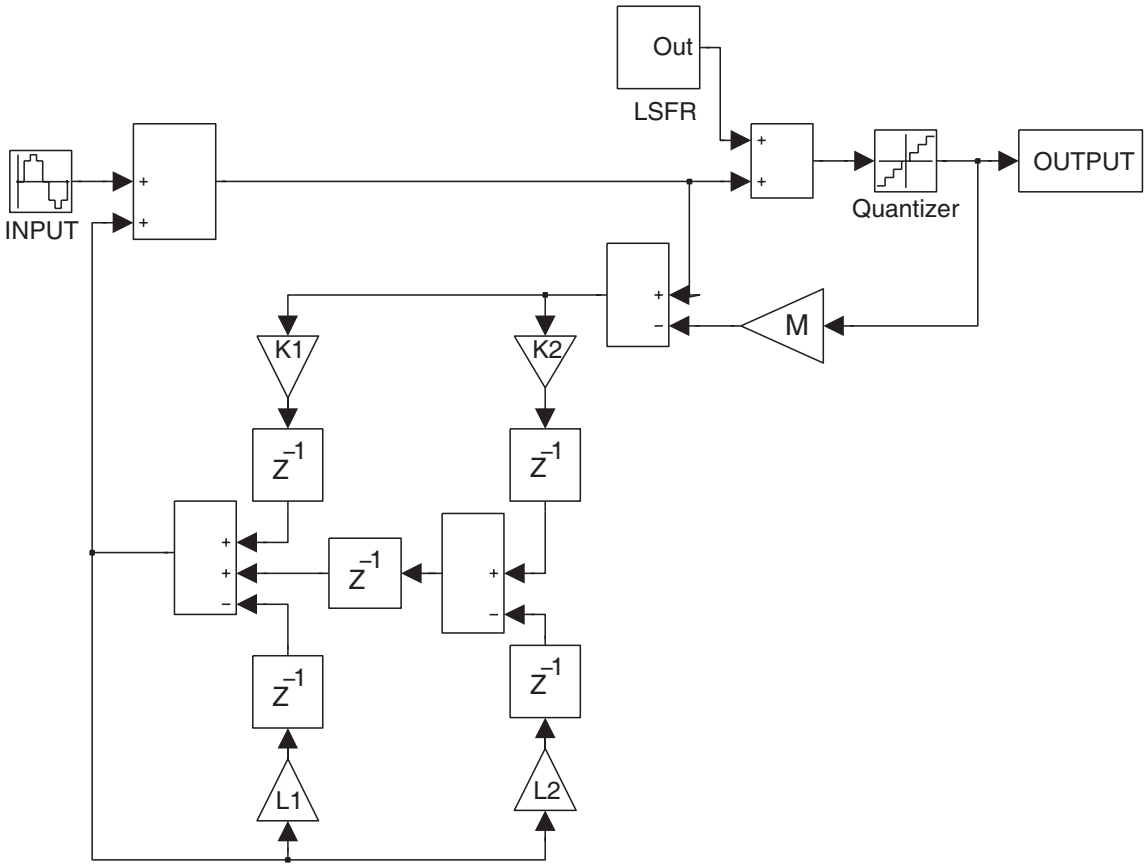



**Figure 162: 2nd-order, SP EF Topology**

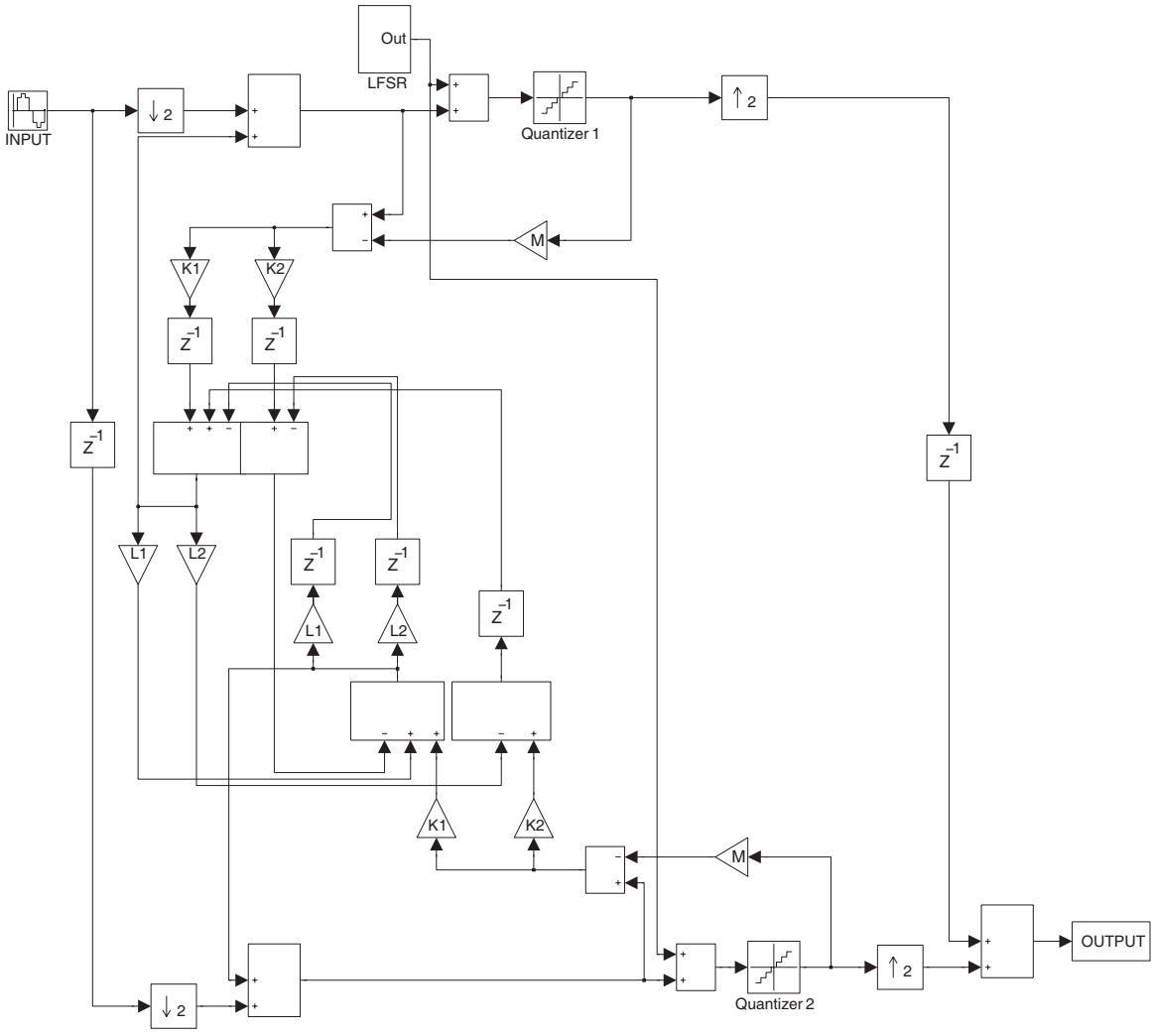



**Figure 163: 2nd-order, 2-path EF Topology**

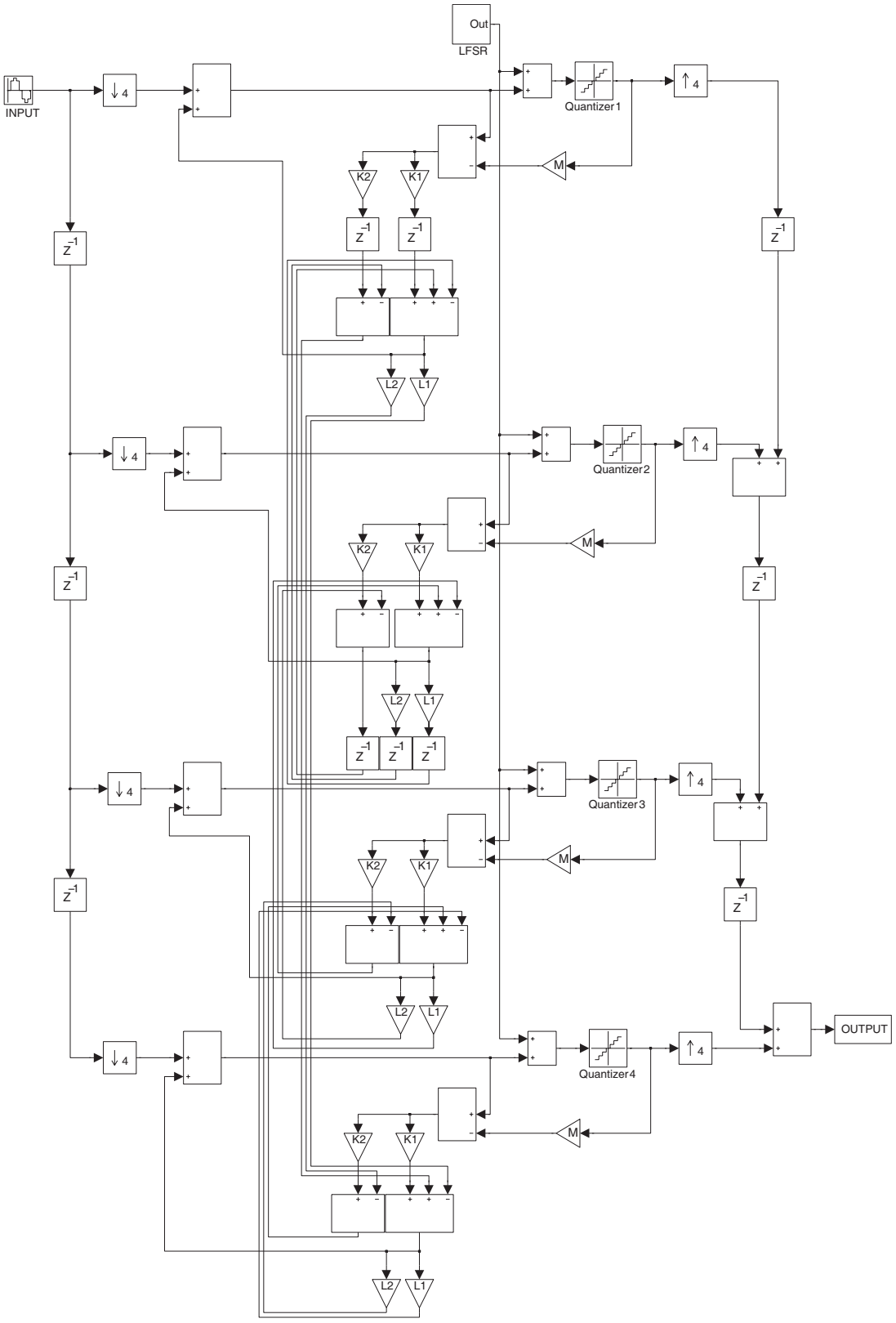



**Figure 164: 2nd-order, 4-path EF Topology**

**Symbolic NTF for 4th-order EF Topology:**

$$NTF_{EF,4^{th}}(z) = \frac{1+(L_1-K_1)z^{-1}+(L_2-K_2)z^{-2}+(L_3-K_3)z^{-3}+(L_4-K_4)z^{-4}}{1+L_1z^{-1}+L_2z^{-2}+L_3z^{-3}+L_4z^{-4}} \tag{125}$$

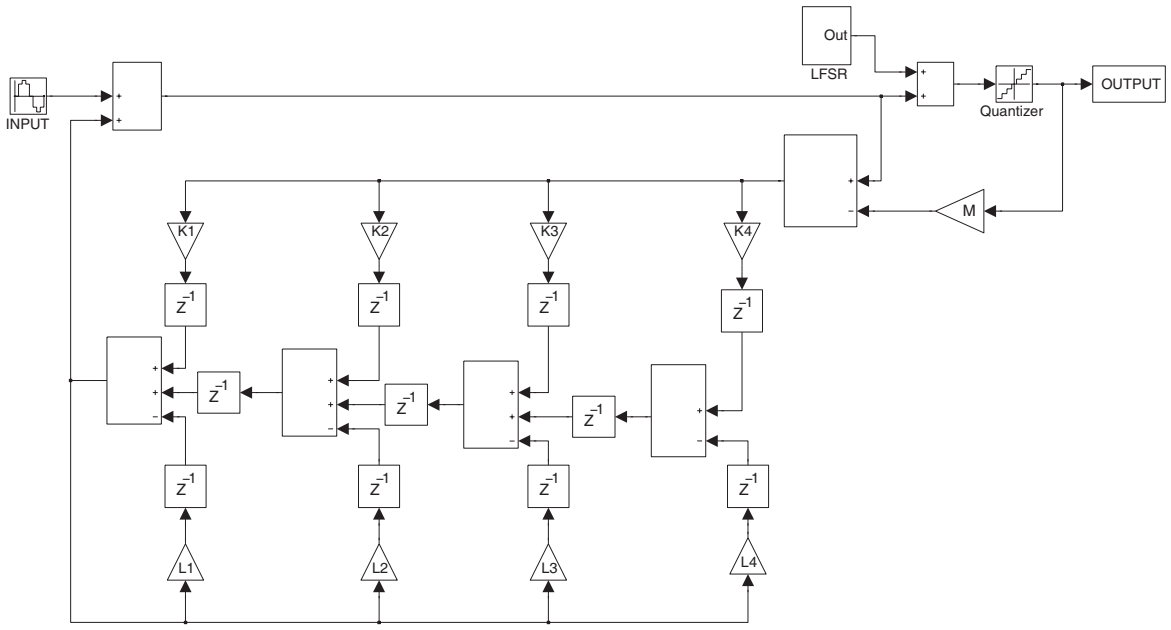



**Figure 165: 4th-order, SP EF Topology**

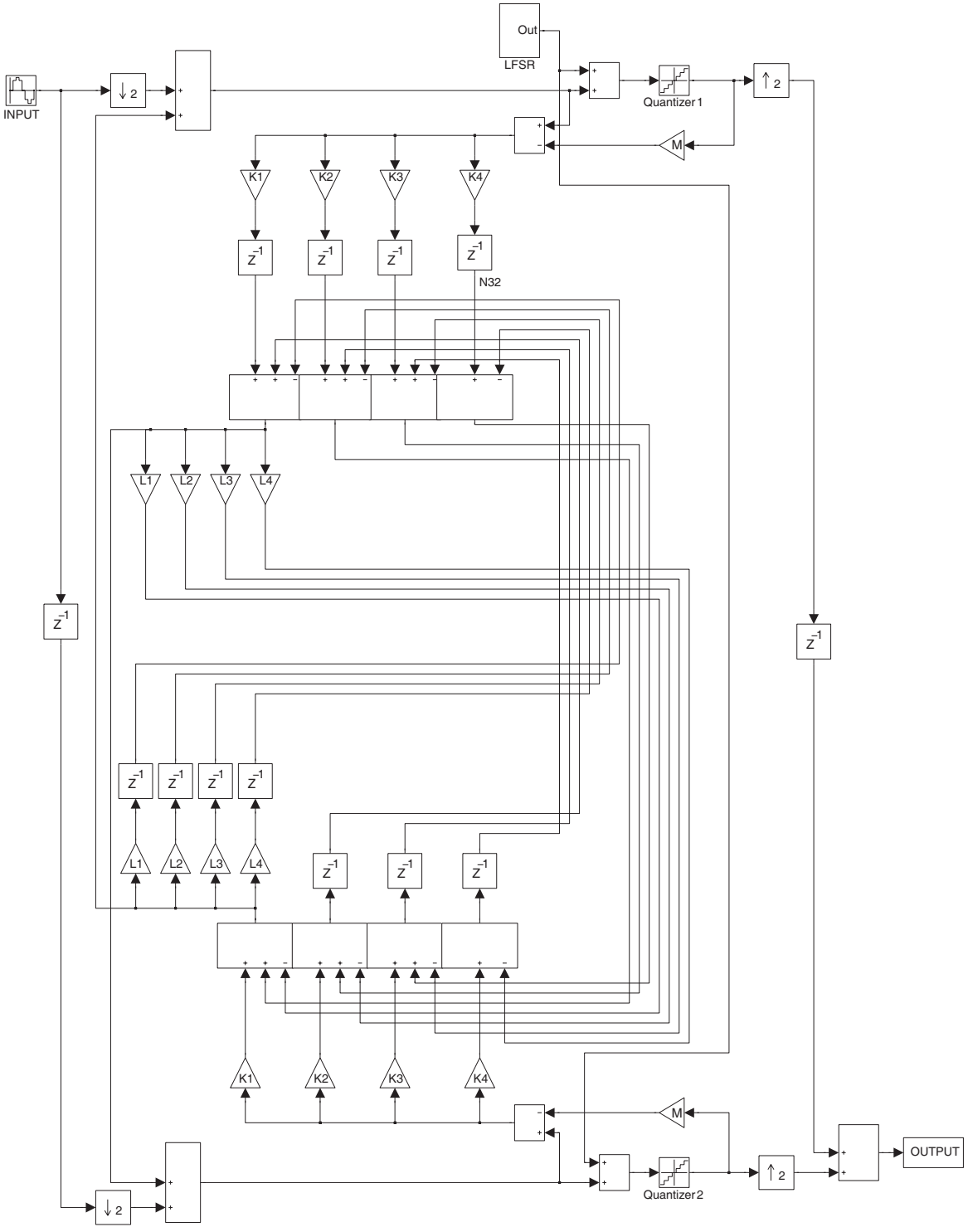



**Figure 166: 4th-order, 2-path EF Topology**

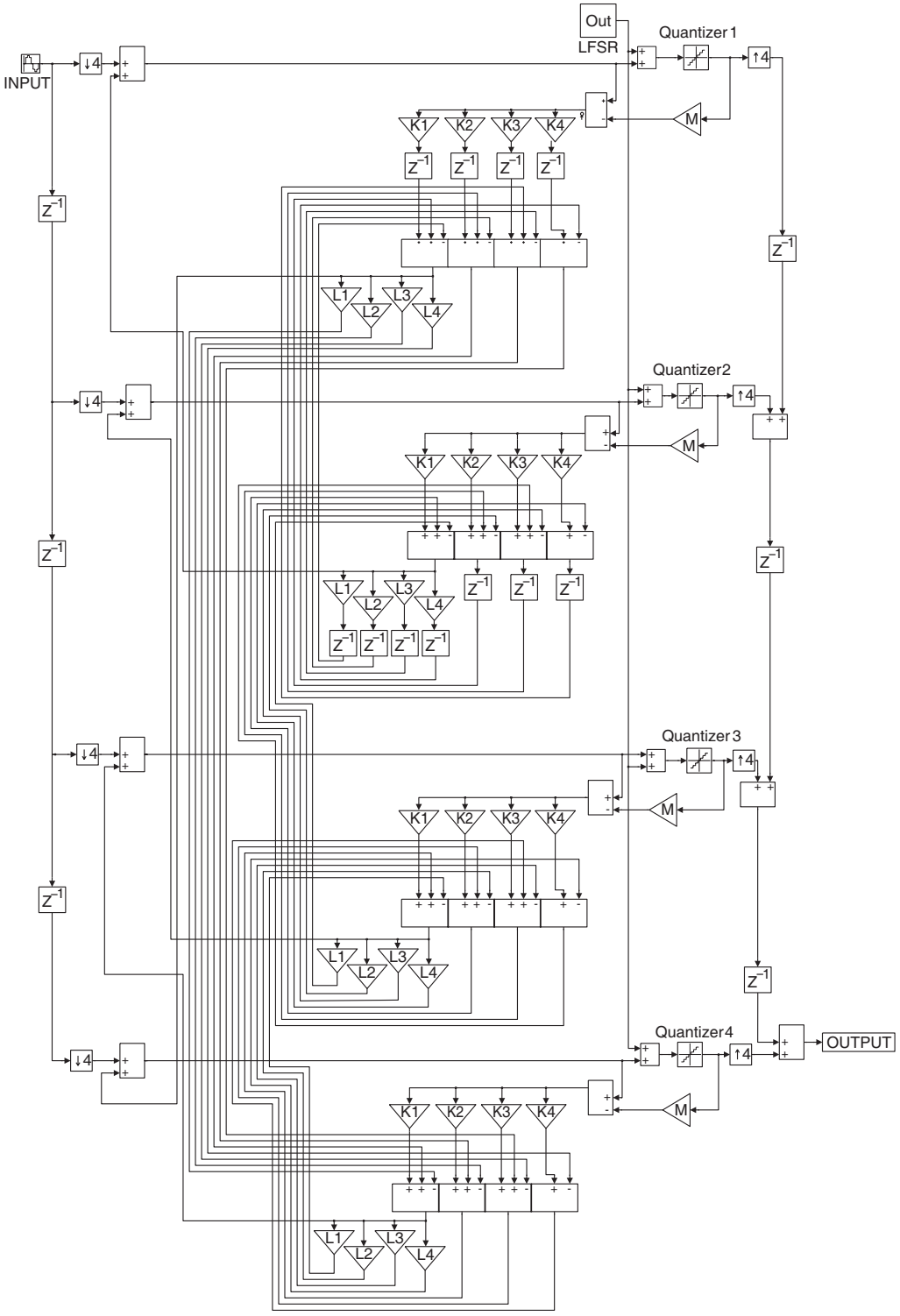



**Figure 167: 4th-order, 4-path EF Topology**

**Symbolic NTF for 6th-order EF Topology:**

$$NTF_{EF,6^{th}}(z)=\frac{1+(L_1-K_1)z^{-1}+(L_2-K_2)z^{-2}+(L_3-K_3)z^{-3}+(L_4-K_4)z^{-4}+(L_5-K_5)z^{-5}+(L_6-K_6)z^{-6}}{1+L_1z^{-1}+L_2z^{-2}+L_3z^{-3}+L_4z^{-4}+L_5z^{-5}+L_6z^{-6}}$$

(126)

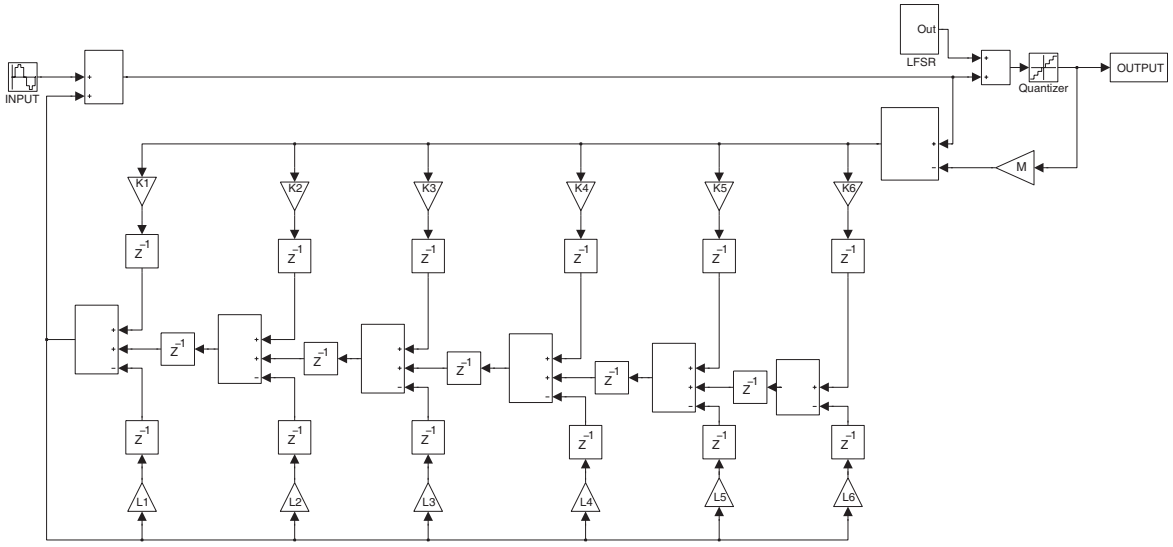



**Figure 168: 6th-order, SP EF Topology**

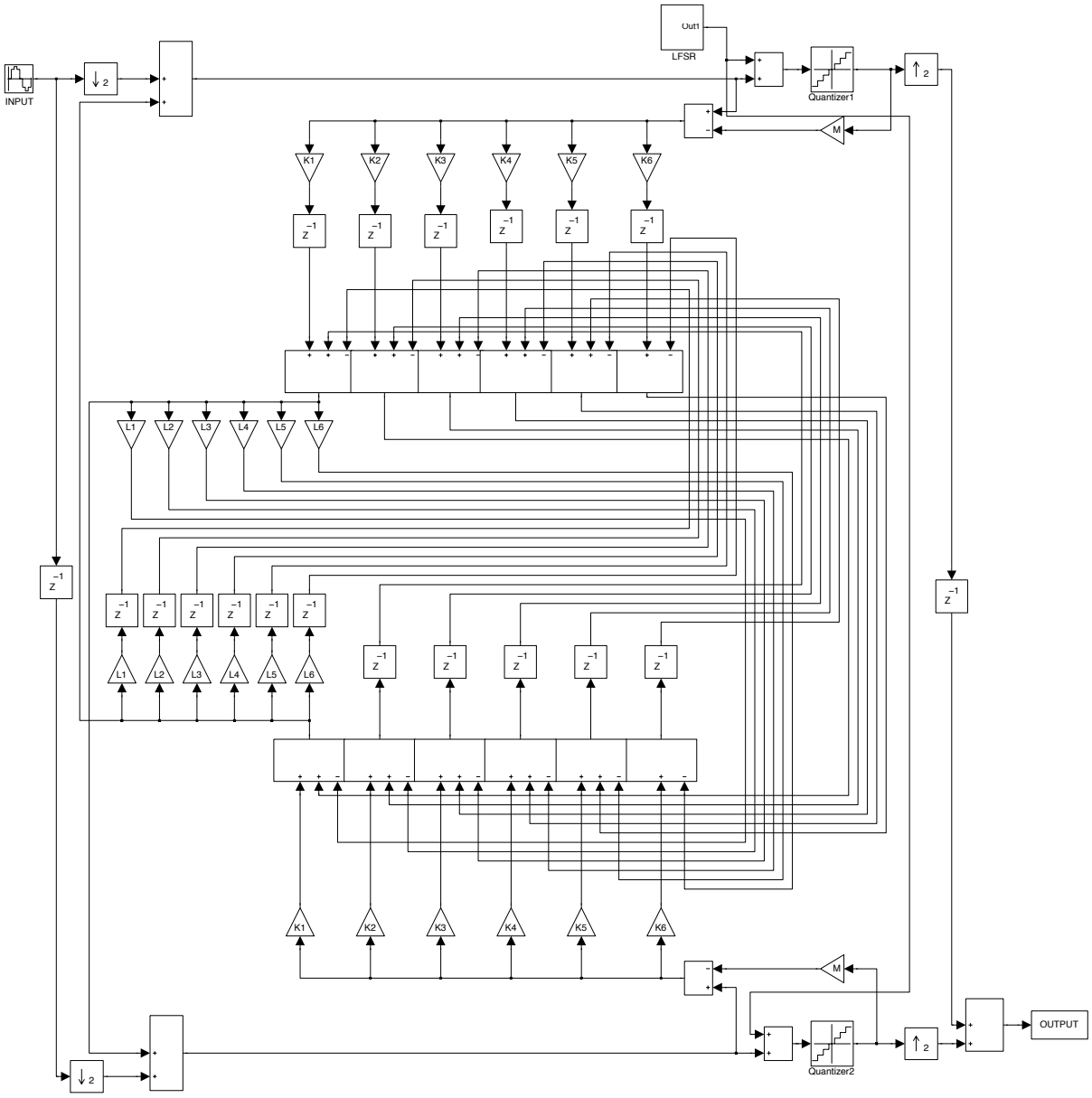



**Figure 169: 6th-order, 2-path EF Topology**

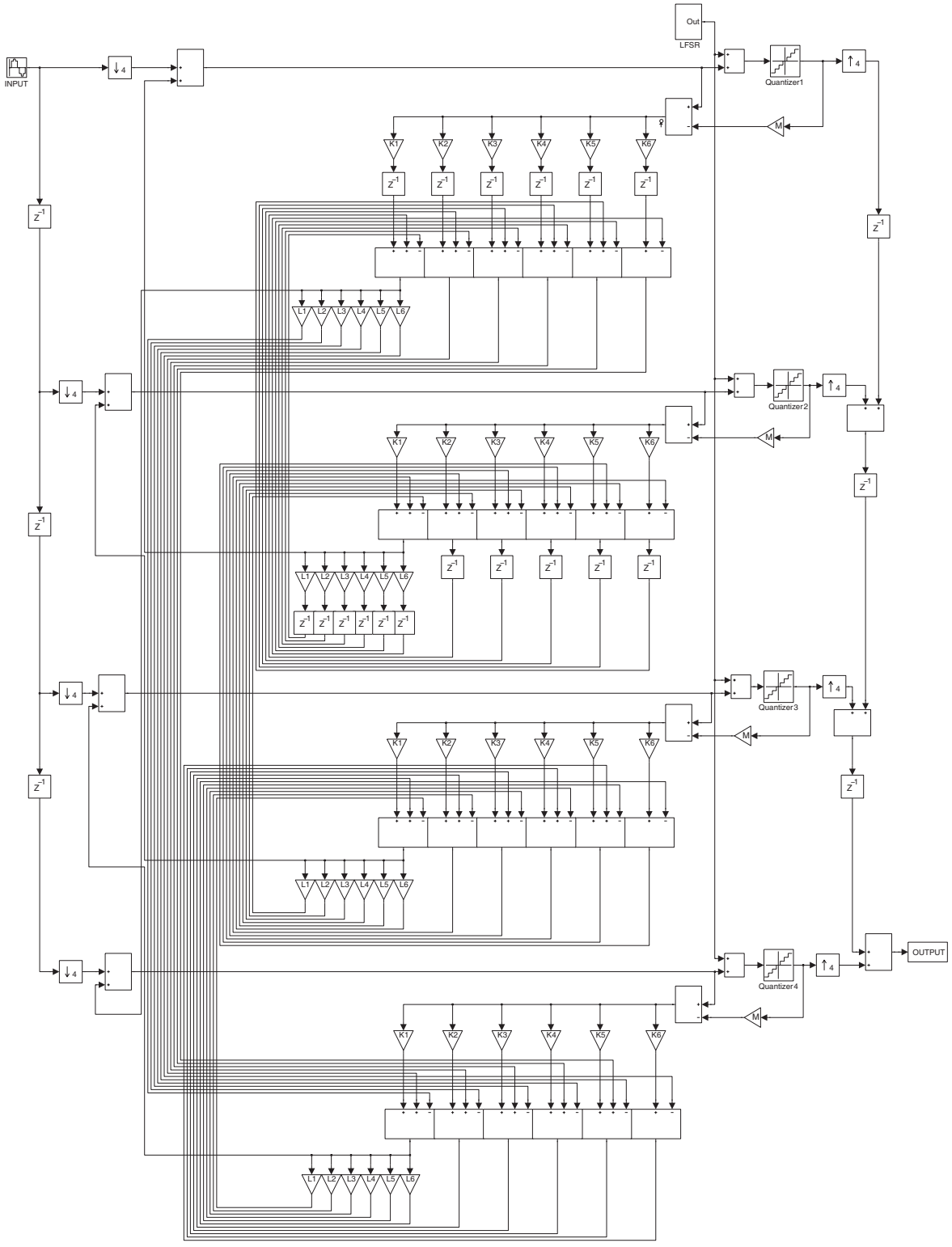



**Figure 170: 8th-order, 4-path EF Topology**

## Appendix D

The designed D/A VBP Σ-Δ modulators of the OF topology are depicted in this Appendix. Their symbolic NTFs are also provided.

**Symbolic NTF for 2nd-order OF Topology:**

$$NTF_{OF,2^{nd}}(z) = \frac{1 + L_1 z^{-1} + z^{-2}}{1 + (L_1 + K_1) z^{-1} + (1 + K_2) z^{-2}} \tag{127}$$

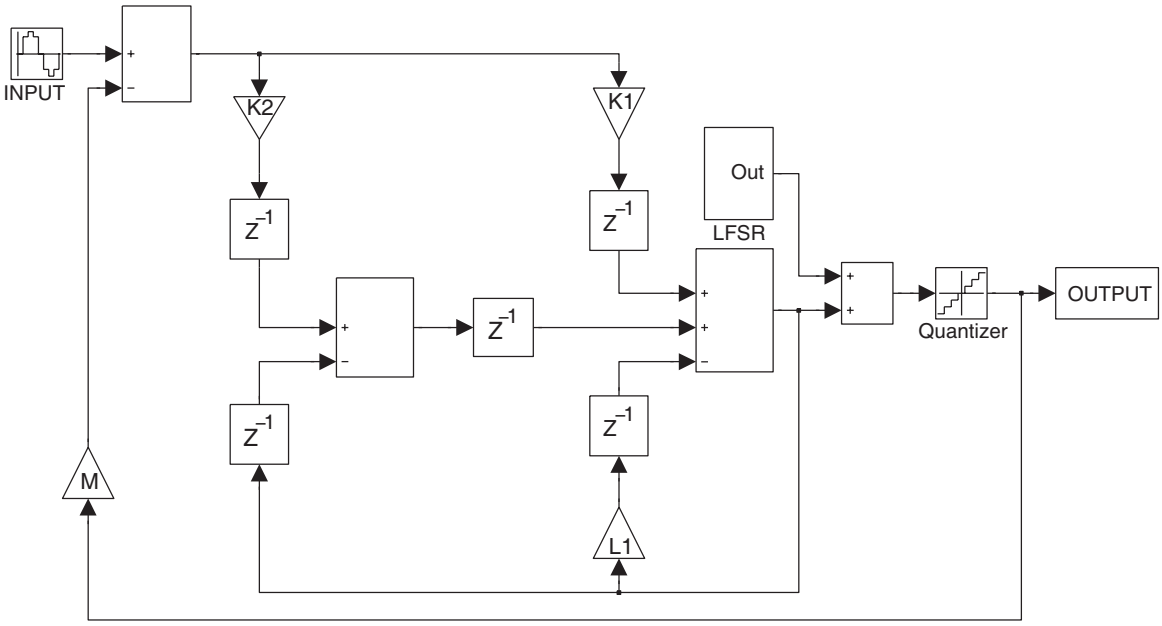



**Figure 171: 2nd-order, SP OF Topology**

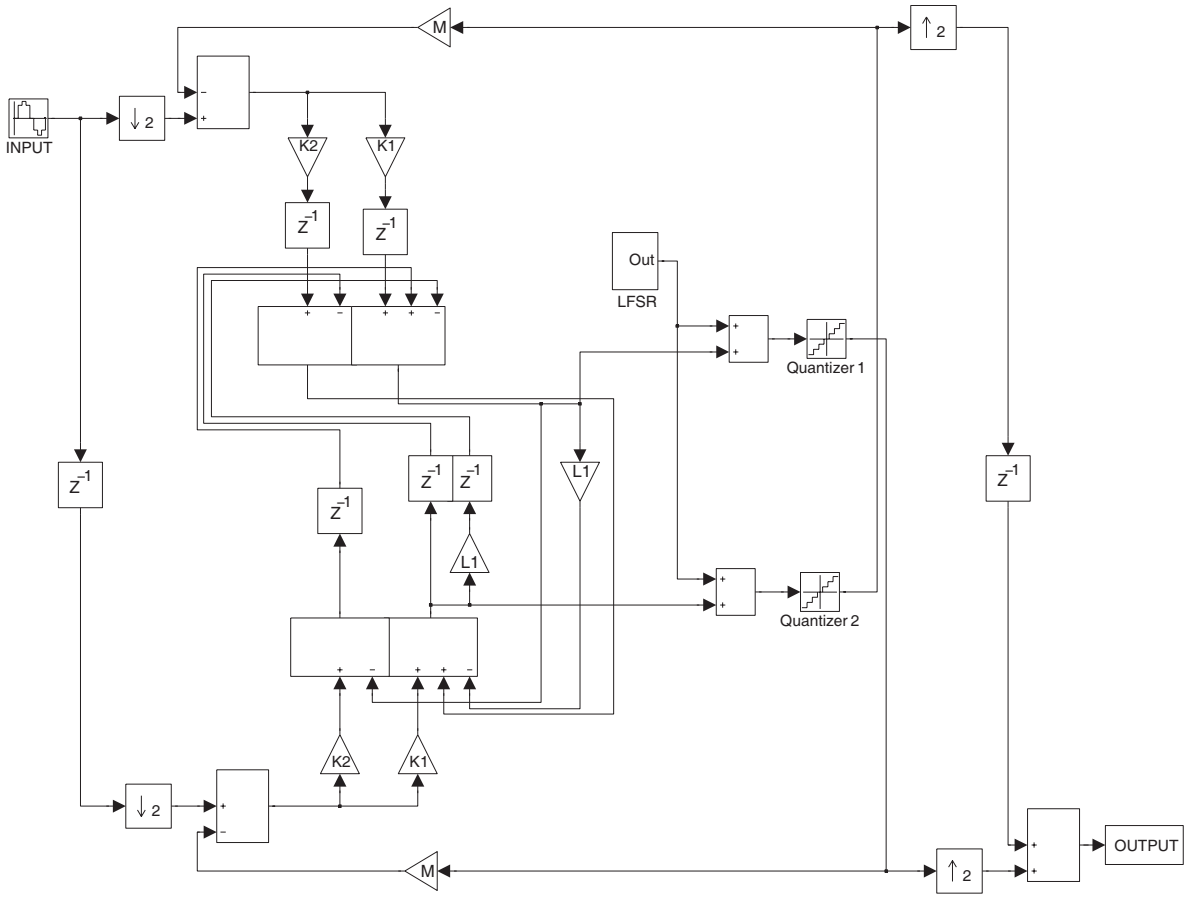



**Figure 172: 2nd-order, 2-path OF Topology**

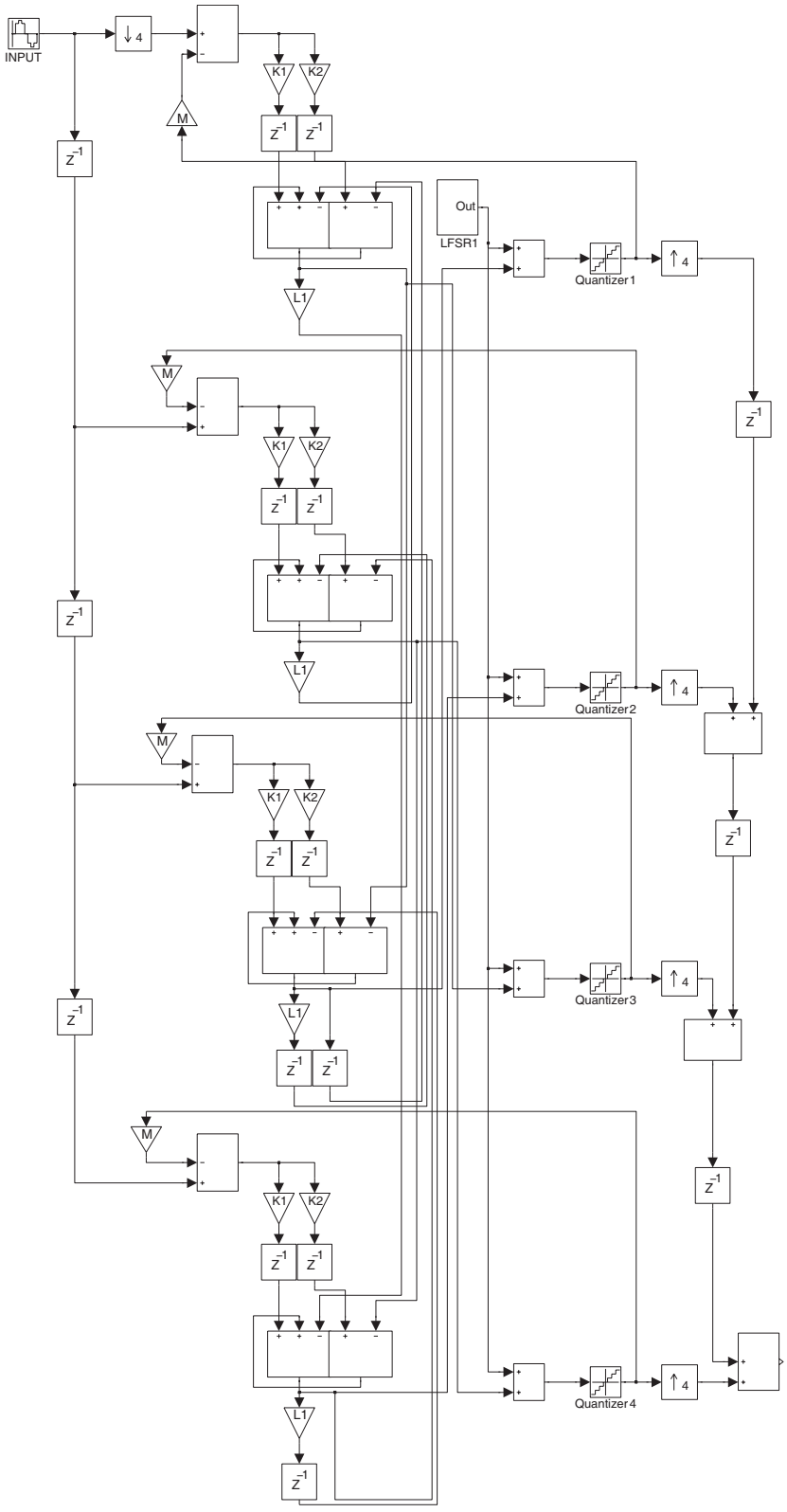



**Figure 173: 2nd-order, 4-path OF Topology**

**Symbolic NTF for 4th-order OF Topology:**

$$NTF_{OF,4^{th}}(z) = \frac{1 + L_1 z^{-1} + L_2 z^{-2} + L_1 z^{-3} + z^{-4}}{1 + (L_1 + K_1) z^{-1} + (L_2 + K_2) z^{-2} + (L_1 + K_3) z^{-3} + (1 + K_4) z^{-4}} \quad \textbf{(128)}$$

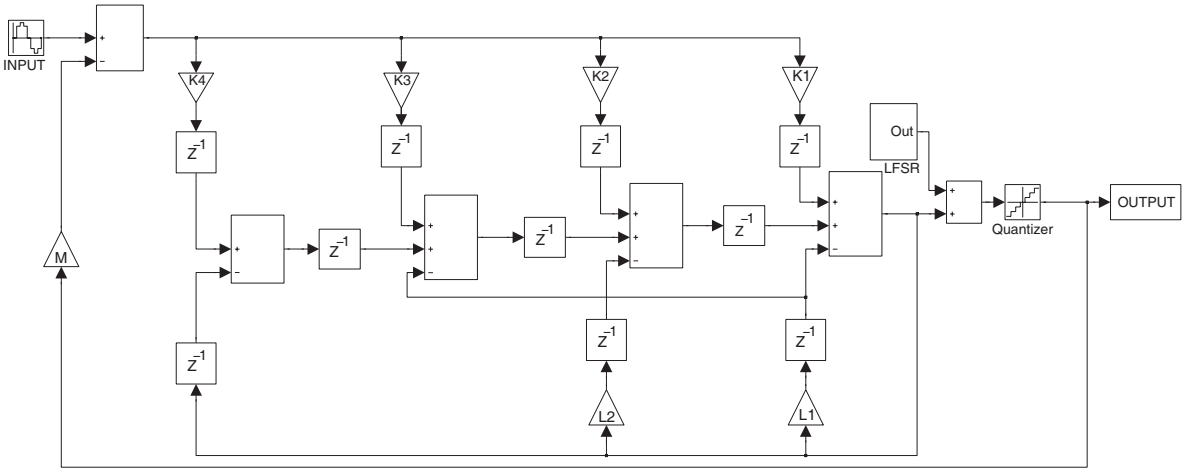



**Figure 174: 4th-order, SP OF Topology**

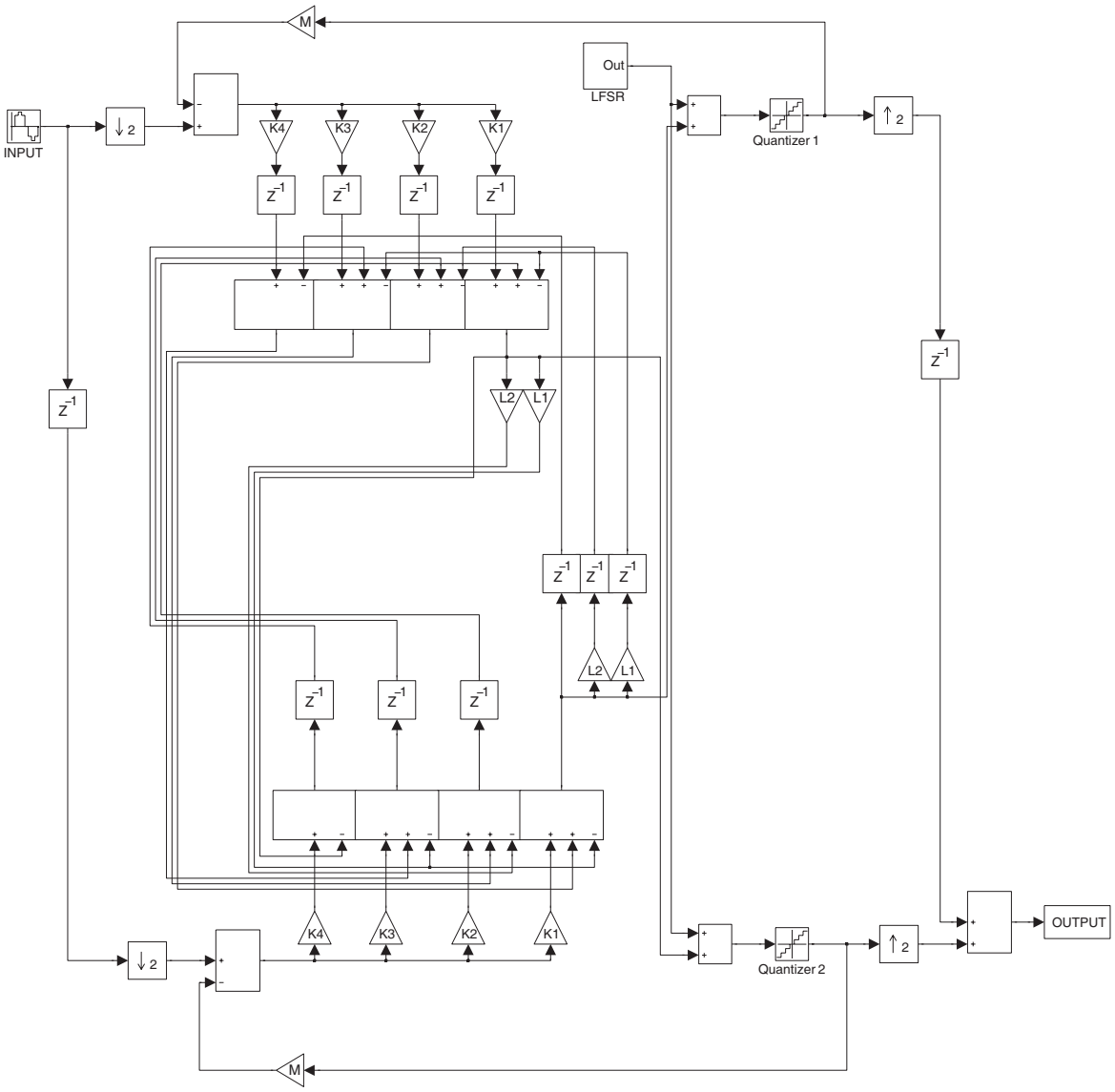



**Figure 175: 4th-order, 2-path OF Topology**

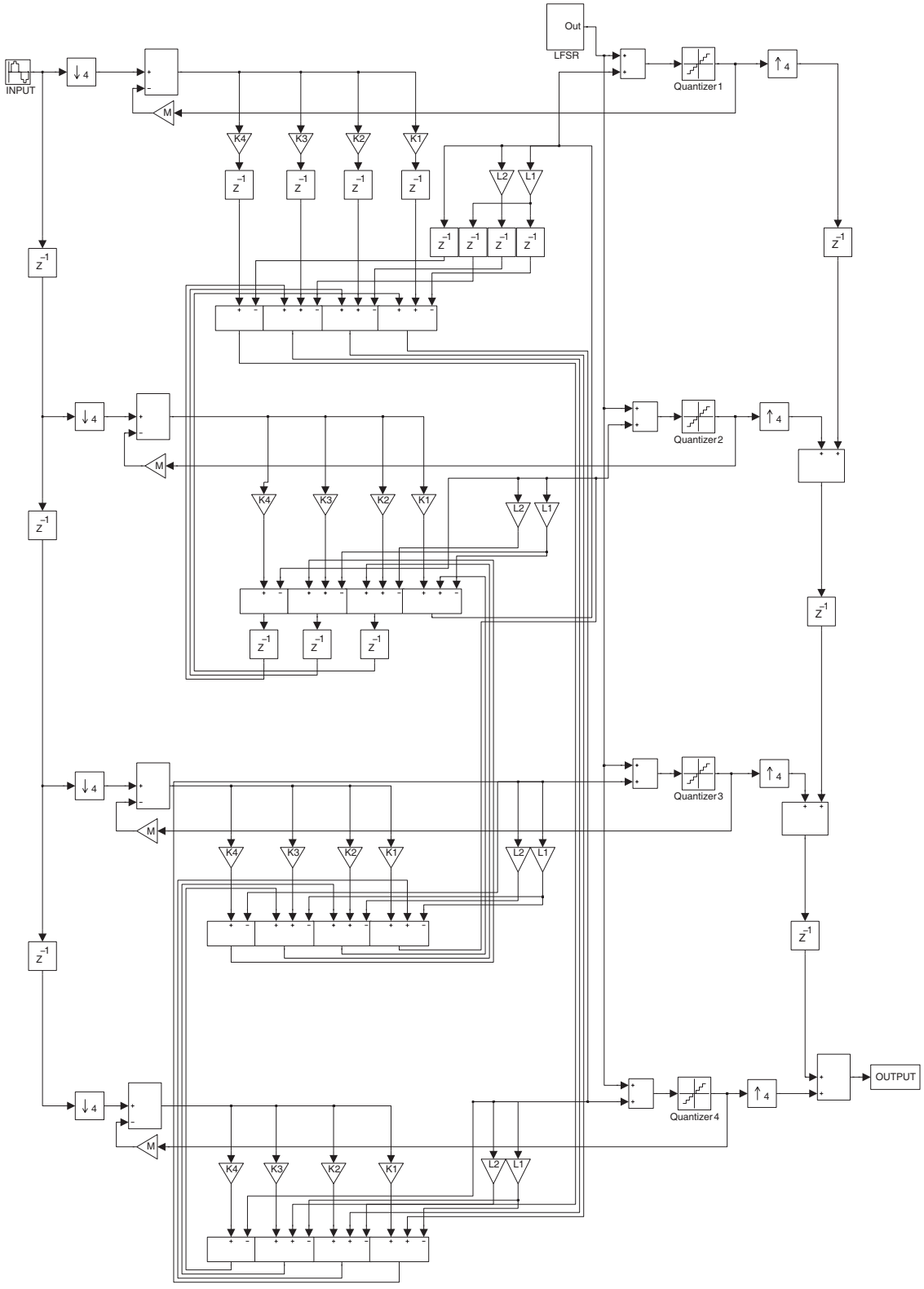



**Figure 176: 4th-order, 4-path OF Topology**

**Symbolic NTF for 6$^{th}$-order OF Topology:**

$$NTF_{OF,6^{th}}(z) = \frac{num_{6^{th}}}{den_{6^{th}}} \tag{129}$$

$$num_{6^{th}} = 1 + L_1 z^{-1} + L_2 z^{-2} + L_3 z^{-3} + L_2 z^{-4} + L_1 z^{-5} + z^{-6}$$

$$den_{6^{th}} = 1 + (L_1 + K_1) z^{-1} + (L_2 + K_2) z^{-2} + (L_3 + K_3) z^{-3} + (L_2 + K_4) z^{-4} + (L_1 + K_5) z^{-5} + (1 + K_6) z^{-6}$$

(130)

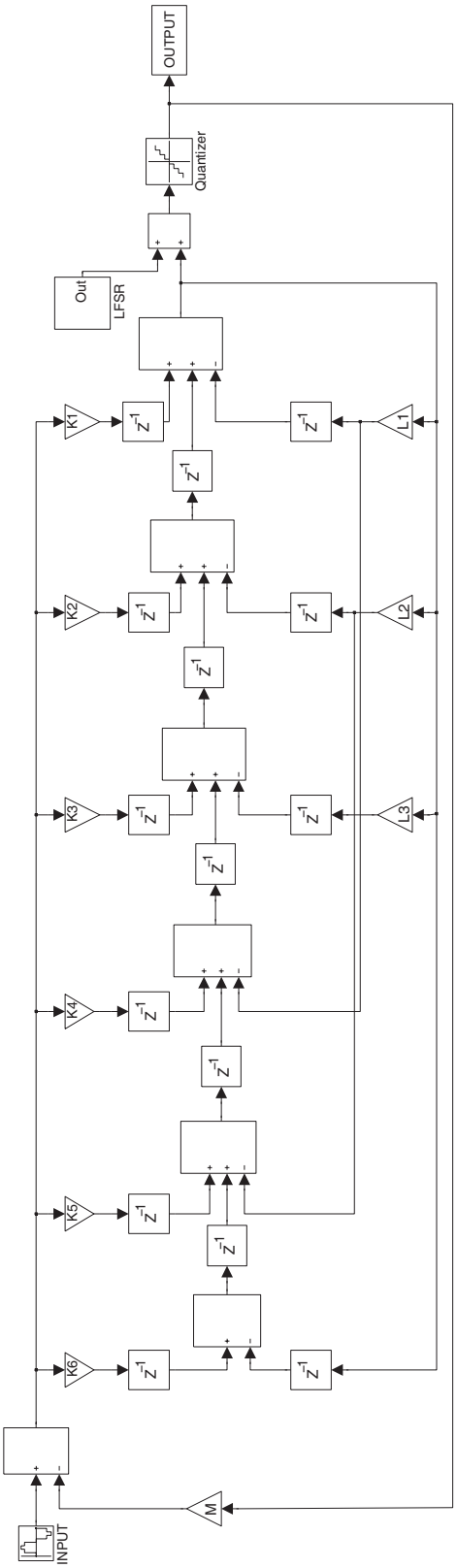



**Figure 177: 6th-order, SP OF Topology**

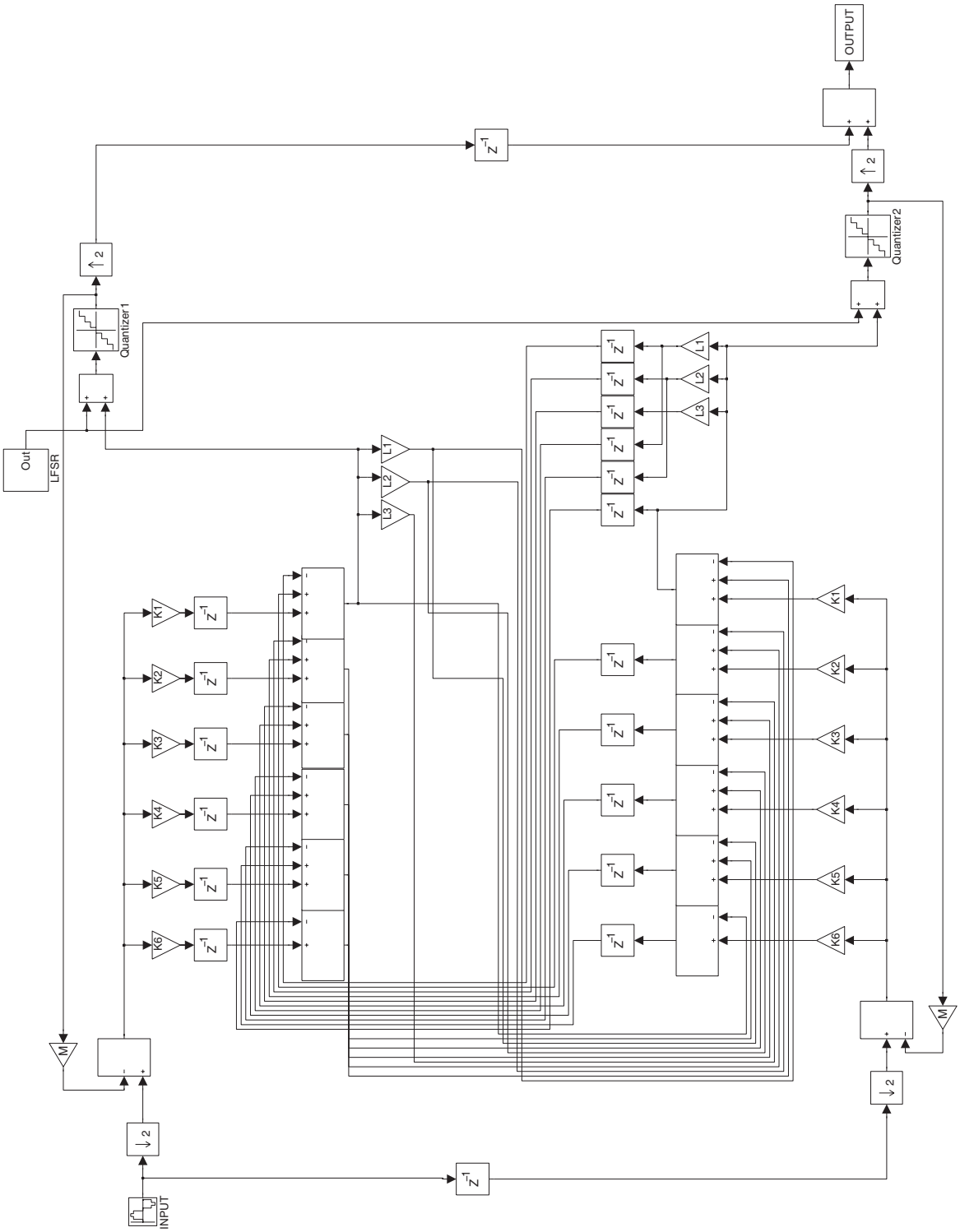



**Figure 178: 6th-order, 2-path OF Topology**

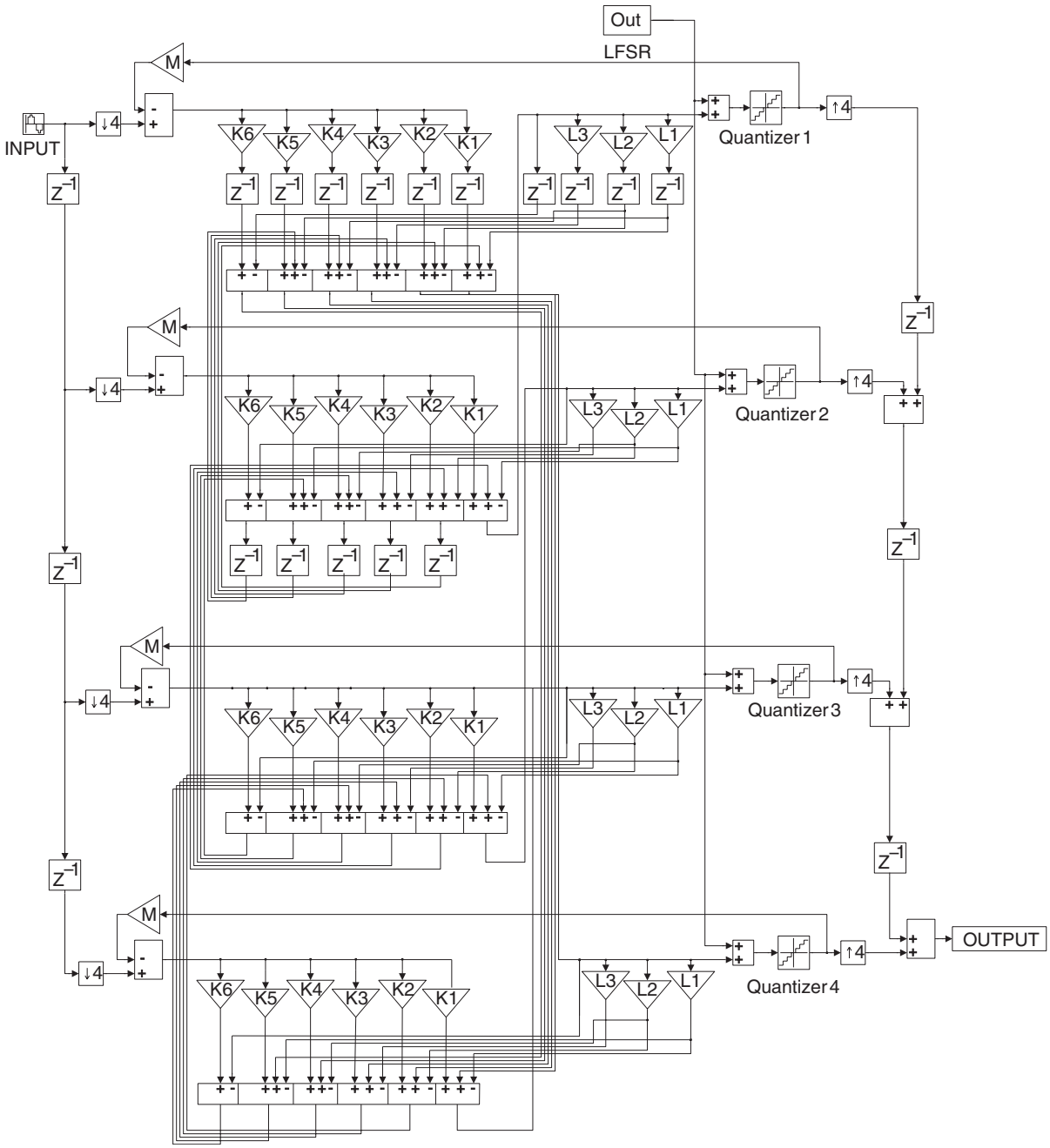



**Figure 179: 6th-order, 4-path OF Topology**

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## BIOGRAPHY

**Işıl Kalafat Kızılkaya** was born in Sinop in 1985. She received the B.E. degree from Yıldız Technical University, İstanbul, Turkey, in 2008. She received the M.E. degree from Boğaziçi University, İstanbul, Turkey in 2011.

Her master's thesis is named 'RF Front-End of a Receiver for a 3 Tesla Magnetic Resonance Imager'. The thesis mainly focused on the design of a low-power fully differential Low Noise Amplifier (LNA), operating at 123 MHz.

From 2009 to 2011 she worked as a research assistant in Yıldız Technical University. In September 2011, she joined the Department of Engineering, University of Westminster, as a research scholar. Her main areas of research interest are analog and digital signal processing circuits' design and implementation, sigma-delta based A/D and D/A converters.