Class-AB rail-to-rail CMOS buffer with bulk-driven super source followers.

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Class-AB Rail-to-Rail CMOS Buffer with Bulk-Driven Super Source Followers

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***Abstract*—This paper describes a rail-to-rail CMOS analog voltage buffer designed to have extremely low static current consumption as well as high current drive capability. The buffer employs a complementary pair of super source followers, but a bulk-driven input device with the replica-biased scheme is utilized to eliminate the DC level shift, quasi-floating gate transistors to achieve class-AB performance, and a current switch which shifts between the complementary pair to allow rail-to-rail operation. The proposed buffer has been designed for a 0.35µm CMOS technology to operate at a 1.8V supply voltage. The simulated results are provided to demonstrate that the total harmonic distortion for a 1.6Vpp 100kHz sine wave with a 68pF load is as low as -46dB, whilst the static current consumption remains under 8µA.**

I. INTRODUCTION

Voltage buffers are essential building blocks in analog and mixed-signal circuits and processing systems, especially for applications where the weak signal needs to be delivered to a large capacitive load without being distorted [1-2]. To accomplish this demand, the input capacitance of the buffer needs to be as small as possible so that the weak signal is not affected under any circumstances, and the output stage needs to have a high slew-rate performance so that the signal can remain driven with large capacitive loads. Furthermore, for applications in portable electronics, where the battery lifetime needs to be extended to the maximum as possible, the static power consumption of the buffer must be small whilst the slew-rate remains high. This suggests the use of a class-AB output stage in the buffer.

The authors recently proposed a CMOS buffer using a new circuit-design technique so-called "bulk-driven flipped voltage follower" in [4], which they demonstrated that the proposed buffer meets most of the needs mentioned above. In this paper, we present a novel CMOS buffer based on our previous work in [4] but with additional features of rail-to-rail power-efficient operation to maximize the dynamic range as much as possible whilst attaining low-static high-drive current.

II. CLASS-AB BULK-DRIVEN SUPER SOURCE FOLLOWER

This section briefly describes the previous works [1-4] using Figure 1 and Figure 2, which we have utilized to form the core part of our proposed CMOS buffer – a class-AB bulk-driven super source follower.

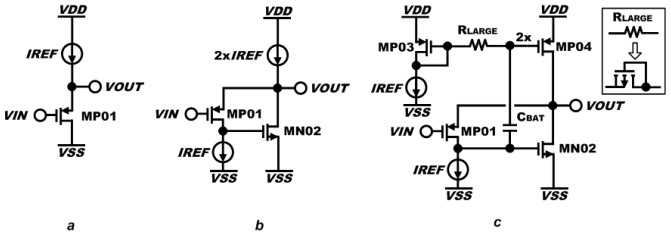

Figure 1. (a) class-A source follower, (b) class-A super source follower, and (c) class-AB super source follower proposed by Lopez-Martin *et al* [2]

Figure 1a illustrates a conventional pMOS source follower, widely used as a level-shifted voltage buffer [1-2]. If the body-effect is neglected, then the output voltage V_{OUT} follows the input voltage V_{IN} with an upward DC shift, i.e. $V_{OUT} = V_{IN} + V_{SG\mathrm{MP01}}$, where $V_{SG\mathrm{MP01}}$ is the source-to-gate voltage of the transistor MP01. In case of an nMOS source follower, V_{OUT} is instead shifted down from V_{IN}. This conventional source follower is widely used, however the drawback is that it is sensitive to resistive loads. Since the drain current of MP01 is affected by the output current, the DC-level $V_{SG\mathrm{MP01}}$ cannot be kept constant. To overcome this concern, there exists a buffer which is often referred to as a super source follower [1], as shown in Figure 1b. The topology of Figure 1b is the same as Figure 1a, but since the drain current through MP01 is biased with a constant current I_{REF} and is independent of the output current, $V_{SG\mathrm{MP01}}$ is also held constant against the output current. Today, we can observe many published proposals using this super source follower.

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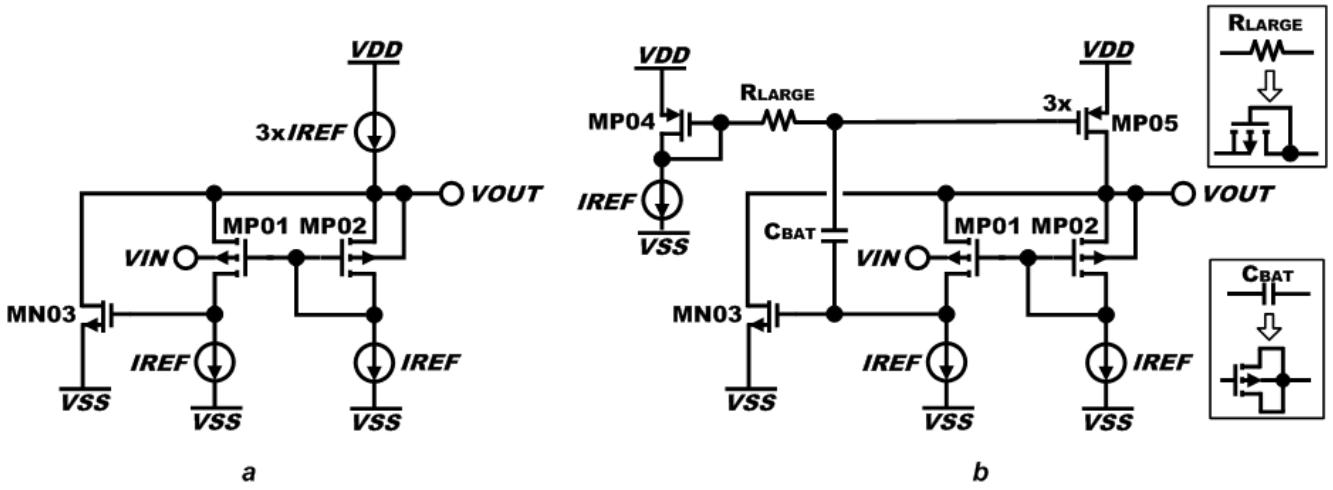

Figure 2. Bulk-driven super source followers (a) class-A operation, and (b) converting into class-AB operation using the QFG technique proposed by Ramìrez-Angulo *et al* [2-3]

Recently, A.J. Lopez-Martin *et al* emphasized in their work in [2] that despite the output becoming much insensitive to resistive loads with the super source follower, the Slew-Rate (SR) remains in class-A operation. In the case of a pMOS super source follower as shown in Figure 1b, the positive SR is limited to I_{REF}/C_L, where C_L is the load capacitance. Hence increasing I_{REF} leads to one possible approach for the SR improvement, but at a cost of larger static power consumption. To avoid this trade-off, A.J. Lopez-Martin *et al* proposed a class-AB super source follower in [2] by using a quasi-floating gate (QFG) technique presented in [3]. Their proposed circuit diagram is depicted in Figure 1c.

In Figure 1c, the gate of MP04 is weakly connected to the gate of MP03 with a large resistor R_{LARGE}, and also to the gate of MN02 with a capacitor C_{BAT}. In terms of DC characteristics, there exists no current flow across R_{LARGE} and therefore the gate voltage of MP03 and MP04 are the same. Thus the static power dissipation between Figure 1b and Figure 1c remains the same. In terms of AC characteristics, a high pass filter is formed with a cutoff frequency of $1/(2\pi R_{LARGE}C_{BAT})$, when observed from the gate of MN02 to the gate of MP04. Thus the ac element of the signal at the gate of MN02 can propagate to the gate of MP04, which in turn achieves class-AB operation without introducing any extra static current consumption. Furthermore, it is remarkable to realize in [2-3] that a unity-size diode-connected MOSFET but in the cutoff region can form a substantially large resistance of R_{LARGE}, which leads to achieving a low cutoff frequency $1/(2\pi R_{LARGE}C_{BAT})$ with a moderately small capacitance of C_{BAT}. In [2], A.J. Lopez-Martin *et al* discuss the C_{BAT} value in terms of attenuation factor α ($\approx 1/(1+C_{GS4}/C_{BAT})$). A C_{BAT} greater than 5 times C_{GS4} leads $\alpha > 0.83$, which is enough to propagate almost all frequencies except the DC component of the signal.

Figure 2a illustrates the bulk-driven version of the super source follower, which is the same type of circuit-design technique the authors previously presented in [4]. As can be observed, the input is connected to the bulk terminal of MP01 instead of its gate. MP02 is the replica of the input device MP01, i.e. MP02 and MP01 having equal transistor sizing and are biased with the identical drain current and the gate voltage. Since the bulk-terminal of MP02 is directly shorted to its source-terminal, MP01 tends to replicate the conditions of MP02 and hence the source-terminal follows the input voltage with no DC voltage in between, thus $V_{OUT} = V_{IN}$. Remarkably, the input capacitance C_{IN} of this type of buffer can be small because of the small junction capacitance of MP01. The junction capacitance of a MOSFET C_j is given by:

$$C_j = C_{j0} / (1+ (V_{SB} / \Phi_0))^{0.5} \qquad (1)$$

where C_{j0} is the zero-bias (V_{SB}=0) junction capacitance, V_{SB} is the bulk-to-source voltage, and Φ_0 is the bulk junction potential. Since V_{SB} of MP01 in Figure 1d is designed to be zero, the junction capacitance of MP01 is constant at C_{j0}. We will discuss the simulated value of C_{IN} later on in this paper.

Figure 2b shows a class-AB bulk-driven super source follower, where the class-AB operation has been implemented to Figure 1d with the same technique proposed by A.J. Lopez-Martin *et al* in [2]. However, we have chosen a modified approach for implementing the C_{BAT}. Ramìrez-Angulo *et al* stated the significance of the QFG technique in [3] that the actual value of C_{BAT} does not need to be highly accurate, as long as even a low frequency signal can be coupled. Owing to and appreciating this fact, we attempted to eliminate the need for a poly-poly capacitor, and chose to form the C_{BAT} with a MOSFET as shown in Figure 1e. The authors observe that the size of the MOSFET five times larger than MP05 is more than enough to achieve good attenuation.

III. Proposed Rail-to-Rail Class-AB CMOS Buffer

We applied the bulk-driven super source follower as shown in Figure 2b in our design to propose a rail-to-rail power-efficient CMOS voltage buffer. Figure 3 illustrates the circuit diagram of our proposal.

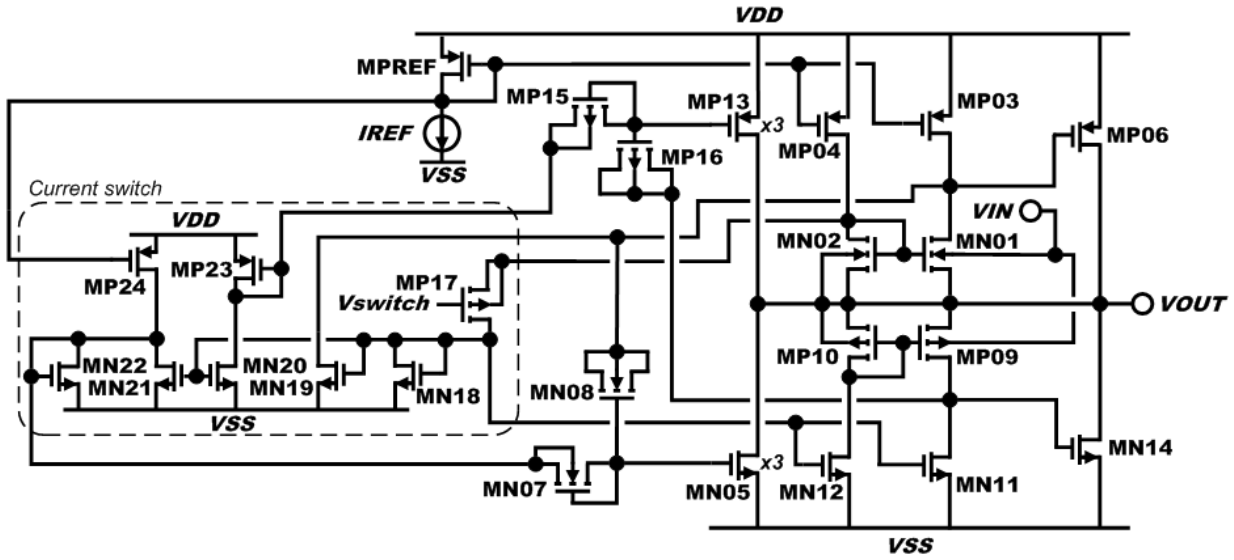

Figure 3. Proposed class-AB rail-to-rail CMOS analog buffer using a complementary pair of bulk-driven super source followers

The operation principle of Figure 3 is very simple to follow. From MN01 to MN08 and from MP09 to MP16 form a nMOS-type and pMOS-type of the bulk-driven super source follower, respectively, and from MP17 to MP24 forms a current switch. The *Vswitch* at the gate of MP17 determines the switching point between the two types of follower. When V_{IN} (and thus V_{OUT}) is close to *VSS* the pMOS follower is active while the nMOS follower is off, and when V_{IN} moves towards *VDD*, V_{OUT} and the drain voltage of MN02 also increase and eventually MP17 turns on to reduce the drain current of MN01, MN02 and MN05 (i.e. to shut off the nMOS follower) and instead to increase the drain current of MP09, MP10 and MP13 (i.e. to activate the pMOS follower) to continue the buffer operation.

IV. Simulated Results

Using a 0.35µm CMOS process, we designed to operate the circuit of Figure 3 at 1.8V supply voltage and simulated with the BSIM3 MOSFET models. Table 1 shows the simulation results summarizing the overall performance.

TABLE I. Simulated results of the overall performance of Figure 3

Parameter	Simulated Results
-3dB frequency	6MHz
Static current dissipation	5µA to 8µA for V_{IN} sweeping between *VDD* and *VSS*
Slew rate	SR+ = 9.3V/µs, SR- = 13.7Vµs
Input capacitance	17fF
THD	-52dB (1.6Vpp@100kHz, CL=10pF) -50dB (1.6Vpp@100kHz, CL=22pF) -47dB (1.6Vpp@100kHz, CL=47pF) -46dB (1.6Vpp@100kHz, CL=68pF)
Simulated condition: *VDD*=1.8V, *VSS*=0V, *VSW*=0.9V, CL= 10pF	

From Table 1 we emphasize that the proposed buffer of Figure 2 meets the demands we discussed in the Introduction. The input capacitance is as small as 17fF, the SR is very high such that the buffer can deliver a 1.6Vpp 100kHz signal with a total harmonic distortion as low as -46dB when the capacitive load is as large as 68pF, whilst the static current consumption remains under 8µA. Figure 4 is the simulated results of DC-sweeping the V_{IN}, which indicates that the offset remains small throughout the rail-to-rail operation.

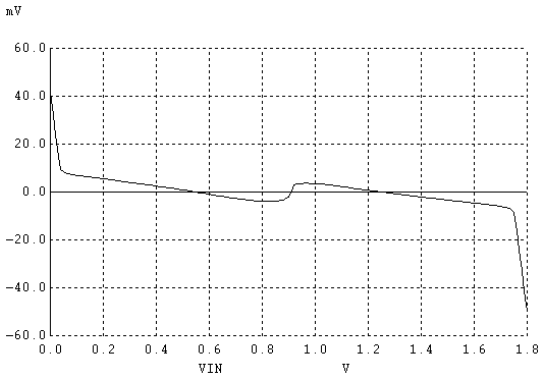

Figure 4. Simulated results of the DC offset voltage versus V_{IN} (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Fig 5 indicates the simulated results of the static current dissipation with DC sweeping the V_{IN} between *VDD* and *VSS*.

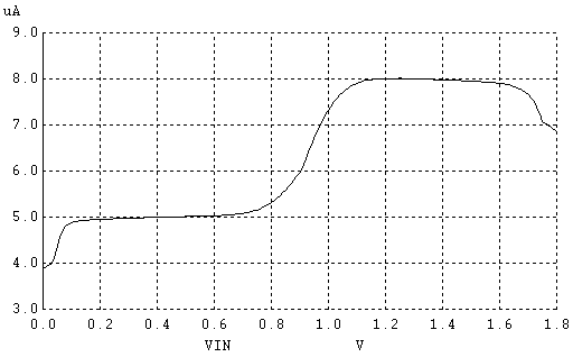

Figure 5. Simulated results of the static current dissipation (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 6 illustrates the simulated results of the V_{OUT} and the I_{OUT} with V_{IN} having 1.6V peak-to-peak 100kHz sine wave signal and a capacitive load CL of 68pF.

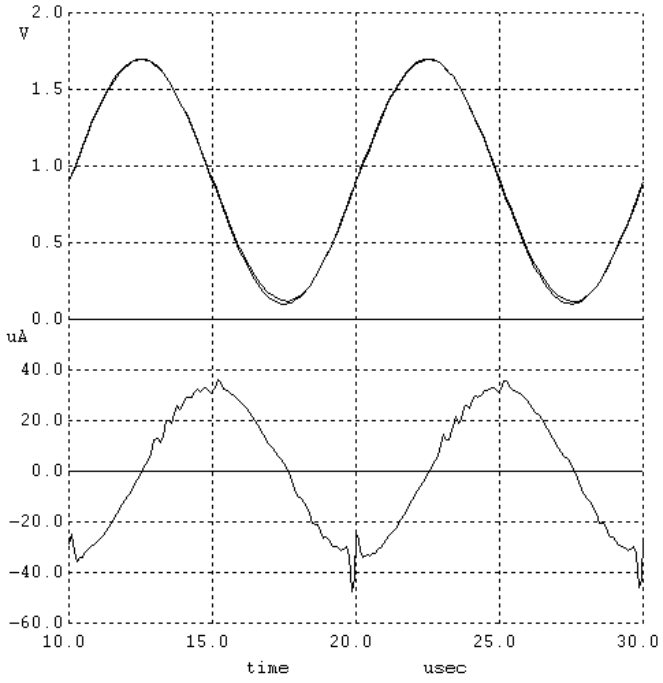

Figure 6. V_{OUT} vs V_{IN} and I_{OUT} with V_{IN} = 1.6Vpp 100kHz sinewave and CL =68pF (*VDD*=1.8V, *VSS*=0V, *Vswitch*=0.9V)

Figure 5 and Figure 6 show clearly that the goal of excellent power efficiency is achieved – during the static mode the current dissipation of the proposed buffer remains under 8μA, whereas I_{OUT} can be pushed and pulled to approximately ±40μA during the dynamic V_{IN} so that the Total Harmonic Distortion (THD) of V_{OUT} can be as small as -46dB even the CL is as large as 68pF.

To verify the input capacitance of the proposed buffer shown in Figure 3, we have set up the simulation condition as shown in Figure 7.

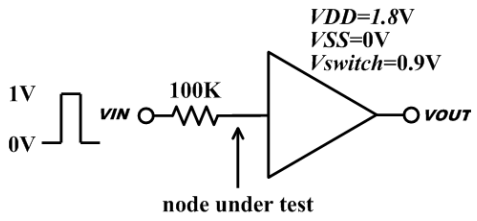

Figure 7. Simulation setup for the input capacitance

The simulated plot of the setup in Figure 7 is given in Figure 8.

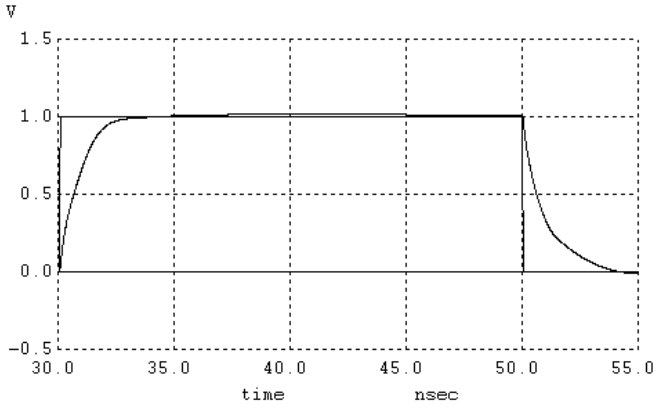

Figure 8. Simulation results for the Figure 7 setup

From Figure 8, the time constant τ was found to be 1.7ns. Hence, the input capacitance was determined as 17fF (τ=RC).

V. CONCLUSION

A new design technique for a CMOS buffer using the complementary pair of bulk-driven super followers has been presented. Applying the bulk-driven MOSFETs with the replica-biased scheme and the QFG techniques into the buffer enabled us to have a few femto-Farad range of the input capacitance so that the weak input signals are minimally affected, whilst delivering the signal without much distortion even if the capacitive load is very large. The static current consumption can remain small too. Our proposed buffer can become a serious contender for portable electronics needing to deliver weak analogue signals into large capacitive loads with as little distortion as possible.

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