Investigation of Stepwise Charging Circuits for Power-Clock Generation in Adiabatic Logic

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***Abstract*— The generation of power-clocks in adiabatic integrated circuits is investigated. Specifically, we consider stepwise charging strategies (2, 3, 4, 5, 6, 7, and 8-step) based on tank-capacitor circuits, comparing them in terms of their energy recovery properties and complexity. We show that energy recovery achievable depends on the tank-capacitor size. We also show that tank-capacitor sizes can be reduced as their number increases concluding that combined tank capacitance (CTT) versus load capacitance (CL) ratio is the significant parameter. We propose that using a CTT/CL ratio of 10 and using a 4-step charging power-clock constitute appropriate trade-offs in practical circuits.**

Keywords—power-clocks; adiabatic circuits; stepwise charging; tank-capacitor; energy recovery;

I. INTRODUCTION

In VLSI systems, recent advancements in mobile, high performance computing devices have resulted in energy efficient design being the major concern. Adiabatic circuits are capable of operating with substantially less energy dissipation compared to conventional CMOS circuits [1]. There are several principles shared by adiabatic circuits. These include only turning switches off when no current is flowing through them, only turning switches on when there is no potential difference across them and then using a slowly changing power-supply/clock -the so-called "power-clock" to evaluate the function [2]. A slowly changing power-clock allows approximately constant current charging/discharging and by avoiding current surges, the circuit dissipates less energy [3]. The use of power-clocks also makes possible the recycling of charge, enabling energy to be recovered. To produce approximately constant current charging/discharging, the power-clock should ideally be a ramp which rises and falls linearly. Such a ramp can be approximated using resonant inductor circuits [4] and step charging circuits [5]-[7]. The use of inductors presents a problem with on-chip integration; therefore, step charging circuits offer a more promising solution. Such a power-clock which rises and falls in a number of steps, n is shown simplified in Fig. 1(b). This can be achieved using a step charging circuit [5].

In literature, there are several papers that addressed the design of step charging circuits for adiabatic charging and discharging. Consideration is mostly given to circuit topology, step charging waveform generation and stability of the step charging circuits [8]-[14]. However, the important considerations that have been found to be missing in all of the papers are; i) the energy recovery achievable in the step charging circuits; ii) what should be the ratio of tank-capacitance to load capacitance, which can deliver potential energy benefits; and iii) the number of steps in a step charging circuits that will constitute an appropriate trade-offs in terms of energy recovery and circuit complexity.

Energy recovery determines the efficiency of the adiabatic circuits, therefore an important parameter to be considered for the design of adiabatic circuits. In adiabatic circuits, the step charging power-clock makes possible the recycling of charge, enabling energy to be recovered. Thus it is important to study the factors that decide the energy recovery achievable in step charging circuits.

Energy recovery, E_R, in an adiabatic circuit can be defined as the portion of the energy supplied to the circuit that can be recovered from the circuit and can be reused for the subsequent cycles. It is calculated as the difference of energy supplied, E_S, and energy dissipation, E_D, :

$$E_R = E_S - E_D \quad (1)$$

percentage energy recovery is calculated as:

$$\% E_R = (E_R / E_S) \times 100. \quad (2)$$

In [8] the authors presented a step charging circuit which is independent of the tank-capacitor topology that generates the step charging waveform. However, the ratio of the tank-capacitors to load capacitor used is 270. Similarly, in [9], [10] the authors discuss the stability of a step charging circuit which uses tank-capacitors connected in series. However, the ratio of the tank-capacitors to load capacitor used is 750. In [11] a step charging circuit with an equalizing capacitor that equalizes the node voltages of the tank-capacitors by connecting "touching" them with the equalizing capacitor is presented. The stability of the step charging circuit was also investigated by changing the order in which the tank-capacitor nodes were connected "touched" [11] with the equalizing capacitor. However, the ratio between tank-capacitors and the equalizing capacitor used was 300. In [12] the authors presented a step charging circuit and the stability of the step charging circuit was considered. It has been mentioned in the paper that the step charging circuit stays stable even if the value of the load capacitor changes significantly when the size of the tank-capacitor is much larger than the load capacitor. However, nothing has been mentioned about how large the size of the tank-capacitance should be in comparison to the load capacitance in order to ensure stability of the step charging circuit. In [13], [14] the adiabatic stepwise charging and discharging of a capacitor with an inductor current that controlled the switching transistors was

demonstrated experimentally and the power consumption was investigated as the function of the number of steps.

All the above cited references so far work around using a large tank-capacitator value for stability. Large tank-capacitors incur high silicon area cost and presents with the difficulty of on-chip integration. This can be a problem for the applications that require low power operation and have area constraint. Therefore, it is worth investigating what should be the relationship of total tank-capacitance to load capacitance that can deliver potential energy benefits with lower silicon area cost and ensure stable operation.

In this paper simulations were performed to investigate the appropriate ratio of *total* tank-capacitance to load capacitance which can deliver potential energy benefits in 2, 3, 4, 5, 6, 7, and 8-step charging strategies based on tank capacitor circuits. We have defined a new metric called "*total* tank-capacitance" C Total Tank (CTT) which denotes the total of all the tank-capacitor values in a step charging circuit. To ensure approximately equal step sizes, all the tank-capacitors are made equal. The step charging circuits (2, 3, 4, 5, 6, 7, and 8-step) were also compared among themselves to investigate the number of steps that constitute the appropriate trade-offs in terms of energy recovery properties and circuit complexity. This is because as the number of step in a step charging circuit increases, energy dissipation improves at the cost of increased circuit complexity.

The work presented in this paper has not been compared with any of the previously mentioned references[8]-[14] because none of the above mentioned references considered and reported results relating to energy recovery for their step charging circuits. Also no discussion about the appropriate ratio of total tank-capacitance to load capacitance was mentioned in any of the above cited references. To the author's best knowledge this is a first in this area. This paper is organized as follows; In section II, the step charging circuit is discussed. In section III, simulation results are discussed. The paper is concluded in section IV.

II. Step Charging Circuit

The basic structure of an n-step charging circuit using tank- capacitors is shown in Fig. 1(a), driving a capacitive load, CL [5]. Each switch is momentarily closed in ascending order from S_1 to S_{n+1} and back to S_1. In steady state, this produces a step-like waveform as shown in Fig. 1(b)

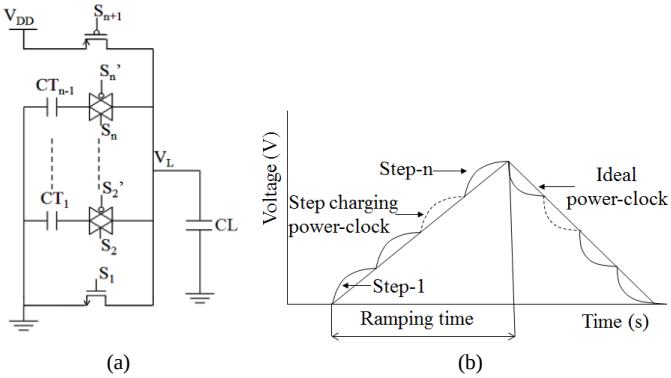

Fig. 1. (a) n-step charging circuit [5] (b) Step charging output waveform as an approximation of a linear power-clock.

In n-step charging, the load capacitor is charged from 0 to V_{DD}/n, under the constant voltage, V_{DD}/n then from V_{DD}/n to $2V_{DD}/n$, under the constant voltage, $2V_{DD}/n$ and finally from $(n-1)V_{DD}/n$ to V_{DD} under V_{DD}. This implies that supply, V_{DD}, charges the load capacitance from $(n-1)V_{DD}/n$ to V_{DD} instead of charging from 0 to V_{DD}. Therefore, the current from the supply to the load capacitance is reduced to 1/n of that of a conventional case, which means that the energy from the V_{DD} supply is decreased to 1/n.

The energy dissipation in a step charging circuit depends on the number of steps, n. Each step, in a step charging circuit dissipates $CLV_{DD}^2/2n^2$ Joules of energy, if all the voltage steps are equal. Therefore, the total energy dissipated in a circuit powered by a stepwise charging circuit is given by the expression below

$$E_D = nE_{step} = CLV_{DD}^2/2n \qquad (3)$$

Where, $E_{step} = CLV_{DD}^2/2n^2$ and n is the number of steps. The above expression shows that the energy dissipation is reduced to 1/n in n-step charging compared to the conventional direct charging. The conventional direct charging corresponds to n=1.

All the switches of the step charging circuit of Fig. 1(a) are CMOS transmission gates except the switches to V_{DD} and ground which can be simple pMOS and nMOS transistors respectively. The switches of the step charging circuit are controlled using a Finite State Machine (FSM). As the number of step increases, the waveform becomes a progressively better approximation to a ramp and energy performance is thereby improved [6].

III. Simulation Results

To measure the energy recovery achievable by 2, 3, 4, 5, 6, 7 and 8-step charging circuits, a 2-input Positive Feedback Adiabatic Logic (PFAL) [15],[16] AND/NAND gate, as shown in Fig. 2, was used as the test circuit of Fig. 3.

The simulations have been performed using the single test circuit because the ratio of total tank-capacitance to load capacitance (CTT/CL) is considered for the step charging circuits.

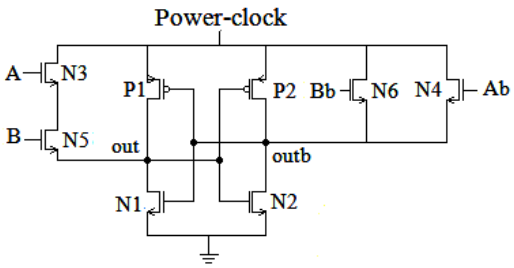

Fig. 2. Test circuit: PFAL Adiabatic AND/NAND gate [15].

The power-clock generator comprises the step charging circuit of Fig. 1(a) together with its FSM. Fig. 3 shows this generator driving the test circuit.

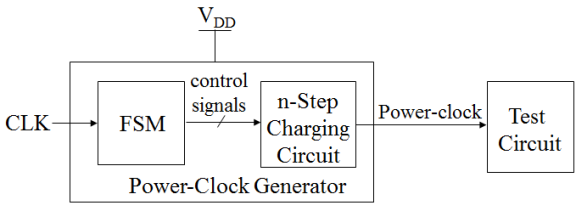

Fig. 3. General block diagram of an Adiabatic System.

Simulations were performed in a 'typical typical' process corner using TSMC 180nm CMOS process at 1.8V power supply. All the transistors in the step charging circuits and the test circuit were kept at minimum dimensions (Wmin=220nm, Lmin=180nm) except for the width of the pMOS switch to VDD in step charging circuits which was set at Wp= 440nm, with a view to equalising its performance with respect to the nMOS switch, S1. Simulations were performed with equal L-H (Low-to-High) and H-L (High-to-Low) ramping times of 50ns, 100ns, 200ns, and 400ns to investigate the effect of ramping time on energy recovery. The tank-capacitors of the step charging circuit of Fig. 1(a) require a numbers of cycles (20-30) to settle. For this reason, all measurements were taken after the circuit had reached steady state.

Energy recovery achievable by 2, 3, 4, 5, 6, 7 and 8-step charging circuits at different CTT/CL ratios was measured. The simulation results shown in Fig. 4 (a), (b), (c) and (d) illustrate the correlation between CTT/CL ratios and energy recovery at ramping times of 50ns, 100ns, 200ns and 400ns. The plots show that increasing the CTT/CL ratio above, say, 10, offers relatively little improvement in energy recovery. This suggests that as a design rule, a CTT/CL ratio of 10 is appropriate. Fig. 4 (a), (b), (c) and (d) also shows the "diminishing returns" of increasing number of steps against improvements in energy recovery. It shows an improvement of about 10%, 9%, 4%,3%, 2% and 1% in energy recovery against increasing number of steps from 2 to 8 respectively at a CTT/CL ratio of 10.

The relatively small improvement between 4 and 5-step charging circuit suggests that 4-step charging circuit might be considered an adequate tradeoff between complexity and energy recovery. Also, keeping the CTT/CL ratio of 10 ensures the stable operation of the step charging circuits.

The reported results do not include the energy cost of operating the switches in the step charging circuit/FSM controller. These are largely fixed overheads and, in a chip

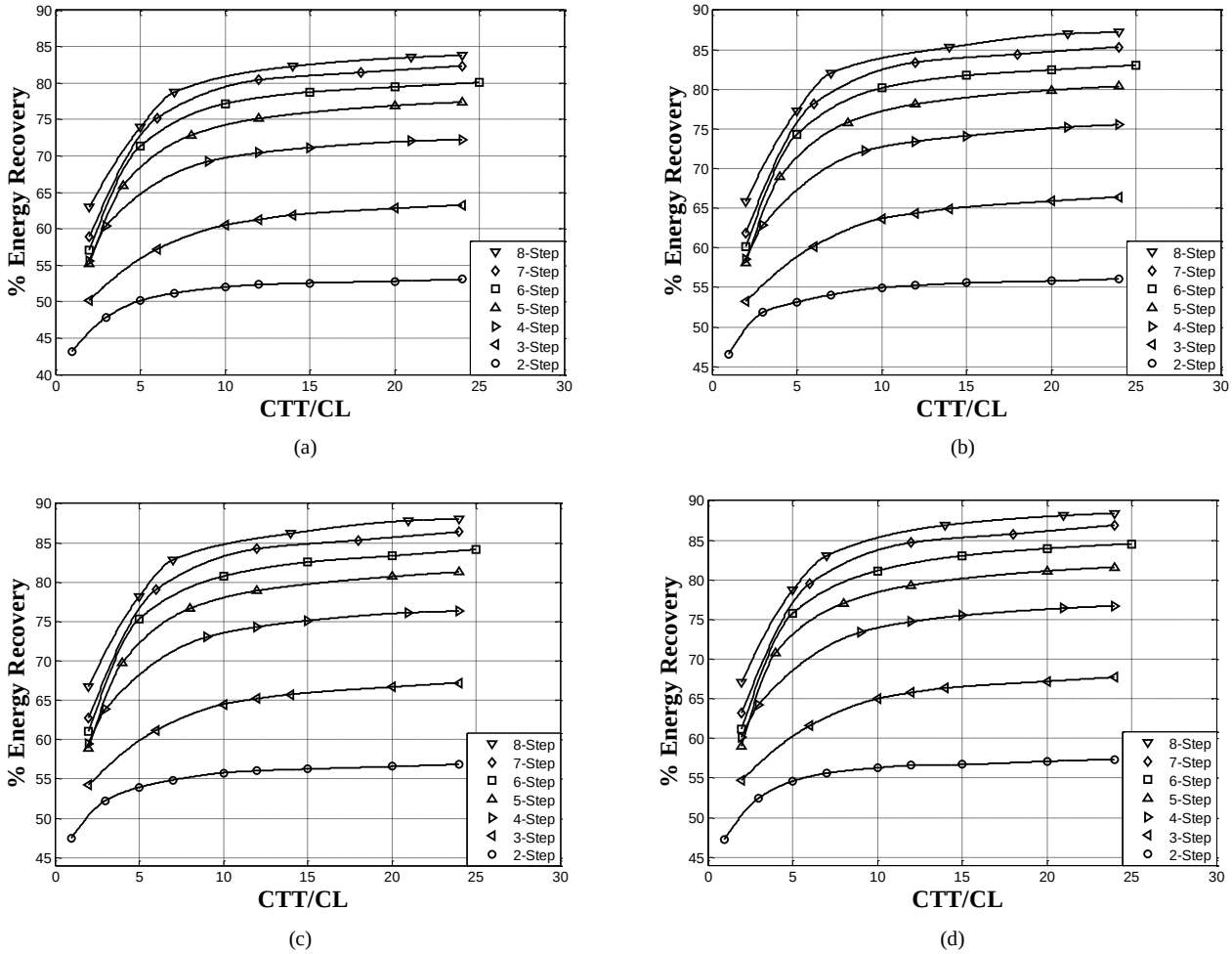

Fig. 4. Energy recovery vs CTT/CL ratio at ramping time (a) 50ns (b) 100ns (c) 200ns and (d) 400ns.

with a significant adiabatic core, will become a relatively insignificant factor in energy performance.

Because the results use "*total* tank-capacitance" C Total Tank (CTT) to load capacitor (CL) ratios, it can be seen that a larger number of steps with correspondingly smaller tank-capacitors deliver relatively better results in terms of energy recovery, compared to fewer, larger number of tank-capacitors in a small number of steps. For e.g. according to Fig. 4(a), (b), (c), (d) a 4-step charging circuit at CTT/CL ratio of 10(three tank-capacitors) gives better energy recovery compared to 2-step charging circuit with a CTT/CL ratio of 10 (one tank-capacitor). This illustrates, that the tradeoffs are best decided on CTT/CL ratios. Such a strategy has the advantage that the amount of silicon area dedicated to tank-capacitors can remain largely constant regardless of the number of steps.

Energy performance of adiabatic circuits is additionally a function of ramping time. Fig. 5 compares energy recovery achievable by 2, 3, 4, 5, 6, 7 and 8-step charging circuits at ramping times of 50ns, 100ns, 200ns and 400ns at a CTT/CL ratio of 10. Fig. 5 also shows that as the ramping time is increased above 100ns, the improvement in energy recovery is relatively small. But as the ramping time is reduced from 100ns to 50ns there is a decrement in energy recovery by approximately 3%.

Adiabatic losses dominate the energy dissipation at lower ramping times (higher speed) so energy recovery decreases.

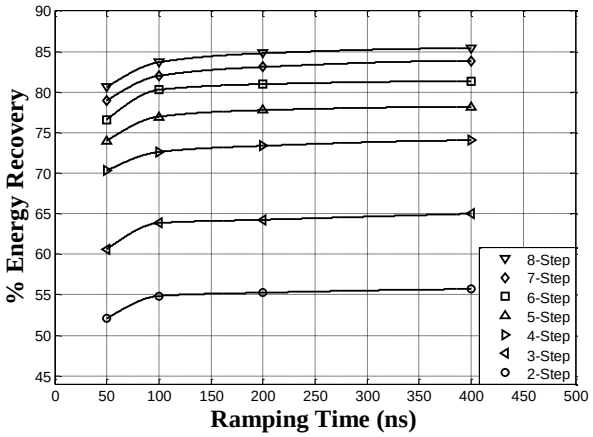

Fig. 5. Energy recovery vs Ramping time.

IV. Conclusion

In this paper, simulations of 2, 3, 4, 5, 6, 7 and 8-step charging circuits are presented. The relationship between total tank-capacitance to load capacitor (CTT/CL) that can give potential energy benefits was investigated for each implementation presented and a comparison was made on the account of circuit complexity and energy benefits. The simulation results show that tradeoffs can be made on the basis of total tank-capacitance to load capacitor (CTT/CL) ratios. Suitable tradeoffs have been suggested specifically that a CTT/CL ratio of 10 with a 4-step charging circuit are appropriate, and increasing either parameter yields relatively little benefit. Furthermore, the energy performance of adiabatic circuits improves at higher ramping time (slower speed).

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