On board Processor and Processing Strategies for Next Generation Reconfigurable Satellite Payloads

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***Abstract*—Today, the increasing demand in higher data rates necessitates new methods as well as higher flexibility for satellite telecommunication payloads in order to address a variety of applications and customers. This paper presents one of these processing strategies that is applicable to today's processing satellite payloads aiming to meet those demands. For this purpose, a two-tier filter bank is designed as part of a digital on-board processor, which first divides the spectrum at the output of the ADC into a number of sub-bands extracting all the stacked channels in the digital domain. Following the analysis section of the first tier of operations, the extracted channels go under a secondary channelisation process to obtain much finer granularity of 31.25 kHz or 50 kHz depending on the communication standard used for data transmission. The implementation of the channeliser was delivered on a bit-true simulation model and the input and the output of the channelisers were compared and evaluated both in the time and frequency domains.**

Keywords—Satellite Payload, On-Board Processing, DSP, IIR, FFT, FPGA

I. INTRODUCTION

Digital On-Board Processing (OBP) is becoming increasingly important in satellite communications to provide additional flexibility in frequency planning and routing. This has become the norm in the lower frequency bands typically used for mobile satellite communications, where the available spectrum is heavily congested. At L-band, for example, Thuraya and INMARSAT systems use narrowband digital beam-forming and channel routing to handle large numbers of beams with high frequency reuse to support much higher traffic capacities than conventional payloads. As the processing technology becomes more capable, the same features are also of increasing interest for high bandwidth communications at higher frequency bands. The Intelsat EPIC fleet of fully processed satellites currently in development to provide broadband capacity across commercial C-, Ku- and Ka- bands is the most notable example in this category.

Irrespective of the precise functionality required, flexible demultiplexing of the traffic bands into a large number of individually processed channels is a common requirement for all missions. It is the individual control of channel level processing combined with sufficient flexibility in the channel definition to support arbitrary frequency plans that allows OBP to realise efficient utilisation of limited satellite resources and ultimately maximises the useful satellite capacity. However, the channelisation function can be a major cost driver in terms of processing resources, which can be a significant drain on payload power budgets and a potential barrier to the more widespread use of large-scale digital processing for telecommunications satellites.

The channeliser presented here was designed considering narrowband communication scenarios such as Mobile Satellite Services (MSS), however it could also be used for broadband communications such as Broadcast Satellite Services (BSS) or Fixed Satellite Services (FSS). The system that is presented here is a generic model and the chosen parameters are examples. This paper is summarising one of the findings of the "REconfigurable FiLter-banks of Efficient Channelisation for Satellites" (REFLECS) project delivered by the authors under a European Space Agency (ESA) contract.

The paper is organised as follows. The second section briefly explains the N-element channel stacking scheme, which is used to increase the channeliser efficiency. The third section explains the overall channeliser two-tier in details. The bit-true simulation results are presented in section four. Finally, the concluding remarks are presented in chapter five.

II. N-ELEMENT CHANNEL STACKING SCHEME

One major technology constraint comes from the limited-availability of space-qualified Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC). The ADC often represents important limitation on achievable signal performance. One way to decrease this limitation is to stack a number of MSS channels by spacing them evenly across the available Nyquist zone. This scheme is presented in Fig. 1, where the ADC channel stacking is depicted and the corresponding stacked elements in the spectrum is shown in Fig. 2. The aim of channel stacking is to reduce the cost of on-board processing by reducing the number of processing chains required as well as by standardising space-grade components. The resulting signal presented to the ADC has a spectrum comprising a number of adjacent sub-bands, each representing the signal from a different antenna element, which must be further demultiplexed.

In this project, a number of signals are stacked together in the frequency spectrum prior to the processing of the signal in the digital domain as described above. The next section presents a solution to the demultiplexing of the stacked channels and to deliver a secondary channeliser to extract individual sub-channels for mobile users in this case. However, it should be noted that the channel stacking scheme is not specific to any particular mission.

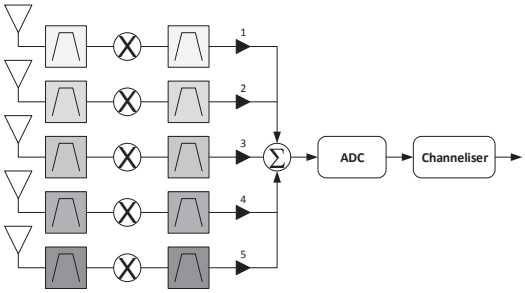

Fig. 1: Five-element ADC stacking example

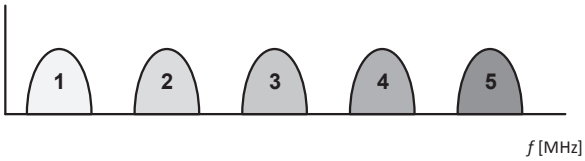

Fig. 2. Stacked five elements in the spectrum

III. SETUP AND DESIGN DETAIL

Our proposed two-tier design first divides the spectrum at the output of the ADC into nine sub-bands extracting all the stacked channels in the digital domain with a sampling frequency of 1280 MHz. The stacked elements from the ADC are all real-valued (not complex) and which means symmetry exists in the spectrum.

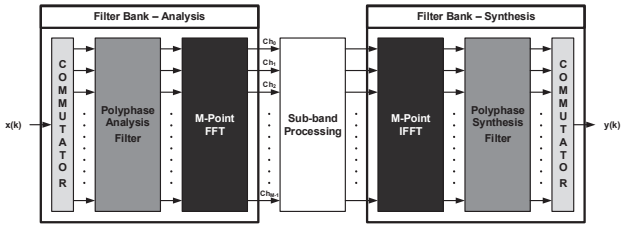

Fig. 3. Generalised FFT filter bank structure

Another decision was that the channeliser should support 50 MHz usable bandwidth per element with 10% guardband. The system should be also capable of channelising each of the 50 MHz channels into further 31.25 kHz or 50 kHz sub-channels. This means the design should be capable of demultiplexing and then multiplexing the spectrum up to 14400 individual sub-channels.

In the literature there are various channelisation methods such as the uniform DFT-based Filter Banks (FB) [1-3], non-uniform filter banks [4-6], Host Windowing [7-8] and Coefficient Decimation [9-10] methods. However, when the complexity and power budget are considered, none of these methods alone provide a solution to demultiplex the spectrum into such a high number of sub-channels. The most commonly used method in the literature is the DFT modulated filter banks for channelisation purposes, which is usually divided into three stages. The first stage is the analysis part, where the

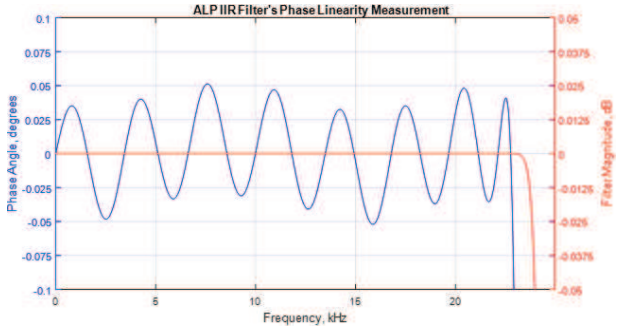

Fig. 5. ALP IIR filter's phase linearity deviation

incoming signal is separated into individual sub-channels as can be seen in Fig. 3. The filter is implemented in polyphase form and the input is distributed to each polyphase section of the filter via a commutator. Distributing the input samples to individual polyphase sections reduces the input sample rate by the number of channels, which also reduces the power dissipation of the rest of the processing chain. After the filtering process, the signal goes through a DFT block which separates the spectrum into individual channels. The DFT can be efficiently implemented by the Fast Fourier Transform (FFT) algorithm. The number of FFT points determines the number of channels the spectrum is to be divided into. Fig. 3 shows the generalised structure of an FFT FB.

Based on our two-tier channelisation method, the spectrum is first divided into nine channels using maximally decimated FFT FB, and after the stacked elements are retrieved in the digital domain, they are divided further either into 31.25 kHz granularity for GMR 1 or 50 kHz granularity for the GMR 2 standards in order to extract individual sub-channels for mobile users. The second-tier channeliser is a non-maximally decimated FFT FB. It is necessary to implement a synthesis part too in order to stack back both individual sub-channels (a collection of 31.25 kHz or 50 kHz channels) and the 50 MHz channels.

A bit-true simulation model, which is a precise model of the logic level implementation including loss of precision overflow, saturation and limiting is created to test the system performance. The system was created in the MATLAB/Simulink environment taking advantage of existing design tools and libraries, a high-level model of which is shown in Fig. 4. For the bit-true models, all the floating-point signals were converted into fixed-point for all the internal arithmetic and all the data paths within the computations quantised. The system shown in Fig. 4 takes the digitised real input data samples and first passes them through the first tier of the channeliser which is called the "Course Analysis" block and it contains the prototype filter and the FFT unit responsible for dividing spectrum into 64 MHz channels. The output is then fed into the "Channel Select" block which chooses nine non-empty channels. Then the data goes into second tier of operations

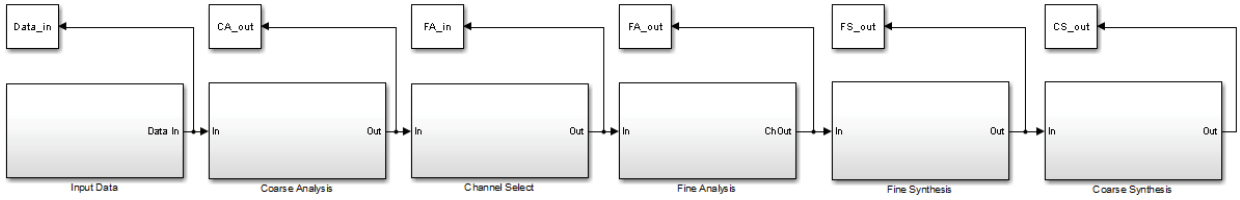

Fig. 4. Bit-true Simulink model of the end-to-end channeliser

called the "Fine Analysis" block to separate each 64 MHz channels into 31.25 kHz or 50 kHz sub-channels using the same method. The channelisation process is followed by the sub-band processing. In our case, the sub-band processing will be the alteration of the individual sub-channel locations along the frequency spectrum. After moving the individual channels to the required frequency slot, the signal is passed through the third and final part of the synthesis where the individual sub-channels are passed through Inverse DFT (implemented by IFFT) followed by the polyphase filters to combine the relocated individual sub-channels back together to deliver the output. As shown in Fig. 4, individual sub-channels are combined into nine 64 MHz channels in "Fine Synthesis" block and these 64 MHz channels are combined together at the "Course Synthesis" block to create the spectrum.

The channeliser is capable of multiplexing/demultiplexing a mixture of 31.25 kHz or 50 kHz channels as longs as the 50 MHz channels contain only one type. However, the stacked channels can be a mixture of either standards. The second-tier FFT FB can divide the available spectrum into either 2048 or 1280 sub-channels. It also supports half channel offset which is required for some type of telecommunication channels.

Prototype filters designed to have linear characteristics which preserve the signal's phase characteristics, and therefore for many communication systems digital filters are designed and deployed with linear phase in mind. The most common digital filter type that is used in communication systems is a Finite Impulse Response (FIR) filter which by their nature can be easily implemented with linear phase (flat group delay) characteristics. However, one major drawback of linear phase FIR filters is that they have high filter orders, which comes at a cost of increased computational complexity compared with minimum-phase Infinite Impulse Response (IIR) filters. An alternative could be to use Almost Linear Phase (ALP) IIR filters. ALP IIR filters are a class of polyphase IIR filters where the phase response is adjusted such that it becomes almost linear phase at the passband and nonlinear at the stopband regions [11-15].

Since the second tier channeliser is a non-maximally decimated FB, the analysis part of the design outputs the signal at an oversampled rate where the aliases exist in the spectrum. These aliases need to be removed before the sub-channels goes into further processing. This can be achieved by filtering the signal at the output of the analysis part of the second tier channeliser. A lowpass type of filtering operation with a narrow transition band is required for every sub-channel in order to remove the aliases due to oversampling. This means the filter order can be high which contributes to the computational complexity in a considerable amount. In order to minimise this extra computational burden an ALP IIR filter has been used. The phase linearity deviation of the deployed IIR filter is depicted in Fig. 5 and as can be seen from the figure it is approximately 0.1° which is well within the boundaries for our application. The frequency response of the ALP IIR filter is depicted in Fig. 6.

IV. SIMULATION RESULTS

The system functionality of the channeliser shown in Fig. 4 was tested and verified end-to-end using a computer-generated data stream and the input and the output of the channeliser was compared both in the time and frequency domains. In the time domain, the Mean Square Error (MSE) analysis was chosen as a comparison metric

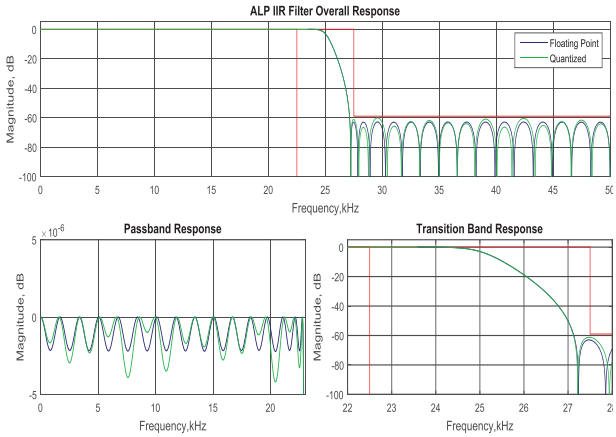

Fig. 6. Frequency response of the second stage filter

where the frequency spectrum was used to observe the amount of noise added to the received signal as it traversed through the channeliser processing stages as depicted in Fig. 5 and Fig. 6. For simulation purposes, randomly generated QAM/QPSK modulated data streams with 31.25/50 kHz bandwidth were stacked together in the frequency spectrum to emulate the ADC output, as explained in the previous section, and sent to the channeliser for further processing.

The top plot in Fig. 7 (input vs. Output) shows a portion of the input data and corresponding output data from the channeliser overlaid on top of each other. This is to demonstrate that we can successfully demultiplex and multiplex not only the stacked channels but also individual mobile channels of 31.25/50 kHz bandwidth. The bottom figure (MSE) shows the MSE error between the input and the output of the channeliser which is approximately 1.49×10^{-6}. On the other hand, Fig. 8 shows the spectrum of the input against the output. As can be seen from this figure, the frequency spectra of the input and output of the channeliser are matching and the end-to-end system is working with minimal noise floor increase which is due to filter bank aliasing. This is not avoidable, and the increase in the noise floor is because of the aliases introduced by the down samplers especially those in the analysis part of the system.

In the final analysis, we have made the following important observations; The increased complexity due to the introduction of reconfigurability and flexibility in communication processors can be reduced by replacing FIR filters with their ALP-IIR counterpart implementations without affecting the overall channelisation performance. In some cases, this resulted in improved metrics. It should also be noted that the filters were designed using conservative specifications and we are confident that the overall hardware complexity and power consumptions of our implementations can be modestly improved upon deployment of less stringent specifications.

V. CONCLUSIONS

In this paper, a bit-true end-to-end two-tier channeliser is introduced, which is capable of separating the available communication spectrum into either 31.25 kHz or 50 kHz sub-channels. Nine channels of up to 50 MHz each are stacked prior to the ADC to increase the efficiency of the channelisation process. The system is also compatible with data that have half channel offset and the offset can be selected individually for each channel to comply with relevant satellite

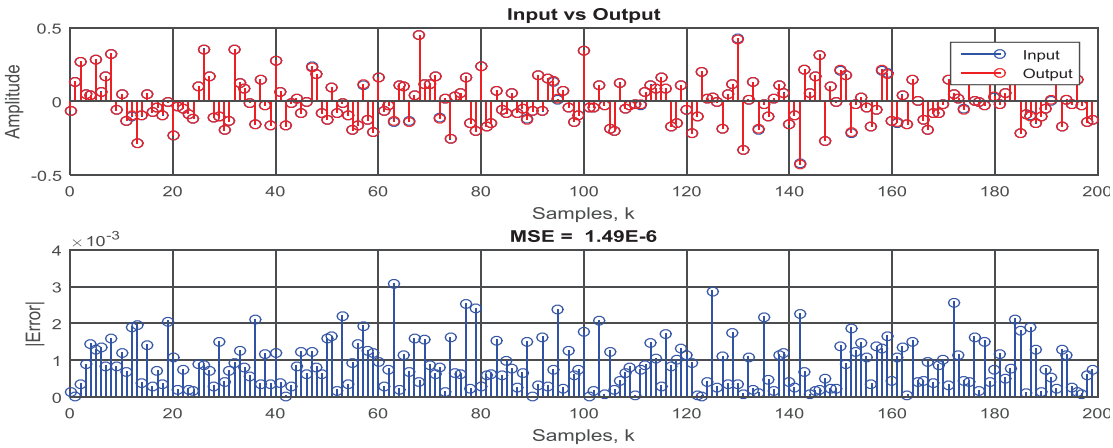

Fig. 7: End-to-End MSE performance of the bit-true channeliser system

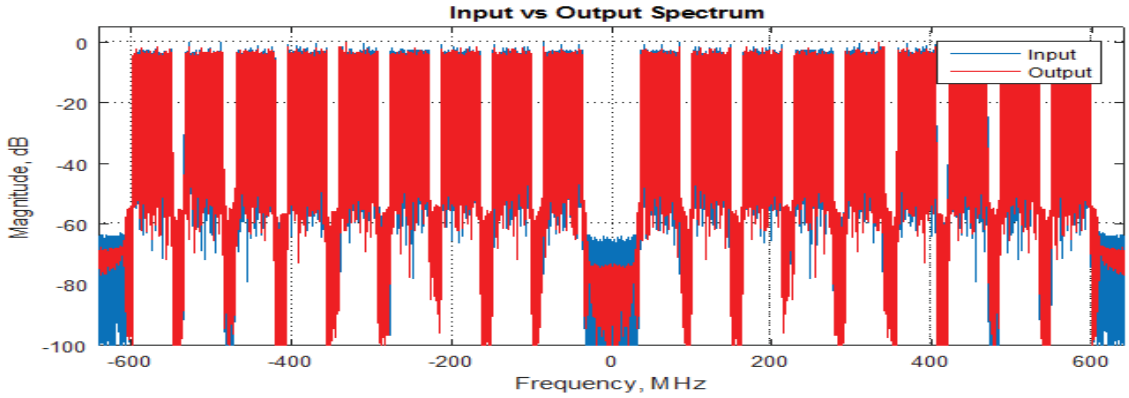

Fig. 8: Spectrum of the input vs output of the overall system

communication standards. Each of these nine channels can be configured independently. The first-tier of the channeliser demultiplexes the stacked channels and is a maximally decimated filter bank whereas the second-tier contains a non-maximally decimated filter bank. By using this method, it is possible to reduce the prototype filter complexity but in turn requires an extra stage of filtering for every one of the stacked channels. The increased hardware complexity can be reduced by employing an IIR filter with almost linear phase characteristics, designed carefully to meet the requirements set for phase linearity. The overall channeliser's performance is measured and validated using MSE analysis.

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