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Design and Simulation of a 3rd-order Discrete-Time Time-Interleaved Delta-Sigma Modulator with Shared Integrators between Two Paths

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***Abstract*, this paper presents the design and simulation of a 3rd-order two-path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator. By exploiting the concept of the time-interleaving techniques and time domain equations, a conventional 3rd-order Discrete-Time (DT) ΔΣ modulator is converted to a corresponding 3rd-order two-path DTTI counterpart. For the sake of saving power and silicon area, the integrators between the two paths of the DTTI ΔΣ modulator are shared. Using one set of integrators makes the DTTI ΔΣ modulator robust to path mismatch effects compared to the typical DTTI ΔΣ modulator which has individual integrators in all paths. A problem arises out of sharing integrators between paths which we call the delayless feedback problem. A solution for this problem is proposed in this paper and for an OverSampling Ratio (OSR) of 16 and a clock frequency of 320MHz, a maximum SNR of 76.5dB is obtained.**

***Keywords*: Discrete-Time, Time-Interleaved, ΔΣ modulator, Signal-to-Noise Ratio, OverSampling Ratio.**

I. INTRODUCTION

The ΔΣ modulators can achieve a very high resolution analog-to-digital conversion for low bandwidth applications by using oversampling and noise shaping techniques[1]. Recently, wideband applications require the ADCs with higher signal bandwidth. In order to increase the signal bandwidth of the modulator, a variety of methods can be used such as: using higher sampling frequency, increasing the order of the modulator and the number of quantizer bits.However, each of them has a price and is limited by technology [2].

One efficient appoach to increase the signal bandwidth is to use the time-interleaving technique [3] which increases the effective sampling frequency by paralleling more channels. This method is discussed in the next section.

II. TIME-INTERLEAVED (TI) ΔΣ MODULATORS

The well known procedure for the design of a ΔΣ modulator is based on choosing: the order and architecture of the ΔΣ modulator, the OSR and the number of bits for the quantizer. The time-interleaving technique can be successfully applied to ΔΣ modulators. However, the performance of the whole modulator is degraded due to channel mismatches. By paralleling M interconnected modulators that are working concurrently, the effective sampling rate and the OSR becomes M times the clock rate and the OSR of each modulator respectively [4],[5]. It should be noted that the required resolution can be obtained without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

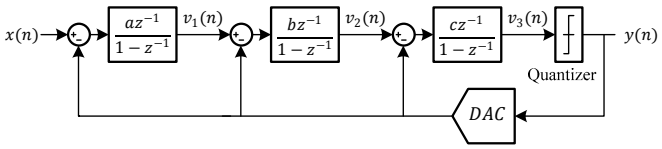

Figure 1: A 3rd-order conventional single-loop DT ΔΣ modulator.

A. DERIVATION OF THE TI ΔΣ MODULATOR

The 3rd-order DTTI ΔΣ modulator is derived directly from the time domain node equations of its conventional DT ΔΣ modulator as shown in Figure 1. It is assumed that the DAC in the feedback loop is ideal ($H_{DAC}(z) = 1$). The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th as follows [6]:

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (1.a)$$
$$v_2(2n) = bv_1(2n-1) - by(2n-1) + v_2(2n-1) \quad (1.b)$$
$$v_3(2n) = cv_2(2n-1) - cy(2n-1) + v_3(2n-1) \quad (1.c)$$
$$y(2n) = Q[v_3(2n)] \quad (1.d)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (2.a)$$
$$v_2(2n+1) = bv_1(2n) - by(2n) + v_2(2n) \quad (2.b)$$
$$v_3(2n+1) = cv_2(2n) - cy(2n) + v_3(2n) \quad (2.c)$$
$$y(2n+1) = Q[v_3(2n+1)] \quad (2.d)$$

where $Q[.]$ represents the quantization function. The input $x(n)$ is distributed between two channels through an input multiplexer which operates at twice the clock frequency of each channel. The input $x(n)$ is relabelled as follows:

$$x_1(n) = x(2n), \quad x_2(n) = x(2n-1) \quad (3)$$

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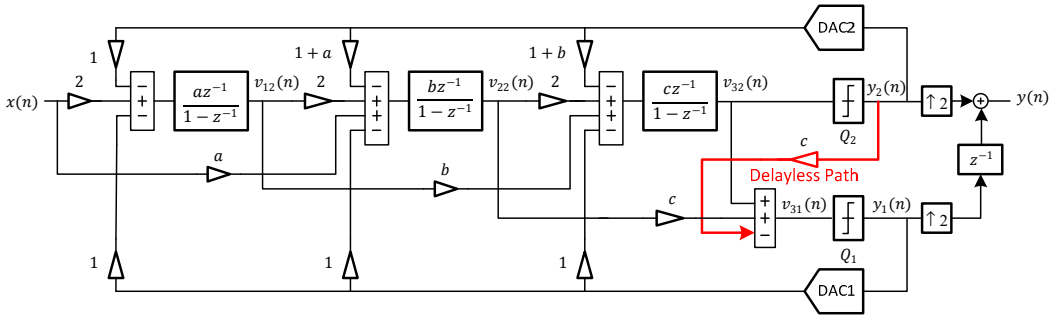

Figure 2: A 3rd-order DTTI ΔΣ modulator with shared integrators and delayless feedback path.

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n), \quad v_{12}(n) = v_1(2n-1) \tag{4.a}$$
$$v_{21}(n) = v_2(2n), \quad v_{22}(n) = v_2(2n-1) \tag{4.b}$$
$$v_{31}(n) = v_3(2n), \quad v_{32}(n) = v_3(2n-1) \tag{4.c}$$
$$y_1(n) = y(2n), \quad y_2(n) = y(2n-1) \tag{4.d}$$

By sharing only one set of integrators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Hence equation (3) results in (5) as follows:

$$x_1(n) = x_2(n) = x(n) \tag{5}$$

Equation sets (6) and (7) are derived by substituting equation set (4) and equation (5) into equation sets (1) and (2) respectively as follows:

$$v_{11}(n) = ax(n) - ay_2(n) + v_{12}(n) \tag{6.a}$$
$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \tag{6.b}$$
$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \tag{6.c}$$
$$y_1(n) = Q[v_{31}(n)] = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \tag{6.d}$$

and

$$v_{12}(n+1) = ax(n) - ay_1(n) + v_{11}(n) \tag{7.a}$$
$$v_{22}(n+1) = bv_{11}(n) - by_1(n) + v_{21}(n) \tag{7.b}$$
$$v_{32}(n+1) = cv_{21}(n) - cy_1(n) + v_{31}(n) \tag{7.c}$$
$$y_2(n+1) = Q[v_{32}(n+1)] \tag{7.d}$$

Equation set (7) can be rewritten as equation set (8):

$$v_{12}(n) = ax(n-1) - ay_1(n-1) + v_{11}(n-1) \tag{8.a}$$
$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \tag{8.b}$$
$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \tag{8.c}$$
$$y_2(n) = Q[v_{32}(n)] \tag{8.d}$$

Equation set (9) is derived by further substituting equation set (6) into equation set (8).

$$v_{12}(n) = 2ax(n-1) - ay_1(n-1) - ay_2(n-1) + v_{12}(n-1) \tag{9.a}$$
$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \tag{9.b}$$
$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \tag{9.c}$$

The 3rd-order DTTI ΔΣ modulator which is shown in Figure 2 is derived directly from the time domain equation set (6) and (9).

The motive behind sharing integrators is to eliminate the instability that can arise from the DC offset mismatch of the two individual integrator set based two channel interleaving case. The DTTI ΔΣ modulators need an input demultiplexer which samples the input signal at the highest clock frequency of the DTTI ΔΣ modulator and distributes it between channels. This fast demultiplexer is a limiting factor for the performance of the DTTI ΔΣ modulators. This architecture does not need an input demultiplexer and the input signal is shared between channels [3],[5]. Removing the input demultiplexer has no effect on the NTF of the DTTI ΔΣ modulator but it causes some notches in its Signal Transfer Function (STF) at the following frequencies $0.5F_{clk}$, $1.5F_{clk}$, $2.5F_{clk}$, $3.5F_{clk}$, … which is shown in Figure 5 where F_{clk} is the clock frequency of the DTTI ΔΣ modulator [5].

B. DELAYLESS FEEDBACK PATH PROBLEM IN TI ΔΣ MODULATORS

This is the issue that forms the focus of this paper which makes implementation of Time Interleaved (TI) ΔΣ modulators with shared integrators impractical and it is called the "*delayless feedback path problem*" that comes from equation (6.c) in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay [7]. One method to eliminate the delayless path is to move this feedback to the digital domain instead of performing it in the analog domain [5]. The disadvantage of this method is that the first quantizer (Q1) requires more comparators than the number of the comparators in the second quantizer (Q2) [7]. The second method is to use a sample-and-hold in front of the first quantizer (Q1) and quantizing the signal when the output of DAC2 is ready [3]. This method needs a complicated timing generator, a sample-and-hold and also faster integrators. The third method which is our proposed method is based on substituting $v_{32}(n)$ for $y_2(n)$ in equation (6.c). This method increases the quantization noise of the quantizer Q2 at the output $y(n)$. To better understand how this works we shall perform a step by step

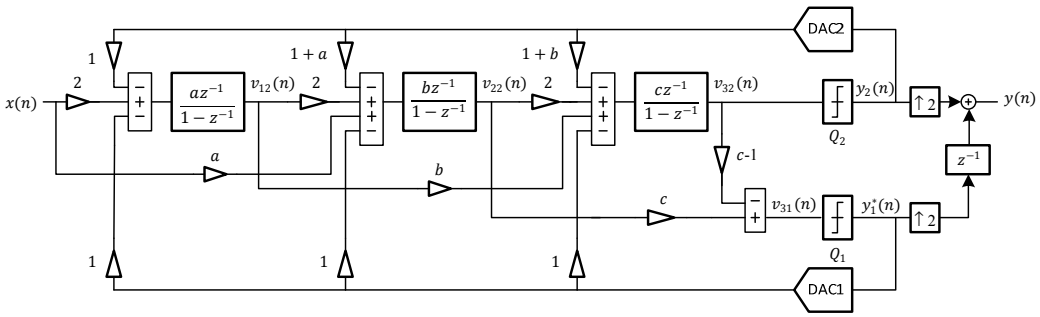

Figure 3: The proposed 3rd-order DTTI ΔΣ modulator with shared integrators and without delayless feedback path.

mathematical analysis of what happens. Quantizer Q1 and Q2 quantize the signal $v_{31}(n)$ and $v_{32}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] = v_{31}(n) + e_1(n) \quad (10)$$
$$y_2(n) = Q[v_{32}(n)] = v_{32}(n) + e_2(n) \quad (11)$$

Where $e_1(n)$ and $e_2(n)$ represent the quantization noise of the quantizer Q1 and Q2 respectively. Equation (12) is derived by substituting (6.c) into (10):

$$y_1(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) + e_1(n) \quad (12)$$

Equation (13) is given by substituting $v_{32}(n)$ for $y_2(n)$ into equation (12). The output of Q1 is called $y_1^*(n)$ in (13):

$$y_1^*(n) = cv_{22}(n) - (c-1)v_{32}(n) + e_1(n) \quad (13)$$

$y_1^*(n)$ approximates $y_1(n)$ in the DTTI ΔΣ modulator. The error which is induced by this method is presented by equation (14). This error does not cause instability in the modulator but increases quantization noise of quantizer Q2 at the output $y(n)$ followed by degrading the SNR of the modulator.

$$error = y_1^*(n) - y_1(n) = cy_2(n) - cv_{32}(n) = ce_2(n) \quad (14)$$

The resulting 3rd-order DTTI ΔΣ modulator is shown in Figure 3. The Signal Transfer Function (STF) and Noise Transfer Function (NTF) can be obtained by determining the loop filters of the modulator. In this design, the DTTI ΔΣ modulator has six loop filters ($FF_1(z), FF_2(z), H_1(z), H_2(z), H_3(z)$ and $H_4(z)$) and can be determined with the help of the symbolic toolbox of MATLAB. These loop filters for the DTTI ΔΣ modulator are as depicted in Figure 4. The STF and NTFs can be formulated by performing the following algebraic analysis:

$$Y(z) = Y_1^*(z^2)z^{-1} + Y_2(z^2) \quad (15)$$
$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \quad (16)$$
$$NTF_1(z) = \frac{H_3(z^2) + [1 - H_4(z^2)]z^{-1}}{[1 - H_1(z^2)][1 - H_4(z^2)] - H_2(z^2)H_3(z^2)} \quad (17)$$
$$NTF_2(z) = \frac{[1 - H_1(z^2)] + H_2(z^2)z^{-1}}{[1 - H_1(z^2)][1 - H_4(z^2)] - H_2(z^2)H_3(z^2)} \quad (18)$$
$$STF(z) = NTF_1(z)FF_1(z^2) + NTF_2(z)FF_2(z^2) \quad (19)$$

Where $STF(z), NTF_1(z)$ and $NTF_2(z)$ represent the signal transfer function from $x(n)$ to $y(n)$, the noise transfer function from $e_1(n)$ to $y(n)$ and the noise transfer function from $e_2(n)$ to $y(n)$ respectively. The z^2 terms show the effect of the up-samplers in the modulator.

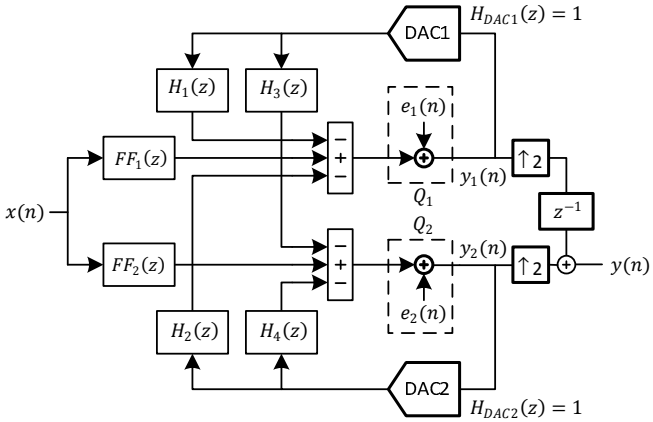

Figure 4: The block diagram of a DTTI ΔΣ modulator.

The conventional ΔΣ modulator is designed through the use of the delta-sigma toolbox from MATLAB to operate at 160MHz clock frequency and OSR of 16. The modulator coefficients are $\{a, b, c\} = \{0.333, 1, 3\}$. The STF and NTFs of the DTTI ΔΣ modulator are given by (20), (21) and (22).

$$STF(z) = z^{-3}(1 + z^{-1}) \quad (20)$$
$$NTF_1(z) = z^{-1}(1 - z^{-1})^3 \quad (21)$$
$$NTF_2(z) = (1 + z^{-1})(1 - z^{-1})^3 \quad (22)$$

Figure 5 compares the STFs of the DT and the DTTI ΔΣ modulator. STF of DT ΔΣ modulator is flat but STF of DTTI ΔΣ modulator has a notch at half sampling frequency resulting from $(1 + z^{-1})$ term in (20). Figure 6 shows the NTFs of the DT and the DTTI ΔΣ modulator. NTFs of the DTTI ΔΣ modulator shape the quantization noise more than the NTF of the DT ΔΣ modulator, however, $NTF_2(z)$ shapes noise less than $NTF_1(z)$ as a result of approximating $y_1(n)$ in (13).

III. SIMULATION RESULTS

The DT and the DTTI ΔΣ modulator have been simulated using the SIMULINK toolbox of MATLAB and all non-idealities such as finite dc gain, slew-rate and bandwidth of the opamps, the DAC mismatches and offsets of the quantizers have been modelled and their effects on the performance of the modulator have been investigated. The quantizers of the

DT and the DTTI ΔΣ modulator have 4bits of resolution in this design. The output spectra of the DT and the DTTI ΔΣ modulator for a 2.4462MHz input and clock frequencies of 160MHz and 320MHz respectively are plotted in Figure 7. The output spectra of the DTTI ΔΣ modulator is shaped more than the conventional DT ΔΣ modulator. The SNDRs of the conventional DT and the DTTI ΔΣ modulator are 64.5dB and 76.5dB respectively. Therefore in this particular case, the SNDRs of the DTTI ΔΣ modulators is improved by 11dB.

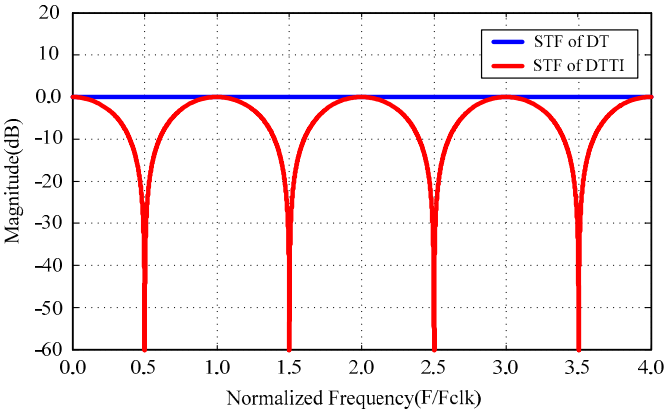

Figure 5: The STFs of the DT and the DTTI ΔΣ modulator.

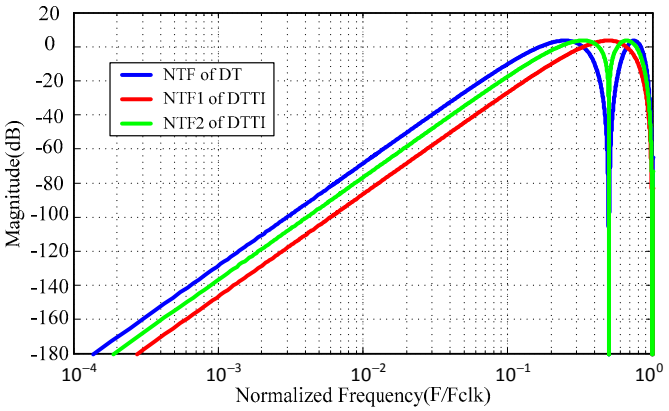

Figure 6: The NTFs of the DT and the DTTI ΔΣ modulator.

IV. CONCLUSION

In this paper a 3rd–order DTTI ΔΣ modulator with shared integrators between two-path and an OSR of 16 has been designed and simulated in the SIMULINK environment of MATLAB to operate at a sampling rate of 320MHz.. All practical non-idealities have been modelled and investigated. To resolve the delayless feedback path issue resulting from sharing integrators between paths, an approximation method has been proposed. The maximum SNDR obtained from the DTTI ΔΣ modulator is 76.5dB which shows an 11dB improvement in comparison with the standard single-loop single-path DT ΔΣ modulator.

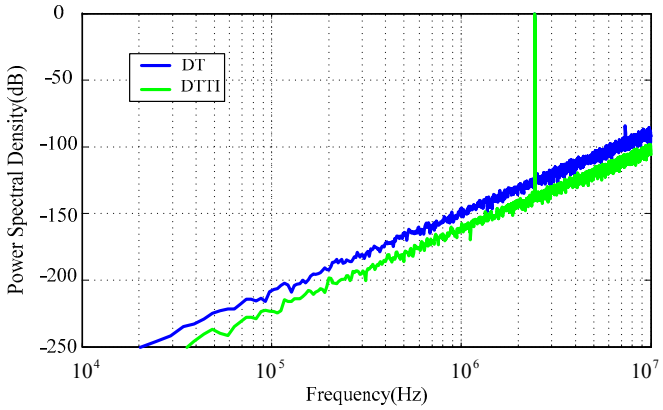

Figure 7: The output spectra of the DT and the DTTI ΔΣ modulator for a 2.4462MHz input with clock frequencies of 160MHz and 320MHz respectively.

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