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A Modeling Platform for Efficient Characterization of Phase-Locked Loop Δ–Σ Frequency Synthesizers

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***Abstract*—To dramatically reduce the need for Silicon reproduction due to poor noise performance, a close-loop simulation platform that combines both measured and/or simulation results of open-loop PLL sub-blocks has been developed. The platform is suited for Δ–Σ based fractional-N frequency synthesizers enabling integrated circuit designers to directly meet cost, performance and schedule milestones. Case studies employing the developed platform are provided for a fractional-N frequency synthesizer operating near 5 GHz. The effects of dead-zone, dithering, near-integer divisor operation, noise folding and prescaler usage on the overall phase noise performance of the entire frequency synthesizer are detailed.**

Index Terms—Fractional-N, Δ–Σ, Synthesizer, PLL, Charge Pump, PFD, VCO, Divider, Prescaler

I. INTRODUCTION

Fractional-N frequency synthesizers employ digital Δ–Σ modulators to modulate the main feedback divider to emulate a fractional divider enabling a high sampling frequency to be used. A high-sampling frequency aids the improvement of phase-noise performance within the PLL loop bandwidth close to carrier [1]. The output frequency is derived by multiplication of the sampling frequency and the fractional divider. The fractional divider is an average value of the instantaneous integer dividers obtained by the Δ–Σ modulator output. The Δ–Σ modulator used could be of cascade type or parallel type (MASH). The phase noise performance of the 3rd-order MASH modulator employed takes the shape of a high-pass power spectral density with very low suppression close to carrier [1]. This suppression improves the phase noise of the closed-loop fractional-N frequency synthesizer inside the loop bandwidth [1]. However, it has been demonstrated that non-linearity in the phase-frequency detector/charge pump combination causes noise folding to within the loop bandwidth worsening the phase-noise plateau rather than improving it. In fact, the frequency synthesizer is always measured in integer mode first and then measured in fractional mode. The fractional mode would yield the same phase noise performance when compared to the integer case if no noise folding exists. Mismatch between the up and down currents yields a discontinuity at the origin of the phase-frequency detector (PFD)/Charge Pump (CP) linearity curve that is considered as non-linearity. Extra offset up and down charge-pump currents at different proportions are normally added to alleviate this non-linearity effect and hence improve the phase noise performance inside the loop bandwidth. Outside the loop bandwidth, the loop filter is responsible for filtering out the Δ–Σ noise. The PFD/CP linearity is simulated, measured and incorporated in the simulation platform. The effect of the PFD/CP non-linearity has been shown to affect the phase noise performance. The developed platform is used for the characterization of some of the above-mentioned phenomena for the effective design of a 5 GHz frequency synthesizer. Details of the platform model implementation are discussed in the following section.

II. A Δ–Σ FREQUENCY SYNTHESIZER SIMULATION PLATFORM

Behavioral modeling for a fractional-N Δ–Σ based PLL has been carried out to check for performance limitations, identify dominant noise sources, automate loop filter optimization, and generate PFD/CP linearity specifications. A platform based on a phase domain model of the fractional synthesizer has been built using Cadence's Verilog-A language. A phase domain model suppresses the carrier, making time domain faster than voltage domain models in the Cadence environment [2,3]. The model includes the PFD/CP, the VCO, the reference, the divider, and the Δ–Σ modulator model. The simulation results obtained together with the measured results of the sub-blocks of the chip

contribute to the optimum design and implementation of fractional-N synthesizers.

A high-speed synthesizer design suitable for operation in the 5 GHz region was selected in this platform. Fig. 1 shows the basic platform system. The model employs data from simulated and measured results. Rather than simulating transient voltage, the model simulates the phases of the individual blocks [2, 3]. The voltage at the output of the reference signal represents the frequency used in the design (in this case 40 MHz, hence the reference is 40V). The PFD model gives a duty cycle output that can take values in the range of -1 to +1 [2]. When the duty cycle is negative there is discharge to the loop filter and when the duty cycle is positive there is a positive charge to the loop filter.

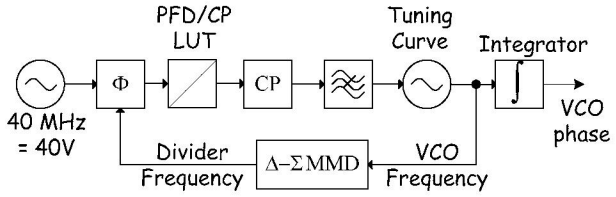

Figure 1: Phase domain model of the synthesizer

The PFD/CP linearity curve, whether taking into account the dead-zone or not, is provided by a look-up table immediately after the PFD. The PFD data could be easily stored in a file and loaded within the used block. The output of this look-up table is a voltage driving the subsequent charge pump that has normalized up and down currents yielding the desired charge pump values. The output of the charge pump current creates a voltage at the output of the loop filter that in turn drives the VCO. The VCO characteristic is a look-up table obtained by either simulating or measuring the gain of the VCO. The output of the VCO is a frequency which in fact is a voltage value in this proposed model. To obtain a phase value at the output of the VCO, it is mandatory to use an integrator as shown in Fig. 1.

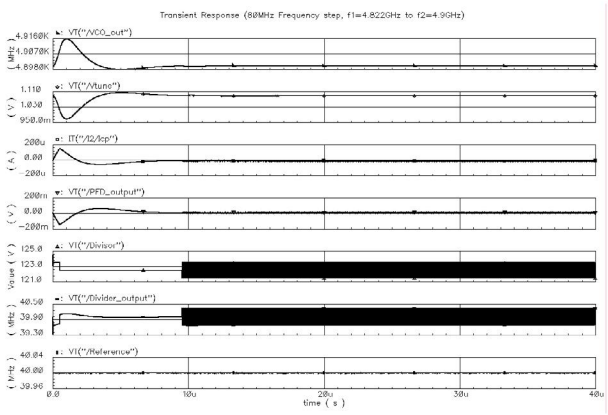

Figure 2: Time-Domain Phase-Model Node Voltages

The simulation in the proposed platform is carried-out in both the time-domain and frequency domains. The time domain simulation aids the monitoring of the settling in the phase-locked loop. Figure 2 shows the phase-domain model time-domain simulation illustrating the voltages at each individual node in the loop. The reference frequency of 40 MHz (represented here by 40V) is shown along with the feedback frequency (divider output) illustrating its average to 40 MHz (i.e. 40V) after 8μs. The PFD output is showing its convergence to 0 in 8μs (i.e. locking condition). The settling of the loop is best viewed by monitoring the tuning voltage that reaches its desired value as illustrated in the figure. The synthesized VCO frequency and its correspondent local oscillator frequency are both shown to reach their respective values within 8μs. It should be mentioned here that this simulation takes a couple of seconds as compared to a few days if transistor-level transient-simulations were used.

Open and closed-loop phase-noise can be characterized in the frequency domain. At this level, open-loop phase noise data must be included in the phase-domain model mentioned above. Each of the individual blocks except the loop filter employs a phase noise mask that has been simulated and measured. The VCO and PFD/CP phase noise have been simulated and measured and are incorporated in the phase-model discussed in this paper which can be enabled when loop phase-noise is needed.

Closed-loop phase noise of the synthesizer is then obtained by performing a power spectral density transform on the integrated VCO signal shown in Fig. 1. The divider and the Δ–Σ modulator are combined into one unique block. The block simply divides the voltage in fractional mode and contains the phase-noise mask of the delta-sigma modulator. The detailed closed-loop phase noise simulation and measurement is discussed in the following section. Also shown are the settled synthesizer phase-domain voltages for the case of no Δ–Σ dithering and 8-LSB Δ–Σ dithering as in Fig. 3 and Fig. 4, respectively. As can be seen in Fig. 3, the expected periodicity is occurring in the synthesizer feedback signal that results in a large spurious signal as will be shown in the next section. This periodicity disappears when 8-LSB dithering is applied to the Δ–Σ modulator as shown in Fig. 4. The 8-Bit LSB dithering causes enough excitation randomizing the spurious energy. This also will be seen in the frequency domain results in the following section.

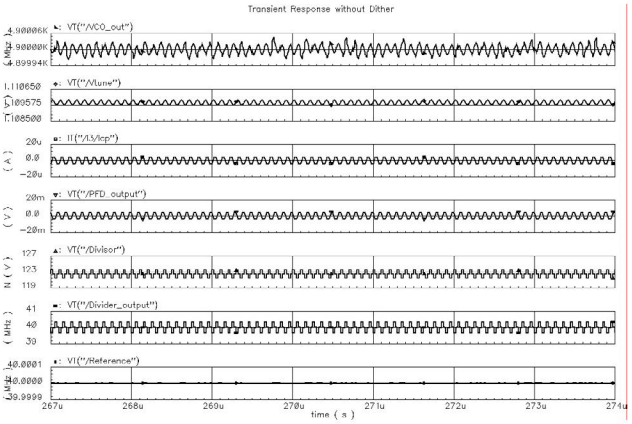

Figure 3: Settled PLL voltages with no Δ–Σ Dithering

III. PLATFORM EVALUATION

With the aid of the developed platform with fast simulation time, it is possible to optimize the filter components to yield optimum phase noise performance. Initial loop filter values were calculated using [4].

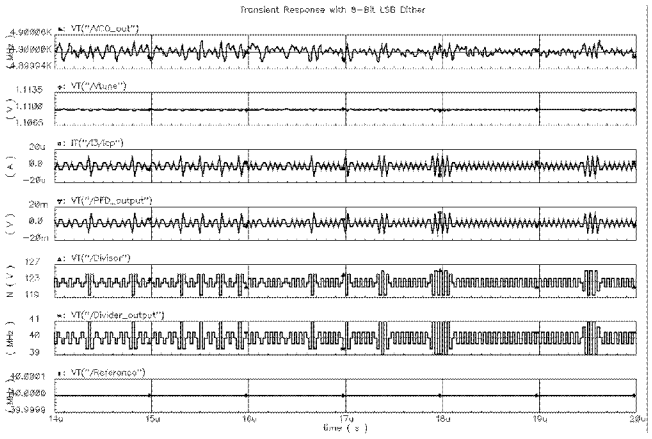

Figure 4: Settled PLL voltages (8-LSB Δ–Σ Dithering)

This section discusses the phase noise power spectral densities (PSD) of the synthesizer in different settings. The performance in the frequency domain (i.e. phase noise) can be easily obtained by performing power-spectral density transform on the time-domain phase-domain model results of the synthesizer in locked condition. Several phenomena can be studied using this platform; however, studies have been limited to three effects in this paper. These are: dead-zone effect, Δ–Σ dithering effect, and close-to-integer division effect.

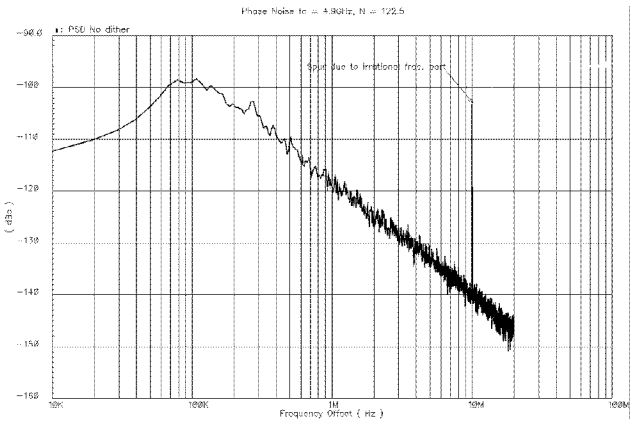

Figure 5: PLL Phase Noise with No Δ–Σ Dithering

The frequency domain phase noise of the PLL with no Δ–Σ dithering is shown in Fig 5. A presence of a fractional spurious signal can be observed at 10MHz for this case which employs an irrational fractional divisor part (0.5). The low-frequency effect below 25 kHz is a deficiency in the power-spectral density function built in Cadence. If low-frequency phase noise is of interest, it is advisable to export the data to a mathematical package for further accurate processing. Other effects that have been monitored using the developed platform are as discussed below:

A. Dithering Effect

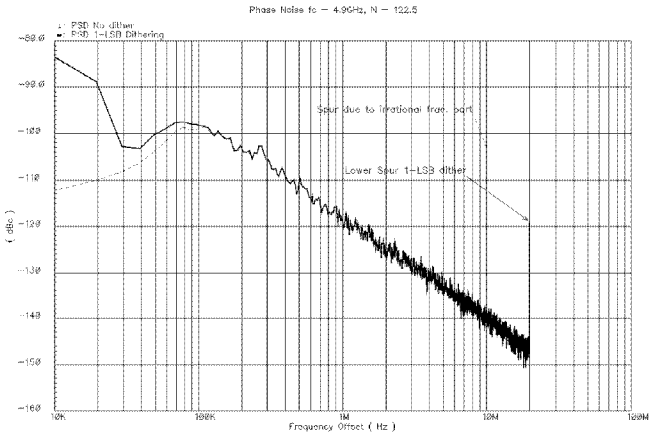

Figure 6: PLL Phase Noise with 1-LSB Δ–Σ Dithering superimposed on that of Figure 5.

Figure 6 shows the phase noise profile for the frequency synthesizer employing a 1-LSB dithering applied to the digital Δ–Σ modulator. Two cases are superimposed. The first case is when no dithering is employed which shows the presence of spurious fractional contents whereas the top part is the case where dithering is applied. In this case, the spurious energy is spread across the spectrum and hence the lifting of the phase noise as illustrated in Fig 6. The 10MHz spurious signal has disappeared, however another low-amplitude spurious signal 20MHz came to existence. Further dithering could be applied if total spurious cancellation is required. This is illustrated in Fig. 7 for the case with 8-LSB dithering. Here it can be seen that there are no spurious signals present but as expected the phase noise level has worsened. This effect must be taken into account when designing synthesizers to strike a compromise between deterministic spurious noise and random phase noise.

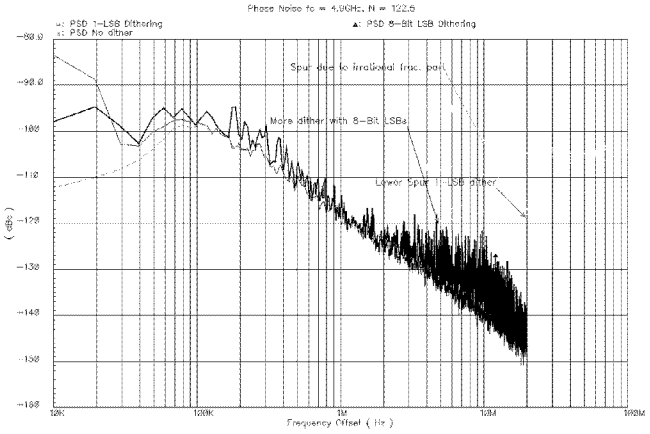

Figure 7: PLL Phase Noise with 8-LSB Δ–Σ Dithering superimposed on those of Figures 5 and 6.

B. *Close-To-Integer Operation*

When close-to-integer feedback divider is used, the spurious signals are harder to noise shape as can be seen in Fig. 8 where no dithering has been applied. Fig. 9 shows the synthesizer phase noise with 10-LSB dithering applied to the Δ–Σ modulator and a close-to-integer division ratio used. There is a total cancellation of the spurious content, however at the expense of deterioration in the phase noise level as illustrated in Fig.9 superimposing the case where 1-LSB dithering has been employed.

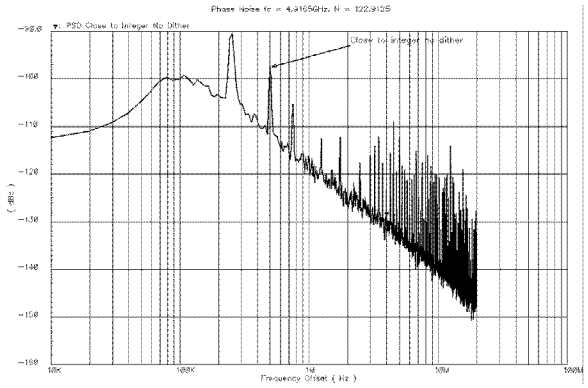

Figure 8: PLL Phase Noise with Close-To-Integer Feedback Division

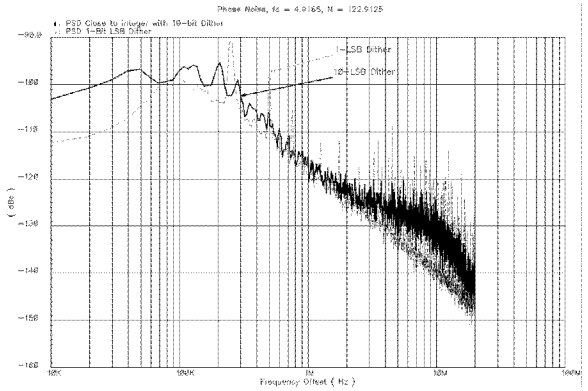

Figure 9: PLL Phase Noise with Close-to-integer Feedback Division and 10-LSB Δ–Σ Dithering superimposed on that of 1-LSB Δ–Σ Dithering

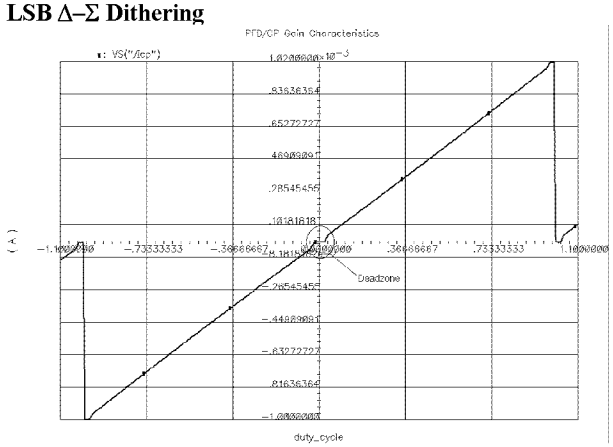

Figure 10: PFD/CP Gain Characteristics illustrating Dead-zone Band.

C. *Dead-Zone Effect*

The dead-zone effect is obtained due to the non-linear effect of the PFD/charge pump in the synthesizer as shown in Fig.10. This manifests itself in the phase noise deterioration as shown in Fig. 10. A 10 dB worse in phase noise is yielded when dead-zone exists as compared to the case when 10-LSB dithering applied to the Δ–Σ modulator shown in Fig. 9 and superimposed on Fig. 11.

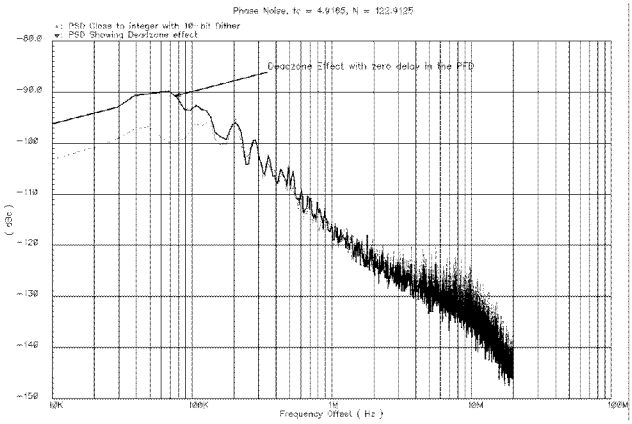

Figure 11: PLL Phase Noise with Close-to-integer Feedback Division and 10-LSB Δ–Σ Dithering superimposed on that with Dead-Zone

IV. CONCLUSION

We have presented a platform for the efficient characterization of a Δ–Σ Frequency synthesizers. The platform employs a phase-domain model of each individual sub-block in the synthesizer. Different effects have been monitored by evaluating the platform testing a 5 GHz frequency synthesizer. Many synthesizer effects can be monitored using the developed platform but for brevity, phenomena such as dithering, close-to-integer division, and dead-zone have been tested and presented in this paper. The platform offers circuit designers a superb tool for chip verification in a short period of time.

ACKNOWLEDGMENT

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