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VHDL-based Modelling Approach for the Digital Simulation of 4-phase Adiabatic Logic Design

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***Abstract*— In comparison to conventional CMOS (non-adiabatic logic), the verification of the functionality and the low energy traits of adiabatic logic techniques are generally performed using transient simulations at the transistor level. However, as the size and complexity of the adiabatic system increases, the amount of time required to design and simulate also increases. Moreover, due to the complexity of synchronizing the power-clock phases, debugging of errors becomes difficult too thus, increasing the overall verification time. This paper proposes a VHSIC Hardware Descriptive Language (VHDL) based modelling approach for developing models representing the 4-phase adiabatic logic designs. Using the proposed approach, the functional errors can be detected and corrected at an early design stage so that when designing adiabatic circuits at the transistor level, the circuit performs correctly and the time for debugging the errors can substantially be reduced. The function defining the four periods of the trapezoidal AC power-clock is defined in a package which is followed by designing a library containing the behavioral VHDL models of adiabatic logic gates namely; AND/NAND, OR/NOR and XOR/XNOR. Finally, the model library is used to develop and verify the structural VHDL representation of the 4-phase 2-bit ring-counter and 3-bit up-down counter, as a design example that demonstrates the practicality of the proposed approach.**

Keywords*— adiabatic logic technique, power-clock, VHDL modelling, synchronization, verification

I. INTRODUCTION

The use of adiabatic logic technique instead of the non-adiabatic logic design can considerably decrease the energy consumption in a large system [1]-[4], [8]-[11], [15]-[22]. Though it is in existence for more than two decades, still, its full potential has not been explored. However, various research papers demonstrated the energy saving potential of the adiabatic logic technique compared to the non-adiabatic logic. In [2], it has been shown that at lower technology nodes adiabatic logic has better energy performance than non-adiabatic logic. Similarly, in [3] the behavior of adiabatic logic circuits in weak inversion or subthreshold regime is analyzed. Through extensive post-layout simulation, it demonstrated that subthreshold adiabatic circuits can save significant energy compared with an equivalent non-adiabatic implementation. Moreover, the recent work of adiabatic principle applicability to adiabatic capacitive logic demonstrate the effectiveness of the technique to achieve zero-power logic dissipation [4]. Nevertheless, the functional verification of the adiabatic design at the transistors level is time-consuming and difficult. The design of adiabatic circuits requires much more efforts in contrast to the non-adiabatic logic for which well-developed tools exist. The major difference between the two is that the adiabatic logic designs use slowly changing AC power-clock supply instead of DC (constant) power-supply.

VHDL is valid and is efficiently used for signal levels ‘0’ and ‘1’ having zero rise and fall times for ideal simulations. However, in adiabatic logic, waveforms are more complex because of the multi-phase clocking and the dual-rail encoding of inputs and outputs. Thus, in addition to logic ‘1’ and logic ‘0’, the adiabatic power-clock supply uses two more logic levels where the power-clock transition is a ramp such that all the four levels share the same period.

Based on the literature review, the first modelling in VHDL of adiabatic logic was done by M. Vollmer and J. Gotze in 2005. They described the adiabatic logic in VHDL for a systolic array with precise timing and bit-true calculation [5]. Their work included the description of logic blocks that required 4-phase clocking scheme but did not model the dual-rail encoding and use one global clock net instead of 4-phase power-clock for cascade designs. A year later, Laszlo Varga et.al, described two-level pipelining scheduling of adiabatic logic using integer linear programming formulation and a heuristic scheduling [6]. The authors presented the VHDL description for functional simulation of the synthesized adiabatic datapath together with the non-adiabatic part of the digital system. This approach focusses mainly on producing a pipeline schedule of the power-clock behaviour of the adiabatic logic but did not model the power-clock and the dual-rail behaviour of the adiabatic logic. In 2010, David John Willingham in his PhD thesis [7] reported Asynchrobatic Logic in Verilog, an industry standard Hardware Description Language (HDL). First, the author demonstrated the idea in a single-rail scheme and then extended it to dual-rail, which was found to be missing in Vollmer and Laszlo’s modelling. The dual-rail implementation proves to be advantageous in detecting an invalid circuit operation to some extent. The author defined three states namely; valid state (logic ‘1’ or logic ‘0’), invalid state and inactive state. This approach also did not model the power-clock in HDL, instead, it used square waves for generating the 4-phase power-clock. Though all were able to demonstrate the pipeline timing, none followed the adiabatic principles, that is, the circuit generates a valid output signal when the input and the power-clock are both in the same phase. Moreover, the square-wave used as a power-clock combines the evaluation and hold period of the

trapezoidal AC power-clock as logic '1', whereas, the recovery and idle period is represented as logic '0.

Therefore, in this paper, HDL-based modelling approach for the 4-phase adiabatic logic technique is developed for functional simulation. It represents the 4-phase power-clocking scheme and includes a systematic approach for precise timing analysis. The proposed approach captures the exact timing errors and detects the circuit's invalid input operations by checking the generated complementary outputs. The modelling includes the dual-rail representation of the input/output signals.

The paper is structured as follows; Section II describes the adiabatic logic technique and a method of encoding trapezoidal waveforms in HDL. The functional simulation of the PFAL buffer circuit using the modelling approach and SPICE simulation results are presented in section III. Section IV shows how the precise timing of the proposed VHDL modelling is captured. The comparison and validation of the proposed VHDL modelling with SPICE simulation results based on the case study of a 2-bit ring-counter and a 3-bit up-down counter is presented in section V. The paper is concluded in section VI, followed by the future work in section VII.

II. Adiabatic Logic Technique and Encoding of Trapezoidal Waveforms

The adiabatic logic technique is one of the innovative solutions at logic and circuit level to achieve a reduction in energy dissipation for devices working at less than 100MHz frequency [8]. The adiabatic circuits would operate ideally with zero dissipation that may be approached as the logic switching is slowed down. A decreased energy dissipation with increased switching time is, therefore, the defining property of an adiabatic switching [9]-[11]. The use of a slowly changing power-clock which allows approximately constant current charging/discharging helps in avoiding the current surges and therefore, the circuit dissipates less energy [9]. In addition, this slowly charging process gives an additional advantage of pumping the stored energy back to the power supply during the discharging process which can be recovered using an AC power-clock generator [12]-[15]. The detailed derivation of (1) is given in [10].

$$E_D = (RC_L/T_r)\, C_L V_{DD}^2 \qquad (1)$$

Where E_D is the energy dissipation, T_r is the ramping time, C_L is the effective output load capacitance, R is the charging path resistance and V_{DD} is the supply voltage. It should be noted that the above equation doesn't take into account the energy loss due to leakage and threshold voltage degradation (non-adiabatic loss)

Fig. 1 shows the input and the 4-phase power-clock with each phase having 90° of phase difference with each other. The 4-phase power-clocks are broken down into four equal time periods namely evaluation (E), hold (H), recovery (R) and idle (I). To have less energy dissipation, all the nodes in a circuit should share the same principle of charging and discharging. For example, in cascade logic, during the evaluation period of the power-clock (PC1), the input which is being sampled must be stable for the stage to produce a valid output in the hold period. The second stage will be sampling its input while the output of the first stage is stable (hold period) and so on. This behavior forms a pipeline, processing one input and one output at every power-clock phase.

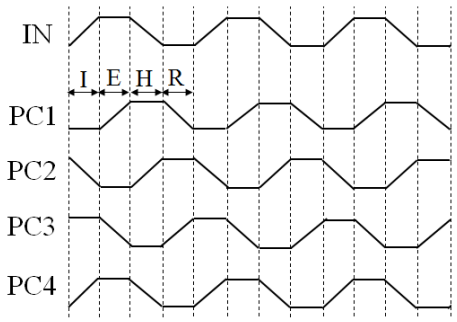


Fig. 1. 4-phase power-clocking scheme.

Recent work on the performance comparison of the adiabatic logic families working in single-phase, 2-phase and 4-phase power-clocking scheme [16], [17] and the power-clock generator [12]-[14] has contributed and distant a myth on the adiabatic logic capability of providing an energy efficient alternative to non-adiabatic logic. Based on the comparison results, the 4-phase adiabatic system is the most promising in terms of performance and energy requirement compared to single and 2-phase power-clocking adiabatic logic scheme [17]. The 4-phase adiabatic logic is implicitly pipelined and glitch-free. This suggests that there is no concern about the critical paths. However, in a large adiabatic system using a 4-phase power-clocking scheme, the debugging of errors are time-consuming due to the complexity of synchronizing the power-clock phases. The difficulty of modelling the adiabatic logic accurately arises due to the trapezoidal shape of the AC power-clock. Thus, to model the adiabatic behavior using HDL, the first task is to conceptualize the trapezoidal AC power-clock behavior using HDL. Then writing the behavioral code of the basic logic gates for functional and timing verification.

The multi-level event-based approach is proposed for modelling the four equal time-periods of a trapezoidal AC power-clock. In this method, the hold and idle periods of the power-clock are represented as logic '1' and logic '0' respectively. Whereas, the evaluation and the recovery period are encoded with an intermediate state marked as 'X', as both share the same duration of the ramp period. This approach is not straightforward, as apart from generating the power-clock which has three logic levels, the adiabatic inputs must also be generated with three logic levels for proper functionality and timing analysis. The trapezoidal AC power-clock is modelled using three logic levels as shown in Fig. 2.

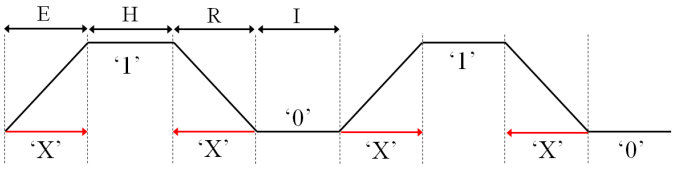


Fig. 2. Encoding trapezoidal AC power-clock in HDL.

The four periods of the power-clock are defined in a package as a function, which is used to develop the cell library of the basic adiabatic logic gates. To realize the adiabatic power-clock in standard logic, four states are required. Each state is encoded based on the logic levels requires. The four states can be easily generated using two flip-flops. Fig. 3 shows the VHDL simulation for generating the adiabatic power-clock signal. The approach can also be easily used for single-phase and 2-phase adiabatic logic techniques, although it will not be straightforward in the case of 2-phase adiabatic logic due to its long idle period [17].

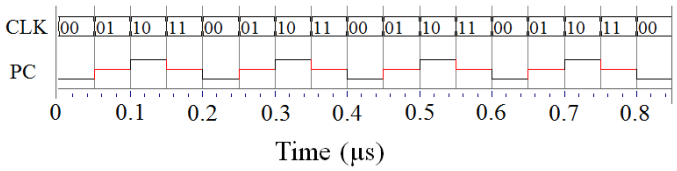
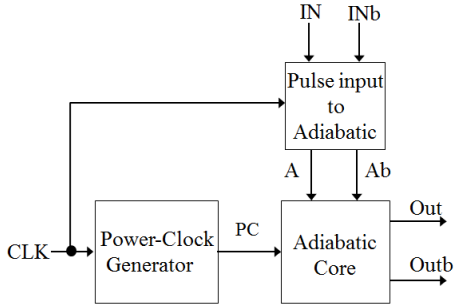


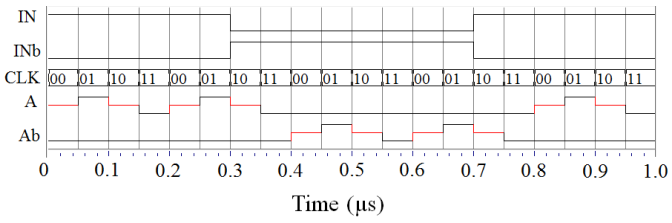
Fig. 3. VHDL simulation for generating a power-clock signal.

III. Functional Simulation of Adiabatic Logic Circuits

The VHDL model for the NOT/BUF adiabatic gate is collectively done using the power-clock generator, pulse input to adiabatic input (multi-level) conversion and the package defining the four periods of the power-clock. The conceptual block diagram for an adiabatic NOT/BUF gate using the proposed modelling approach is shown in Fig. 4 (a). The pulse input to adiabatic conversion block also requires four states and depending on the input pulse (IN, INb) having logic levels '0' or '1', the complementary adiabatic signals (A, Ab) are generated. Fig. 4(b) shows the generation of multi-level adiabatic complementary signals from pulse input. The adiabatic core is a PFAL NOT/BUF gate [18] generating the complementary outputs (Out, Outb). A fragment of the VHDL description of the NOT/BUF adiabatic gate is shown in Fig. 5.



(a)



(b)

Fig. 4. (a) A conceptual block diagram of an adiabatic NOT/BUF gate (b) Conversion of the pulse input to adiabatic multi-level input.

```
Process (PC, A, Ab) is
  Begin
                        // Idle Period
    if PC='0'  then
        Out <= PC;
        Outb<= PC;
    elsif  PC='0'  and  EVALUATE_edge  (A)  and
      EVALUATE_edge(Ab) then      // invalid state
        Out<= 'Z';
        Outb<='Z';
                        // Evaluation Period

    elsif PC='X' and HOLD_edge (A) and HOLD_edge (Ab) then
        Out<= 'Z';                  // invalid state
        Outb<='Z';
    elsif PC='X' and HOLD_edge (A) then
         Out <= PC;
         Outb<='0';
    elsif PC='X' and HOLD_edge (Ab) then
         Out <= '0';
         Outb<=PC;
                        // Hold Period

    elsif  PC='1'and  RECOVERY_edge  (A)  and
        RECOVERY_edge (Ab) then  // invalid state
        Out <= 'Z';
        Outb<='Z';
    elsif PC='1' and RECOVERY_edge (A) then
        Out <= PC;
        Outb<='0';
    elsif PC='1' and RECOVERY_edge (Ab) then
        Out <= '0';
        Outb<=PC;
                        // Recovery Period

    elsif PC='X' and IDLE_edge (A) and IDLE_edge (Ab) then
        Out <= 'Z';                 // invalid state
        Outb<= 'Z';
    elsif PC='X' and IDLE_edge (A) then
        Out <= PC;
        Outb<='0';
    elsif PC='X' and IDLE_edge (Ab) then
        Out <= '0';
        Outb<=PC;

    End if;
  End Process;
End Behavioral;
```

Fig. 5. VHDL description of the NOT/BUF adiabatic gate.

The behavior of the adiabatic NOT/BUF gate encoded using VHDL is shown in the Fig. 6 (a). Similar to the transistor level design, the output follows the power-clock based on the input being processed. The proposed method produces same behavior to that of the SPICE simulation. The four power-clock periods are defined in a package which is used in all the adiabatic VHDL description files by placing the 'USE' directive in the VHDL program. The output waveforms using the proposed VHDL based modelling and the SPICE simulation are shown in Fig. 6 (a) and (b) respectively. VHDL simulation shows the precise timing as depicted in the SPICE simulation. Moreover, the proposed modelling has an additional advantage of detecting an invalid input which spice

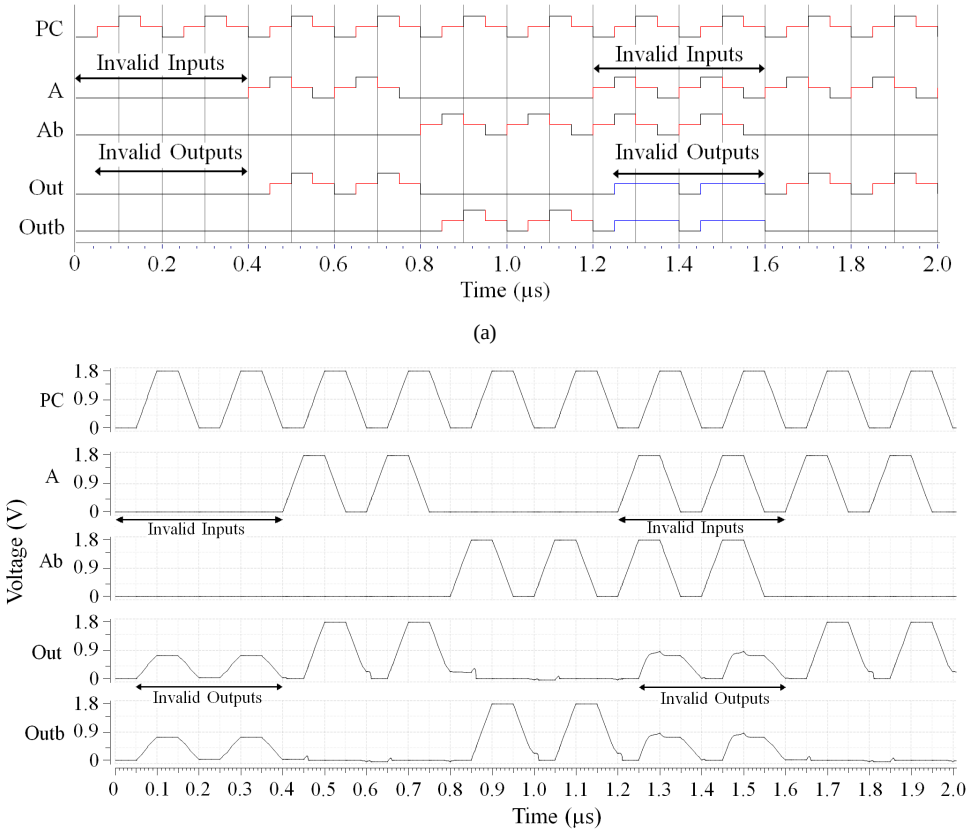


Fig. 6. Simulation results for NOT/BUF gate (a) VHDL Model (b) SPICE

simulations and the previously defined modelling [9] fail to identify. The more detailed analysis of accurately modelling an invalid state is given in the next section

IV. PRECISE TIMING MODELLING

To model precise timing in VHDL, the invalid conditions must also be modelled as accurately as possible. The operation of an adiabatic gate, although conceptually simple, can be somewhat complex to model accurately. This is due to the two cross-coupled inverters forming a latch, which retains the last value stored on the complementary output nodes [19]. For example: if the complementary inputs (A, Ab) are at logic '0' (invalid states), the outputs will retain the last value stored on it. This suggests that if the last value on the two output nodes (Out and Outb) is logic '1' and logic '0' respectively then the same value will be retained. This invalid condition is depicted in the Fig. 7. This, invalid input operation in a large circuit will be difficult to debug, specifically in the case when functionally, the logic value '1'and '0' is expected on the two output nodes. In addition, this invalid circuit operation will lead to high energy consumption, due to the non-adiabatic loss (NAL) [19]. This can be seen in the Fig. 7 when the complementary inputs are at logic '0', the two output doesn't discharge to ground. On the other hand, if the complementary inputs are at logic '1', then the complementary output nodes will be charged through the pMOS transistor (which follows the power-clock) and at the same instant the nMOS transistor will be discharging the output nodes to ground and thus, the two nodes will settle at some intermediate value. This invalid condition is depicted in Fig. 6(b) and Fig. 7.

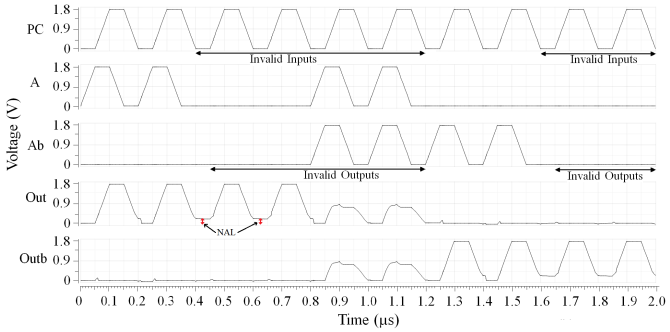


Fig. 7. SPICE simulation results for PFAL NOT/BUF gate with invalid outputs

The proposed HDL model can easily identify the errors caused by the complementary inputs when both are at logic '0', which the SPICE simulation fails to identify. In this case, the circuit remains inactive, that is, the complementary output voltages remain at logic '0', detecting an invalid input condition. Similarly, when the complementary inputs are at logic '1', the complementary output nodes remain at high impedance state encoded by 'Z'. The above invalid operations

are shown in Fig. 6(a). Thus, two different states, '0' and 'Z' are used when the complementary inputs are driven to the same logic values (invalid conditions). This helps in identifying the value of the invalid inputs clearly.

V. Simulation Results

The 4-phase adiabatic logic family used for the SPICE simulation is PFAL. The transistor sizes are set to the technology minimum ($W_{min}=W_n=W_p=220$nm, $L_{min}=L_n=L_p=180$nm). The SPICE simulations were performed with Spectre simulator using Cadence EDA tool in a 'typical-typical', TT process corner using TSMC 180nm CMOS process at 1.8V power supply.

For all the other adiabatic logic gates such as AND/NAND, OR/NOR, XOR/XNOR and MUX/DeMUX the VHDL behavior is described by combining the functional part and the adiabatic NOT/BUF for timing validation. The collection of all the logic gates described in VHDL formed the cell library.

Using the homegrown cell library, the structural models of a 2-bit ring counter and a 3-bit up-down counter were successfully verified. The circuit functionality and timing verification were done using HDL Designer from Mentor Graphic. The time period of the power-clock was taken as 100ns, having equal time for the four periods of the power-clock i.e. 25ns each. The simulation setup for VHDL is similar to that of SPICE so that uniformity and comparability are maintained across both the simulations.

Since the twisted ring counter is able to self-initialize from an all-zeros state and does not have any external inputs, it is an ideal vehicle for comparing the VHDL implementation with the SPICE simulation. The 2-bit adiabatic twisted ring counter consisting of two D flip-flops. The complete design of the 4-phase 2-bit ring counter is given in [16]. The reset input is given as a step signal, not converted to multi-level adiabatic

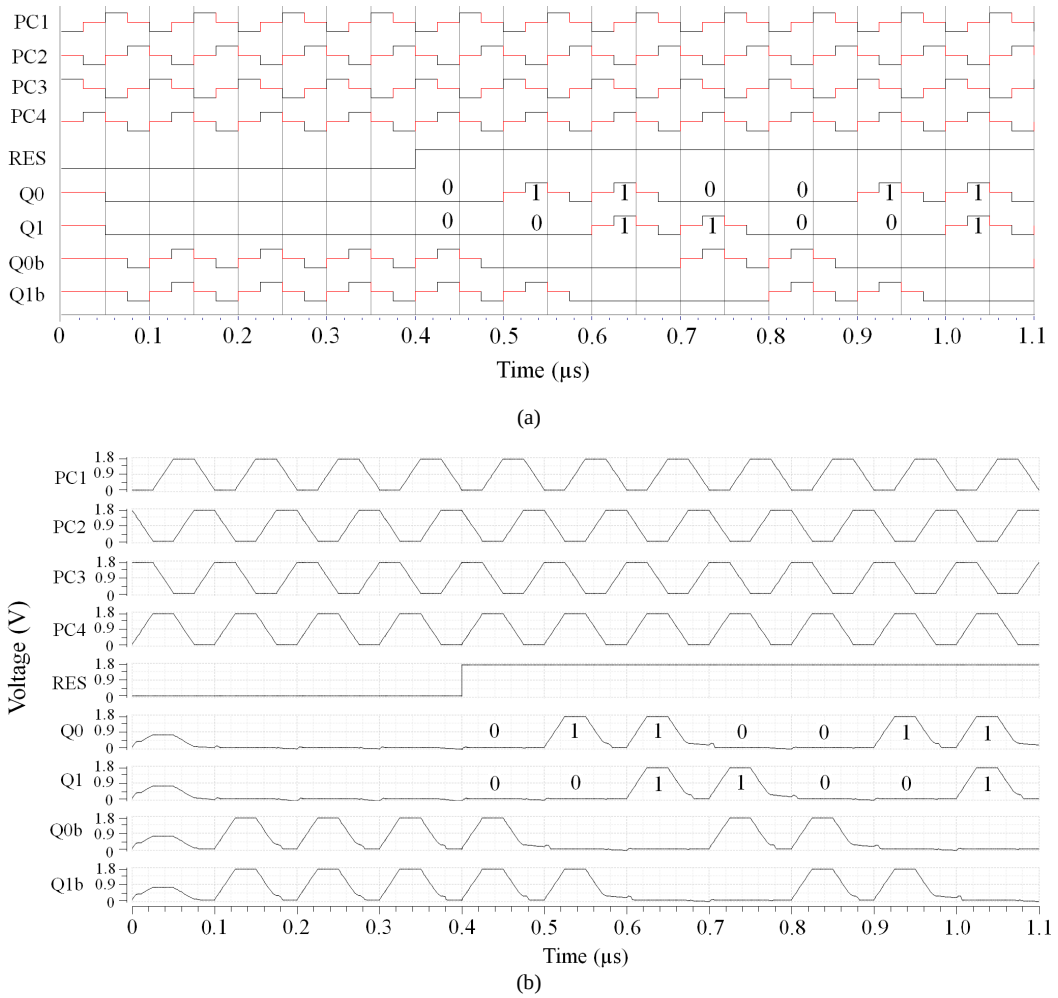


Fig. 8. 2-bit ring counter output waveforms (a) VHDL Model simulation (b) SPICE simulation

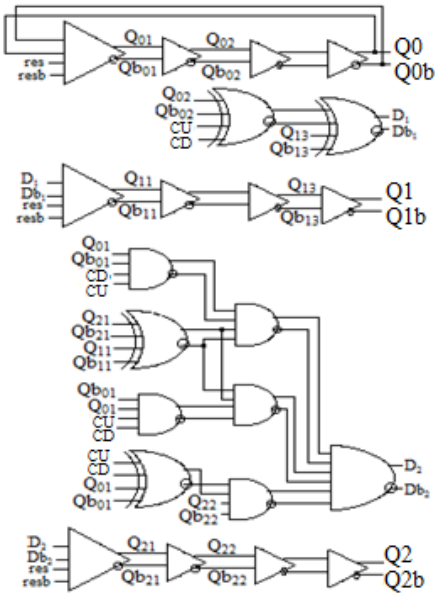
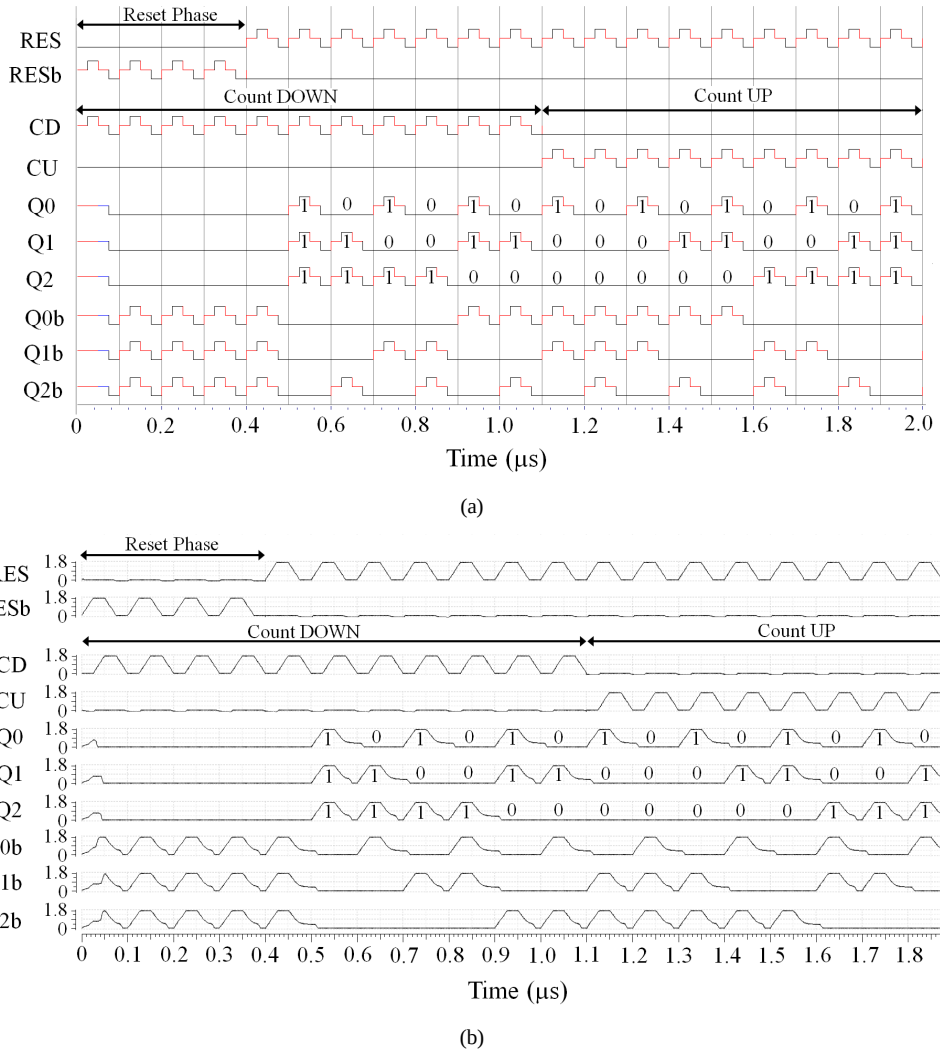


Fig. 9. Circuit diagram of a 3-bit up-down counter.

input. Fig. 8 shows the two output waveforms, one generated using VHDL simulation and the other using SPICE simulation. It is seen from Fig. 8 that there is no variation in the timing verification of the VHDL simulation in comparison to that of the circuit simulation waveform of the ring counter.

As the ring counter does not employ any combinational logic, a 3-bit up-down counter is modelled using HDL. The dual-rail reset signals are coded and converted to the multi-level adiabatic inputs (RES and RESb). The counter starts counting only when the reset signal 'RES' is high. Depending on the 'CD' and 'CU' signals, the counter either count down or up. The boolean expression for the 3-bit up-down counter is given in [17] and its corresponding circuit diagram is given in Fig. 9. The VHDL simulation waveform alongside the SPICE simulation for the 3-bit up-down counter is shown in Fig. 10. The counter design reveals the accuracy of the modelling in terms of timing and representation of the adiabatic logic technique.



(a)

(b)

Fig. 10. 3-bit up-down counter output waveforms (a) VHDL Model simulation (b) SPICE simulation

VI. CONCLUSION

The VHDL-based modelling of the 4-phase adiabatic logic design was proposed. The proposed approach shows the precise time modelling compared to the SPICE level simulation. The approach follows the adiabatic principle which none of the previous modelling approaches in the open literature has followed. The exact behavior of the trapezoidal AC power-clock is represented by presenting all the four periods distinctively using VHDL. The proposed modelling is easy and can be used for the design and validate of a large complex system, eventually reducing the amount of time needed for synchronizing and detecting design errors.

VII. FUTURE WORK

The future scope exists in developing an energy model such that the energy consumption of any 4-phase adiabatic logic families can be fairly approximated before the design of the circuits at transistor level are performed. The energy modelling will not be simple as adiabatic logic energy efficiency has a strong relationship with the frequency of operation, non-adiabatic losses due to threshold voltage degradation and capacitive coupling and dependency on the input transitions.

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