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Low-Cost On-Chip Clock Jitter Measurement Scheme

Martin Omaña, Daniele Rossi, Daniele Giaffreda, Cecilia Metra, TM Mak, Asifur Rahman and Simon Tam

***Abstract*— In this paper we present a low cost, on-chip clock jitter digital measurement scheme for high performance microprocessors. It enables in-situ jitter measurement during the test or debug phase. It provides very high measurement resolution and accuracy, despite the possible presence of power supply noise (representing a major source of clock jitter), at low area and power costs. The achieved resolution is scalable with technology node and can in principle be increased as much as desired, at low additional costs in terms of area overhead and power consumption. We show that, for the case of high performance microprocessors employing Ring Oscillators (ROs) to measure process parameter variations, our jitter measurement scheme can be implemented by re-using part of such ROs, thus allowing to measure clock jitter with very limited cost increase compared to process parameter variation measurement only, and with no impact on parameter variation measurement resolution.**

***Index Terms*— high performance microprocessor, clock jitter, jitter measurement**

I. Introduction

CLOCK is one of the most critical signal in any synchronous system, which has to be distributed throughout the chip by means of a complex network [1]. With the scaling of technology and increase in clock frequency, it is becoming increasingly difficult to guarantee the correctness of clock signals, due to the increasing likelihood of manufacturing defects, clock jitter, duty cycle distortion, Process Parameter Variations (PPV) and Power Supply Noise (PSN) [2, 3, 4].

Jitter affecting clock signal produces uncertainties in its period and rising/falling edges, thus forcing designers to either increase the time margins, or face the possibility of operating malfunctions. For high performance microprocessors, the adoption of minimum time margin is desirable, so that on-chip jitter measurement should be performed during the test or debug phase to validate the design and manufacturing assumptions for the clock. PSN modulating the delay of the clock signal is currently recognized as one of the main causes of clock jitter [4]. It is expected to increase with technology scaling, due to the increasing complexity and integration density, resulting in high switching activities [4, 5, 6].

Together with clock jitter, also PPV occurring during fabrication are increasingly likely and significant with technology scaling. They may induce either performance degradation, or operating malfunctions [7]. Therefore, also PPV mandate on-die measurement during the test and debug phase to validate design and process, possibly drive speed-binning, and eventually dictate design process improvements.

Moreover, if PPV affect the buffers of the clock distribution network, they can cause clock skew [8, 9, 10]. Deskew buffers can be employed to compensate for PPV produced effect [8], but their application is typically still limited to some portions of the whole clock distribution network only (e.g., global distribution), due to cost limitations.

Several measurement schemes have been proposed for clock jitter [4-7, 11-15] and PPV [7, 16, 17]. The use of ring oscillators (ROs) for PPV measurement is widely assessed and adopted. Instead, schemes for clock jitter measurement are not as well established yet, mainly because of limits in their measurement resolution and accuracy [15].

In [14, 15], jitter measurement schemes based on Vernier Delay Lines (VDL) have been proposed. They employ an additional Delay-Locked Loop to calibrate the delay of the elements within the VDL against process, temperature and voltage variations. Although these techniques provide a high measurement resolution, they imply a considerable area overhead**.**

In [13], a circuit based on a NOT chain delay line has been proposed. A counter at the output of each NOT counts the number of CK rising/falling edges propagating to each NOT output within a given time interval. The result is then compared to that expected for a jitter-free CK in order to derive jitter measurement. It features resolution equal to a NOT delay, and requires a considerable area overhead.

Finally, a circuit consisting of latches and NOT chains has been presented in [4]. It is based on a delay line and sampling latches forming an edge-capture circuit. At each clock cycle, the widths of the high and low clock phases are evaluated to derive the clock jitter. It features a measurement resolution equal to an inverter delay, which can be calibrated to compensate the effects of PSN and PPV on the provided measurement. However, the required area overhead and power consumption are not negligible.

Based on the limitations of the approaches proposed so far to achieve high jitter measurement resolution and accuracy at limited costs, in this paper we present a new on-chip digital measurement scheme, whose basic structure has been introduced in [18]. It allows to measure clock jitter with high

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and scalable resolution at limited costs, and with high accuracy despite the presence of PSN. The provided measurement resolution can be higher than a min sized NOT delay, and can in principle be increased as much as desired, with low additional area and power consumption.

The proposed approach is based on a scheme similar to [4], with the following main differences: 1) the implementation of the sampling elements (transfer gates rather than latches); 2) the usage of multiple out-of-phase delay lines in our scheme to increase resolution; 3) the proposal of a sampling strategy to avoid the impact of PSN on jitter measurement.

Compared to [4], our scheme allows a 40% reduction in both area overhead and power consumption. Instead, compared to the approaches in [14, 15], our scheme requires a considerably lower area overhead, while featuring the same measurement resolution.

Then, as introduced in [19], we show that, for high performance microprocessors, the area required by our measurement scheme can be further reduced by re-using and properly modifying part of the ROs often employed for PPV measurement. Our scheme can be set in either the PPV measurement mode, or the clock jitter measurement mode, by acting on an external control signal. The effectiveness of our approach has been verified by means of electrical level simulations, performed considering a PSN up to the 50% of the nominal power supply voltage.

The rest of the paper is organized as follows. In Section II, we present some basics on clock jitter. In Section III, we introduce our proposed jitter measurement scheme, while in Section IV, we report some of the results of the electrical level simulations that we have performed to verify its correct behavior. We show two possible implementations of our jitter measurement scheme, one of which re-uses the ROs that are usually adopted in high performance microprocessors for PPV measurement. In Section V, we evaluate the costs of our scheme and we compare them to those of alternative approaches recently proposed. Finally, we give some conclusive remarks in Section VI.

II. Jitter Affecting Clock Signals

Jitter is the deviation of a signal timing event from its ideal position [20], causing displacements of clock transition times. These displacements are categorized as either deterministic, random, or both. We refer to the following jitter definitions [21]: 1) *timing jitter*, which is the time difference between the actual and ideal signal transition; 2) *period jitter*, which is the time variation of the signal period from its average value; 3) *cycle-to-cycle jitter*, which is the variation in the period of a signal within two following periods. It has been shown that these jitter definitions are mathematically related to each other [21], therefore, in the reminder of this paper, we will consider the *period jitter* only.

Let us first consider the jitter-free clock signal (denoted by *CK*) with 50% duty-cycle. It can be described by (1).

$$CK(t) = \begin{cases} 1 & 0 \le t < \frac{T_{CK}}{2} \\ 0 & \frac{T_{CK}}{2} \le t < T_{CK} \end{cases} \quad (1)$$

In the jitter-free case, the *CK* high and low phase durations ($D_{CK\text{-}H}$ and $D_{CK\text{-}L}$ in Fig. 1(b)) are equal to $T_{CK}/2$. The presence of jitter deviating the *CK* edge by a time $\pm J$ changes the *CK* high phase duration to: $D_{CK\text{-}H} = T_{CK}/2 \pm J$.

A strategy to measure clock jitter consists in measuring the duration of its high and/or low phases over time, and comparing them to their expected duration in the jitter-free case. This is a well assessed and widely adopted approach (employed also in [4]), that we have also considered for our proposed scheme.

III. Proposed Jitter Measurement Scheme

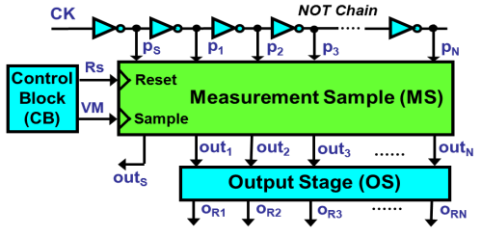
As anticipated above, we measure the duration of clock high and/or low phase(s) over time, and compare the obtained results to those expected for the case of jitter-free clock. For the sake of brevity, we here present the scheme for the clock high phase measurement only, which can be easily extended to measure both clock phases.

A. Scheme with Resolution equal to a NOT Delay

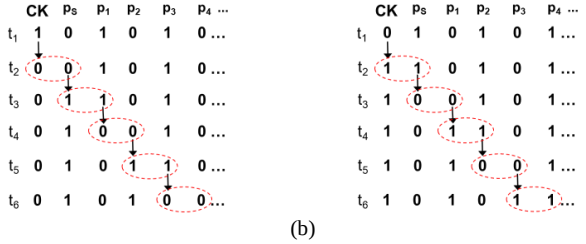
The basic block structure of our proposed scheme is shown in Fig. 1(a). The NOT Chain implements a delay line delaying the input clock signal (*CK*), whose jitter has to be measured, by a given amount of time. The outputs of the NOT gates are sampled by the measurement sample block MS, when the control block CB gives *VM=1*. The output stage OS produces the measurement encoded by a thermometer code. By making R_S=1, CB resets the measurement after a time long enough to allow the system to read it.

Denoting the delay of each NOT in the chain by τ, the total chain delay is $N\tau$. The integer N is such that the total delay covers the whole period T_{CK} of the *CK* under jitter-free conditions. Therefore, it is: $N = \lceil T_{CK}/\tau \rceil$. Considering the clock signal *CK(t)* in 1, and denoting its complemented signal by *CK'(t)*, the signals p_S and p_i (i=1..N) can be represented as:

$$p_S(t) = CK'(t-\tau), \quad p_i(t) = \begin{cases} CK(t-(i+1)\tau), & i\ odd \\ CK'(t-(i+1)\tau), & i\ even \end{cases} \quad (2)$$



(a)



(b)

Fig. 1. (a) Basic block structure of our scheme; (b) schematic representation of the propagation of the CK falling (left) and rising (right) edges within the NOT chain.

The logic values simultaneously present at the outputs of each NOT of the chain after a *CK* falling and rising edge are reported in Fig. 1(b). Each row represents the snap-shot at one specific time instant. The *CK* switches at time t_1 and its falling (rising) edge propagates through the chain. The position within the chain of the *CK* falling (rising) edge is identified by two successive 0s, or two successive 1s, whose location moves progressively to the right. The duration of the *CK* high phase is given by the number of NOTs within the chain that the *CK* rising edge has to pass through, before the *CK* falling edge arrives to the chain input.

In order to account for the effects of PSN, we have considered the realistic model in [22, 23]. It includes also the presence of coupling capacitors, usually employed within the power distribution network (PDN) to reduce the current return paths, thus reducing PSN. However, as shown in [22], even if decoupling capacitors are implemented, the spikes of power supply cannot be smoothed completely.

It is worth noticing that the PDN characteristic impedance seen from different locations inside the PSN topology may exhibit significant differences [24]. Depending also on the operating frequency, the package inductance or the decoupling capacitance might prevail. Particularly, when decoupling capacitors are employed (either at on-chip level, or both at on-chip and on-board level), the supply voltage waveform presents a first triangular peak that is considerably higher than the secondary peaks [25]. Therefore, for evaluation purpose, we have realistically modeled the PSN as a train of narrow triangular pulses [22], whose width depends on the number of switching gates at a single clock period. Moreover, since the pulse width is always very small, the PSN can be modeled as an impulse train with a uniformly-distributed random shift in [0, t_r], where t_r is the rise-time of the clock signal [22]. In our scheme, in order to reduce the effects of PSN on jitter measurement, MS samples the values present on signals p_i (i=1..N) when the *CK* falling edge arrives at the input of the second NOT of the chain (p_s), rather than at the input of the first NOT. This allows the PSN to vanish before sampling. The sampling instant is identified by the condition p_S=p_1=1.

PSN may also influence the delay of some NOT gates while the clock edge travels through the delay line. By means of electrical level simulations, we have verified that only the NOT propagating the *CK* edge when the PSN occurs is impacted, while the sampling circuitry is not. The variation in the delay of the NOT propagating the *CK* edge determines the impact of PSN on measurement accuracy. We have determined the highest variation in NOT delay (worst case), occurring when the PSN is simultaneous to the transition of the NOT propagating the CK edge. It impacts the jitter measurement accuracy of our scheme by only 6.1%. Consequently, we have considered a constant delay τ of the NOTs in the mathematical model of our scheme behavior.

The useful bits representing the jitter measurement start from the output of the second NOT of the chain, denoted by p_1. The output p_S, together with its associated signal out_S is used by the control block CB to determine the sampling instant. Our scheme samples the outputs of the NOT chain at a time instant denoted by t_S, after the *CK* rising edge. It is:

$$t_s = D_{CK\text{-}H} + \tau = T_{CK}/2 \pm J + \tau. \quad (3)$$

At time t_S, CB asserts *VM*, and the values on signals p_S and p_i (i=1..N) are sampled by MS and provided as outputs on out_s and out_i (i=1..N), respectively. We determine the logic values sampled on each out_i by making t=t_S in (2). We obtain:

$$out_i = p_i(t_S) = \begin{cases} CK\left(\frac{T_{CK}}{2} \pm J - i\tau\right), & i\ odd \\ CK'\left(\frac{T_{CK}}{2} \pm J - i\tau\right), & i\ even \end{cases} \quad (i = 1..N) \quad (4)$$

After sampling, the OS block (Fig. 1(a)) complements signals out_i with i odd, so that it is:

$$o_{Ri} = \begin{cases} out_i', & i\ odd \\ out_i, & i\ even \end{cases} \quad (i = 1..N) \quad (5)$$

Then, by combining (4) and (5), we obtain:

$$o_{Ri} = CK'\left(\frac{T_{CK}}{2} \pm J - i\tau\right) \quad (i = 1..N) \quad (6)$$

The word on o_{Ri} (i=1..N) is encoded by the thermometer code, as shown in Fig. 2. It consists of a number of 0s equal to i_0, followed by $(N- i_0)$ 1s, so that:

$$o_{Ri} = \begin{cases} 0, & if\ 1 \le i \le i_0 \\ 1, & if\ i_0 \le i \le N \end{cases} \quad (7)$$

According to (6), $o_{Ri} = 0$ ($\forall i \le i_0$) if the argument of *CK'* is greater than or equal to 0. Thus, we can simply obtain the value of i_0 by equating the argument of *CK'* in (6) to 0, that is: $T_{CK}/2 \pm J - i\tau = 0$, for $i = i_0$. Consequently, it is:

$$i_0 = \frac{1}{\tau}\left(\frac{T_{CK}}{2} \pm J\right). \quad (8)$$

The *resolution* (*Res*) of our scheme is given by the minimum variation in the *CK* high phase duration resulting in one more 0 (1) at the outputs o_{Ri}. The *Res* value can be determined as the difference between the arguments of o_{Ri} and $o_{R(i+1)}$, when it is o_{Ri}=*0* and $o_{R(i+1)}$=*1*. Therefore:

$$Res = \left(\frac{T_{CK}}{2} \pm J - i\tau\right) - \left(\frac{T_{CK}}{2} \pm J - (i+1)\tau\right) = \tau \quad (9)$$

As expected, the resolution is equal to the NOT delay τ.

The thermometer encoding produced by our scheme allows to easily derive the clock jitter measurement. The encoded word o_{Ri} (i=1..N) can be compared with that expected in the case of jitter-free *CK* through *N* parallel XORs. The comparison results in an N-bit vector with a number of 1s equal to the difference between the number of 0s in the produced encoded word and in the expected one. The number of 1s can be counted, and jitter measurement can be obtained by multiplying it by the scheme resolution. After a time long enough to allow the system to read the performed measure, the scheme can be reset by asserting R_S, thus making it ready for a following measurement. We assume signal *Rs* is activated every other *CK* cycle. We use a periodic signal *GR* with half

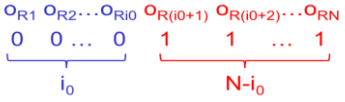


Fig. 2. Word produced by our scheme at the outputs of OS.

the *CK* frequency to generate the R_S pulse upon its rising edge. The timing of these signals are shown in Fig. 3.

B. Scheme with Resolution of Half NOT Delay

To obtain a resolution higher than a NOT delay (τ), we replace the basic block scheme in Fig. 1(a) with that in Fig. 4(a), employing two NOT chains, rather than one. NOT chain 1 consists of NOTs each with a delay equal to τ. Instead, in NOT chain 2, the first NOT has a delay equal to $(1+½)\tau$, while all other NOTs have a delay equal to τ. This way, the outputs of the corresponding NOTs of the two chains have a $\tau/2$ phase difference. The timings of the signals *VM* and R_S of our scheme in Fig. 4(a) are the same as shown in Fig. 3.

Considering the signal *CK(t)* in (1), we represent signals p_S and p_{ji} ($i=1..N$; $j=1,2$) as a function of time as follows:

$$p_S = CK'(t-\tau)$$

$$p_{1i}(t) = \begin{cases} CK(t-(i+1)\tau), & i\ odd \\ CK'(t-(i+1)\tau), & i\ even \end{cases} \quad (i=1..N) \qquad (10)$$

$$p_{2i}(t) = \begin{cases} CK'\left(t-\left(i+\frac{1}{2}\right)\tau\right), & i\ odd \\ CK\left(t-\left(i+\frac{1}{2}\right)\tau\right), & i\ even \end{cases} \quad (i=1..N) \qquad (11)$$

As described before, to achieve low sensitivity to PSN, the values at the outputs of the NOT chains are sampled by MS at time $t_S = T_{CK}/2 \pm J + \tau$. This occurs when the *CK* falling edge arrives at the input p_S of the second NOT of chain 1 (i.e., when $p_S=p_{12}=1$). MS receives the signal p_S together with the $2N$ signals p_{ji} ($i=1..N$; $j=1,2$) from the NOT chains, and it outputs the signal out_S (the sampled value of p_S), together with the signals out_m ($m=1..2N$). These latter signals are the sampled value of p_{21}, p_{11}, p_{22}, p_{12}, p_{23}, and so on, which represent the jitter measure. At the sampling instant t_S, it is:

$$out_m = \begin{cases} p_{2[m/2]}(t_S), & m\ odd \\ p_{1(m/2)}(t_S), & m\ even \end{cases} \quad (m=1..2N) \qquad (12)$$

Such signals feed the block OS, which performs the same function as in (5). This way, the jitter measurement on o_{Rm} ($m=1..2N$) is encoded by a thermometer code. It is:

$$o_{Rm} = CK'\left(\frac{T_{CK}}{2} \pm J - \frac{m}{2}\tau\right) \Rightarrow o_{Rm} = \begin{cases} 0, & 1 \le m \le m_0 \\ 1, & m_0 \le m \le 2N' \end{cases} \qquad (13)$$

where m_0 is the order of the last $o_{Rm}=0$. According to (13) and Fig. 1(b), it is $o_{Rm}=0$, if the argument of *CK'* is greater than or equal to 0. The value of m_0 can be obtained by equating the argument of *CK'* in (13) to 0. It is:

$$m_0 = \frac{2}{\tau}\left(\frac{T_{CK}}{2} \pm J\right) \qquad (14)$$

The *Res* of our scheme in Fig. 4(a) can be expressed as the difference between the arguments of o_{Rm} and $o_{R(m+1)}$, when it is $o_{Rm}=0$ and $o_{R(m+1)}=1$. From (13), it derives that:

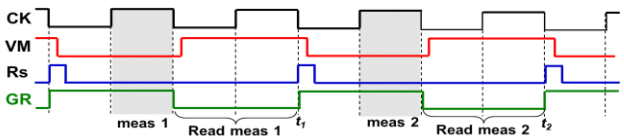


Fig. 3. Schematic representation of the timing of signals VM and R_S.

$$Res = \left(\frac{T_{CK}}{2} \pm J - \frac{m}{2}\tau\right) - \left(\frac{T_{CK}}{2} \pm J - \frac{(m+1)}{2}\tau\right) = \frac{\tau}{2}. \qquad (15)$$

As expected, *Res* is equal to half the delay of a min-sized NOT. Therefore, the resolution of our measurement scheme can be scaled by properly adding a NOT chain to the scheme in Fig. 2(a), and by properly sizing their NOTs.

C. Scheme with Resolution Higher than Half NOT Delay

Our approach can be scaled to achieve a resolution even higher than $\tau/2$ by considering a number of NOT chains greater than 2.

Let us consider the general case of n chains. Chain 1 still consists of NOTs each with an delay equal to τ. As for the remaining *n-1* NOT chains, the first NOT of the *j-th* NOT chain ($j=2..n$) has a delay $d_{j1} = (1+(j-1)/n)\tau$ ($j=2..n$), while all other NOTs have a delay equal to τ.

By considering as output the alternated succession of the n NOT chain outputs (i.e., p_{21}, p_{31}, …, p_{n1}, p_{12}, p_{22}, p_{32}, …, p_{n2}, etc.), any two following outputs will have a phase difference equal to τ/n. The expressions of signals p_S and p_{ji} ($i=1..N$; $j=1..n$), as a function of time, are:

$$p_S = CK'(t-\tau)\,,$$

$$p_{1i}(t) = \begin{cases} CK(t-(i+1)\tau), & i\ odd \\ CK'(t-(i+1)\tau), & i\ even \end{cases} \quad (i=1..N) \qquad (16)$$

$$p_{ji}(t) = \begin{cases} CK'\left(t-\left(i+\frac{j-1}{n}\right)\tau\right), & i\ odd \\ CK\left(t-\left(i+\frac{j-1}{n}\right)\tau\right), & i\ even \end{cases} \quad (i=1..N;\ j=2..n)$$

Extending the function of the OS block (13) to the case of n NOT chains, the outputs o_{Rm} of the scheme with n NOT chains can be expressed as:

$$o_{Rm} = K'\left(\frac{T_{CK}}{2} \pm J - \frac{m}{n}\tau\right) \Rightarrow o_{Rm} = \begin{cases} 0, & if\ 1 \le m \le m_0 \\ 1, & if\ m_0 \le m \le n \times N \end{cases} \qquad (17)$$

where m_0 is the order of the last o_{Rm} signal equal to *0*, and can be expressed as:

$$m_0 = \frac{n}{\tau}\left(\frac{T_{CK}}{2} \pm J\right) \qquad (18)$$

The resolution of our scheme with n NOT chains is given by the difference between the arguments of o_{Rm} and $o_{R(m+1)}$, when $o_{Rm} = 0$ and $o_{R(m+1)} = 1$. From (18), it is:

$$Res = \left(\frac{T_{CK}}{2} \pm J - \frac{m}{n}\tau\right) - \left(\frac{T_{CK}}{2} \pm J - \frac{(m+1)}{n}\tau\right) = \frac{\tau}{n} \qquad (19)$$

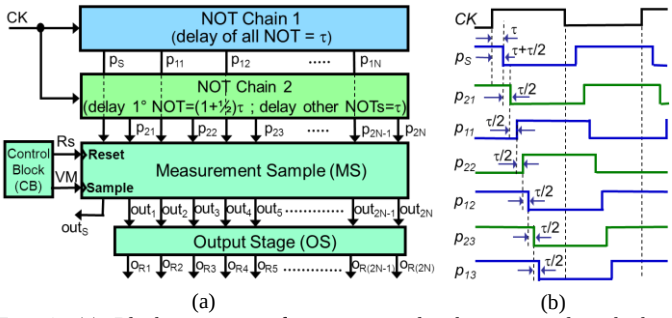


Fig. 4. (a) Block structure of our proposed scheme providing higher measurement resolution than that in Fig. 3; (b) representation of the signals produced at the outputs of its NOT chains.

The achievement of an increasingly higher resolution by augmenting the number of NOT chains is limited by the difficulty in controlling the NOT delays, due to PPV. To solve this issue, the NOT chains can be implemented by using balanced delay lines [26], or inverters whose delay can be calibrated after fabrication [27].

IV. Implementation and Verification

Two possible implementations of our scheme to measure the *CK* high phase are here described. We consider a standard 65nm CMOS technology [28], V_{DD} = 1.1V, 3GHz clock frequency and two NOT chains (Fig. 4(a)). Particularly, first we introduce a possible implementation, in which we have designed all blocks required by our scheme (and introduced in Sect. III). Then we present a possible implementation reusing ring oscillators (ROs) usually present in high performance microprocessors for PPV measurement. Finally, we show some results of the HSPICE electrical level simulations that we have performed to verify the behavior of our scheme.

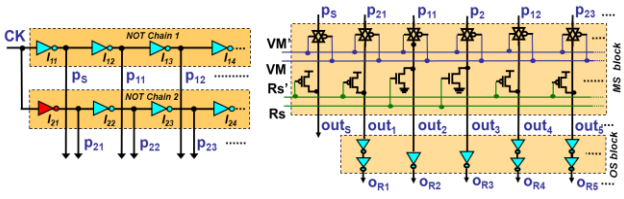
A. Implementation Non Re-using Ring Oscillators

Let us consider the two NOT chains (Fig. 5(a)). In chain 1, all NOTs exhibit a delay $\tau \cong$ 12ps; in chain 2, the first NOT has a delay equal to $(1 + ½)\tau \cong$ 18ps, while all other NOTs have a delay τ. Since each chain needs to cover T_{CK} (≅333ps), the number of NOTs within each chain is $N=\lceil T_{CK}/\tau \rceil$ =28.

As for MS and OS, their possible implementation is shown in Fig. 5(b). The inputs of MS (p_S and p_{ji} j=1..2; i =1..N) are connected to its outputs (out_S and out_m m=1..2N, respectively) through transfer gates (TG) driven by *VM* and *VM'*. This way, when *VM*=0, all TGs conduct and connect the outputs of the NOT chains to signals out_S and out_m. Instead, when *VM* flips to 1, all TGs are turned off, so that the outputs of the NOT chains are sampled. Signals out_S and out_m remain in a high impedance state, keeping latched the logic values till reset.

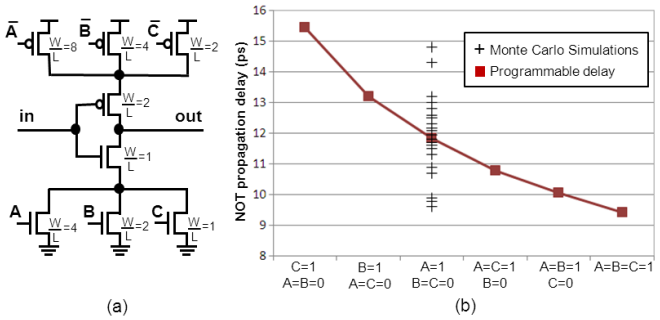
As for OS, it buffers the out_m (m=1..2N) signals and encodes them by a thermometer code on signals o_{Rm}. The sampled data must be maintained for one clock cycle only. Therefore, dynamic latches have been considered, rather than more costly static latches, in order to reduce implementation costs. When R_s is asserted, *VM* flips to 0, making all TGs conductive again. As a result, all signals o_{Rm} become equal to 1, thus removing the previous measurement results.

The outputs of the NOTs at the same level i (i = 1..N) within the *j-th* chain (j = 1, 2) present a phase difference of $\tau/2 \cong$ 6ps. According to (15), this is also the resolution provided by our scheme. To compensate possible PPV occurring during manufacturing, the inverter chains have been implemented by NOTs with a programmable delay [27], as shown in Fig. 6(a). By means of Monte Carlo simulations, we have evaluated the variations in the NOT delay due to PPV. The achieved results are reported in Fig. 6(b). We can observe that the variations of the NOT delay are within a range of approximately the ±20% of its nominal value of 12ps. Fig. 6(b) also shows that, by properly setting to 1 the program signals (i.e., A, B and C) of the considered NOT, the delay of the NOT can be adjusted in order to compensate the variations due to PPV.



(a) (b)

Fig. 5. Possible implementation of: (a) the NOT chains; (b) the *MS* and *OS* blocks.



(a) (b)

Fig. 6. (a) Implementation of the considered NOTs with programmable delay; (b) Propagation delay variation in case of process parameter variations as a function of the program signals (A, B and C).

PPV may also imbalance the low-to-high and high-to-low transitions of the NOTs. However, we have verified this negligibly impacts the duty cycle of the clock (by less than 1%), whose jitter is being measured. This is due to the fact that the CK edges are inverted at each NOT of the chain, so that both CK edges propagate as low-to-high and high-to-low transitions. This way, even if the NOTs present different low-to-high and high-to-low transition times, the CK duty-cycle is negligibly impacted. The delay of the NOTs is also sensitive to voltage and temperature variations. Such a sensitivity may be reduced by employing one of the techniques that have been proposed in the literature for the on-chip compensation of voltage and temperature variations (e.g., that in [29]).

As for CB, Figs. 7(a) and 7(b) show an implementation of the circuits generating *VM*, R_S and their complemented signals. Signals *VM* and *VM'* should be fine-tuned in order to avoid any systematic error. Their delays can be equalized by considering the scheme in Fig. 7(a). Signal *VM* (*VM'*) should flip to 1 (0) when p_S=p_{12}=*1*, and it should be kept at this value till reset. This can be obtained by exploiting signals out_S and out_4 generated at the output of MS, that remain latched at the high logic value till reset. The reset signal R_S (and R_S') is activated every other *CK* cycle, and may be implemented by the circuit in Fig. 8(b). The signal *GR* can be obtained by a standard divide-by-2 circuit [30].

(a) (b)

Fig. 7. Possible implementation of circuits generating: (a) VM and VM'; (b) R_S' and R_S.

B. Implementation Re-using Ring Oscillators

Our jitter measurement scheme can be implemented by re-using and properly modifying part of the ROs. This allows to further reduce the area overhead of our proposed scheme. In this regard, we refer to the PPV measurement strategy in [16]: it consists of many Functional Unit Blocks (FUBs), each composed by q ROs with K (usually equal to 99) NOTs. The FUB internal structure is shown in Fig. 8 [12]. The NOTs within each RO are equal to each other. Instead, the ROs within the same FUB are generally different to allow a more accurate measurement of PPV [16]. Some ROs consist of minimum sized NOTs, others are 2X, 3X, etc.

As an example, let us consider the re-use of two ROs, allowing us to achieve a measurement resolution equal to $\tau/2$, as shown in Fig. 9. The delay of each NOT chain should cover the whole T_{CK}, thus N=28 NOTs out of the 99 available are re-used. We modified the FUB in Fig. 8 by connecting multiplexers M1 and M2 to the input of the NAND gates N1 and N2, respectively. This way, by externally acting on the control signal *JT*, our scheme can be easily set in either the PPV measurement mode (*JT*=1), or the clock jitter measurement mode (*JT*=0). Blocks MS, OS and CB in Fig. 9 are the same as in our implementation non re-using ROs. *CK* (*CKd*) must propagate through M1 (M2) and N1 (N2) before entering the NOT chain. As discussed in Section III, the jitter measure is sampled when p_S=p_{11}=1 and the *CK* falling edge arrives to the input of the first NOT of the upper RO, thus making it immune to PSN. As for the NOTs of the chains, we cannot implement them featuring a programmable delay to compensate PPV. However, by initially configuring the FUBs in the PPV measurement mode, we can determine the variation in the delay of the NOTs of the ROs over the nominal value. This makes it possible to correct possible clock jitter measurement errors induced by the presence of PPV.

C. Verification

We show some of the results of the HSPICE simulations that we have performed to verify the behavior of our jitter measurement scheme, considering both the implementations in Sections IV.A and IV.B. The PSN has been modeled as described in Section III.A, with a peak value of 50% of V_{DD}. We also account for the setup and hold times of the sampling circuits, whose values are: $t_{set\text{-}up} \cong$2.2ps, $t_{hold} \cong$ 10fs.

Our scheme non re-using ROs produces an output o_{Rm} as in (13). Thus, when no jitter affects *CK* (i.e., *J=0*), outputs o_{Rm} are encoded by a thermometer code with a number of zeros equal to $m_0 = T_{CK}/\tau$ = 168ps/6ps = 28. Fig. 10 shows the simulation results considering the case with no jitter affecting the first measured *CK* high phase (*CK HP 1*), and a jitter of

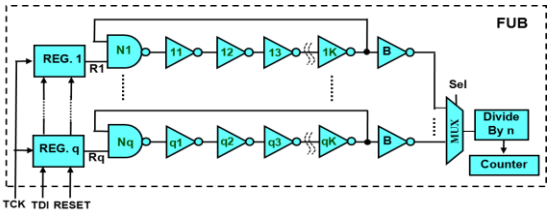


Fig. 8. Internal structure of the FUBs in [12].

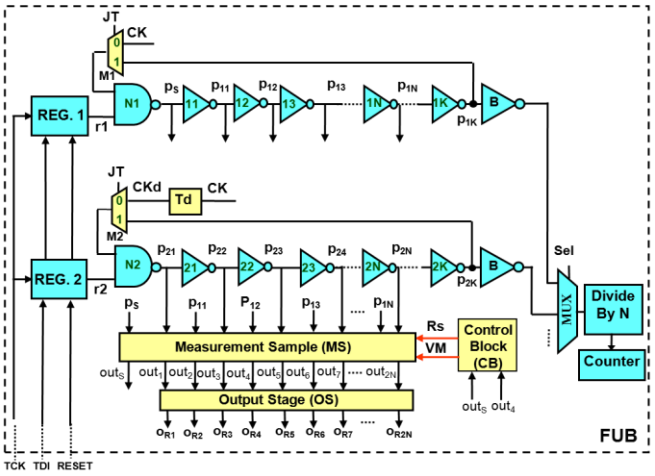


Fig. 9. Implementation of our jitter measurement scheme with two re-used ROs of the scheme in Fig. 9, for the case of *Res* = $\tau/2$.

7ps widening the secondly measured *CK* high phase (*CK HP 2*). As expected, when no jitter occurs (*CK HP 1*), while *VM*=1 (*Valid meas 1*) our scheme outputs a word encoded by the thermometer code with 28 zeros (i.e., o_{Rm}= *0* for $1 \le m \le m_0$=28, o_{Rm} = 1 for $29 \le m \le 58$). Since we measure jitter as the difference in the number of zeros between the produced output and the one expected for the jitter-free case (equal to 28) multiplied by the resolution of our scheme (equal to 6ps), we correctly obtain a measurement of jitter equal to 0ps.

Instead, when for instance a jitter of *J*=7ps affects *CK* (*CK HP 2*), while *VM*=1 (*Valid meas 2*) our scheme outputs a word encoded by the thermometer code with 29 zeros (i.e., o_{Rm} = 0 for m = 1..29, o_{Rm} = 1 for i = 30..58), thus resulting in a jitter measure equal to *J*=6ps, with 1ps measurement error. Therefore, our scheme is able to measure jitter with the expected resolution of 6ps, even in presence of PSN.

As for the implementation of our scheme reusing ROs, we have verified that: 1) the PPV measurement accuracy of the original FUB in [16] is not degraded; 2) the clock jitter measurement accuracy is the same as for the implementation of our scheme non re-using ROs.

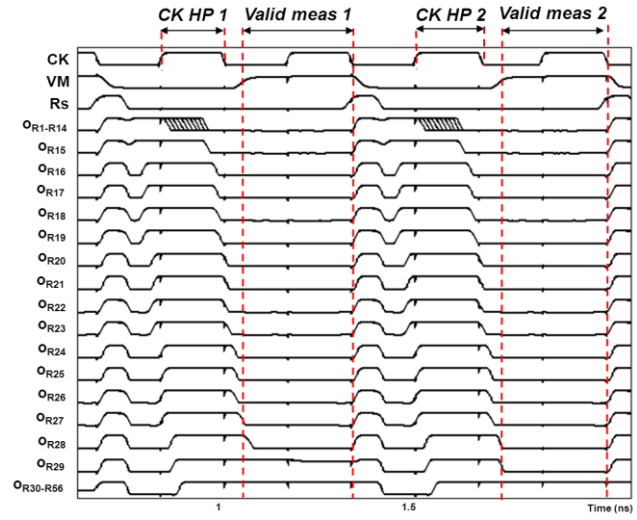


Fig. 10. Simulation results for nominal values of electrical parameters, considering a power supply noise of 50% of V_{DD}.

As for point 1), we have compared the oscillation period of the ROs of the original FUB (T_{RO_orig}) with that of the ROs re-used by our scheme for jitter measurements (T_{RO_our}), as a function of parameters V_{th} and T_{ox}. Figs. 11(a) and 11(b) show T_{RO_orig} and T_{RO_our}, as a function of V_{th} and T_{ox} variations (ΔV_{th} and ΔT_{ox}) up to ±30% of their nominal values. As we can see, the relative difference between T_{RO_our} and T_{RO_orig} is always negligible, with 4% maximum increase with V_{th} variation, and 3% with T_{ox} variation. Similar results have been achieved for other process parameter variations. Therefore, the re-use of the ROs of the FUB in [16] to allow also clock jitter measurement does not impact the PPV measurement accuracy.

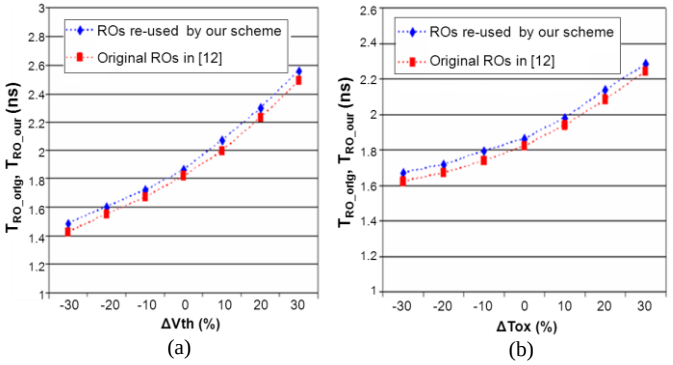
As for point 2), since all NOTs of the two re-used and modified ROs present a delay τ of 12ps, our scheme should provide a clock jitter measurement resolution of $Res = \tau/2 \cong$ 6ps. Fig. 12 shows the simulation results obtained for nominal values of electrical parameters and with a PSN of 50% of V_{DD}. The two cases of no clock jitter (*CK HP 1*), and clock with a jitter of 7ps widening the second measured *CK* high phase (*CK HP 2*) are depicted. As expected, with no jitter, while *VM*=1 (*Valid meas 1*) our scheme provides on o_{Rm} the same encoded word with 28 0s as for the implementation without re-using ROs. Analogously, the same results have been obtained considering a jitter of 7ps affecting the *CK* high phase (*CK HP 2*), with a word encoded by the thermometer code containing 29 0s. Therefore, our jitter measurement scheme implemented by re-using the ROs of the FUB is able to measure clock jitter with the same resolution as the scheme in Subsection IV.A.

V. Costs and Comparison

We have evaluated the costs of our proposed scheme, implemented with and without re-using ROs, in terms of additional area and power consumption. We have compared it to the schemes in [4, 14, 15]. Since neither implementation details, nor costs are reported in [13], it has not been considered for comparison.

As for [4, 14], they feature the same resolution as our approach implemented with one NOT chain, which for the considered 65nm CMOS technology is equal to 12ps.

For comparison purposes, the latches and logic gates of the scheme in [4] have been implemented as the standard latch in [31], and minimum sized symmetric logic gates. The area of our scheme and [4] has been roughly estimated as the gate area of all transistors, while their power consumption has been evaluated by HSPICE simulations. As for [14], we considered the costs reported by the authors, which refer to a true implementation on a test chip with a 65nm CMOS technology.



(a) (b)

Fig. 11. Oscillation periods of the ROs in [12] (TRO_orig), and of the ROs re-used by our jitter measurement scheme (TRO_our), as a function of: (a) threshold voltage Vth; (b) oxide thickness Tox.

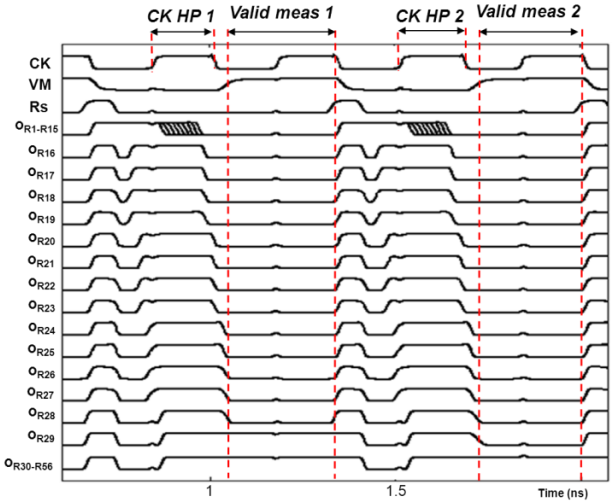


Fig. 12. Simulation results for nominal values of electrical parameters, considering a power supply noise of 50% of V_{DD}.

The obtained results are reported in Table 1. As can be seen, when our scheme does not re-use the ROs of the FUBs, it allows a 40% reduction in both additional area and power over [4]. Compared to [14], our approach allows 99.7% additional area reduction. Instead, our scheme requires a power higher than [14] by 11% only, for an operating frequency 30 times higher (3GHz vs 100MHz).

On the other hand, when our approach is implemented by re-using the ROs of the FUBs, it allows 74% and 30% reduction in area and power consumption, respectively, over the approach in [4]. Compared to [14], in this case our approach allows a 99.9% reduction in area. Instead, as for power, it is 28% higher, for an operating frequency 30 times higher. The area reported for the scheme in [14] refers to a true implementation on a test chip, while for our scheme is a rough estimation of the gate area of all transistors. Nevertheless, since the area reduction allowed by our approach is very high, we can expect a favorable comparison also considering the costs of its implementation on a chip.

From Table 1, it can be noticed that by re-using the ROs of the FUBs to implement our jitter measurement scheme we obtain a considerable reduction of additional area over our scheme not re-using the ROs (approximately 55%). However, the re-use of ROs requires a limited increase in power consumption (approximately 15%), compared to the case with no ROs re-use. This is because our scheme with not re-used ROs is implemented with a NOT chain composed by only 29 NOTs (Section IV), while our scheme re-using the ROs employs all K=99 NOTs of the re-used RO.

TABLE 1
AREA AND POWER COSTS OF THE COMPARED SCHEMES, AND RELATIVE REDUCTIONS (Δ(%) = 100([4,14]-OUR)/[4,14]).

	Additional Area (μm^2)	ΔA (%)		Additional Power (μW)	ΔP (%)	
		[4]	[B]		[4]	[B]
Scheme in [4]	14.1	-	-	1048 (@3GHz)	-	-
Scheme in [B]	2700	-	-	570 (@100MHz)	-	-
Our scheme not re-using ROs	8.3	-41%	-99.7%	634 (@3GHz)	-40%	+11%
Our scheme Re-using ROs	3.7	-74%	-99.9%	730 (@3GHz)	-30%	+28%

As for [15], it features the same resolution as our approach implemented with four NOT chains equal to 3ps for the considered 65nm CMOS technology. The results are reported in Table 2. We can see that, if our scheme does not re-use ROs, it allows a 94% reduction in additional area, while by re-using four ROs of the FUB, it allows a 97% area reduction.

Similarly to [14], the area reported for the scheme in [15] in Table 2 refers to a true implementation on a test chip. As before, since the area reduction allowed by our approach is very high, we can expect a favorable comparison also in the case of its implementation on a chip.

TABLE 2
AREA AND POWER COSTS OF THE COMPARED SCHEMES, AND RELATIVE REDUCTIONS (Δ(%) = 100([15]-OUR)/[15]).

	Additional Area (μm^2)	ΔA (%)	Additional Power (μW)
Scheme in [A]	490	-	N/A
Our scheme not re-using ROs (2 NOT chains)	31	-94%	1525
Our scheme Re-using ROs (2 NOT chains)	12	-97%	1738

VI. CONCLUSIONS

We have proposed an on-chip clock jitter measurement scheme for high performance microprocessors. The scheme enables in-situ jitter measurement during the test or debug phase. It allows to achieve very high and scalable measurement resolution and accuracy, despite the presence of power supply noise. We have shown that, when our scheme is implemented to feature the same resolution as the previous approach in [4], it allows a 40% reduction in both area and power consumption. Instead, compared to the approaches in [14, 15], our scheme requires a considerably lower area overhead, while featuring the same measurement resolution.

We have also shown that, for the case of microprocessors employing Ring Oscillators to measure process parameter variations, our jitter measurement scheme can be implemented by re-using part of the ROs, thus allowing a 55% reduction of additional area over our scheme not re-using the ROs.

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[31] N.H.E. Weste, K. Eshraghian, "Principles of CMOS VLSI Design: A System Pespective", Addison Wesley, 1993, Chapter 5, page 327, Figure 5.54 (b).

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