(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 October 2015 (01.10.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/144771 A1

(51) International Patent Classification:
H03M 3/00 (2006.01)

(21) International Application Number:
PCT/EP2015/056425

(22) International Filing Date:
25 March 2015 (25.03.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1405451.4 26 March 2014 (26.03.2014) GB

(71) Applicant: **UNIVERSITY OF WESTMINSTER** [GB/GB]; 309 Regent Street, London W1B 2UW (GB).

(72) Inventors: **KALE, Izzet**; 309 Regent Street, London W1B 2UW (GB). **TALEBZADEH, Jafar**; 309 Regent Street, London W1B 2UW (GB).

(74) Agent: **BAWDEN, Peter**; Bawden & Associates, 4 The Gatehouse, 2 High Street, Harpenden, Hertfordshire AL5 2TH (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

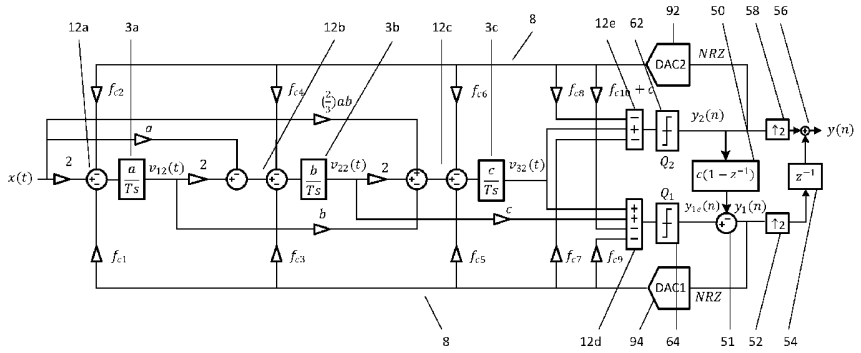
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: TIME INTERLEAVED DELTA SIGMA MODULATORS

Figure 7: A 3rd-order single-loop two path CTTI ΔΣ modulator.



(57) **Abstract**: In order to overcome the so-called delayless path problem, a time interleaved delta sigma modulator includes a plurality of paths for respective time interleaved data channels, said paths comprising a feed forward path arrangement, including first, second and third filter stages (3a, 3b, 3c), a first path including a first quantizer (Q1 64) being connected to a first feedback path (8) including a first DAC (94), a second path including a second quantizer (Q2 62) being connected to a second feedback path (8) including a DAC (92), and the output of the first DAC having a coupling (31) to the input of the second quantizer intentionally introducing errors in the analog domain, and the output of the first quantizer being coupled to the output of the second quantizer via a correction means performing a difference between the present time sample and the previous one and correcting the intentional errors introduced by said coupling (31).

WO 2015/144771 A1

TIME INTERLEAVED DELTA SIGMA MODULATORS

Field of the invention

This invention relates to Delta Sigma modulators.

Background of the invention

Delta Sigma (DS, or ΔΣ) modulators have applications in Analogue to Digital Converters (ADCs), Digital to Analogue Converters (DACs), Class D amplifiers, etc. They have become very popular converters for high-resolution applications because of their oversampling and noise shaping nature. These characteristics make them more robust to their components' nonlinearities and nonidealities. Indeed, by trading accuracy with speed, DS converters have become more attractive in the context of present CMOS technology evolution. The rapid growth of the portable communication device markets such as audio systems and consumer electronics has been led to an increasing demand for low power high resolution ADC designs over the last decade. The ΔΣ modulator can achieve a very high resolution analog-to-digital conversion for relatively low-bandwidth signals by using the oversampling and the noise shaping techniques. It is known that ΔΣ modulators do not require precise analog components and sharp cut-off frequencies for their analog anti-aliasing filters.

The noise-shaping loop filter of a ΔΣ modulator can be implemented as a single-loop Discrete-Time (DT) structure (Figure 1a) by using Switched-Capacitor (SC) circuits or as a single–loop Continuous-Time (CT) structure (Figure 1b) through active-RC or Gm-C filters. In Figures 1a and 1b, the reference numbers and symbols employed are applied throughout the remaining Figures to similar items. Referring to Figure 1a, a DT modulator accepts an input x(n), which is fed to a single loop comprising a feed-forward path 2 including a filter (accumulator) 4, which provides an output q(n) to an Analog to Digital Converter ADC 6 (quantizer), the output of the ADC providing the output y(n) of the modulator. The output of the modulator is fed in a feedback path 8, which includes a DAC 10, the output of the DAC being subtracted from the input signal in a combiner 12. Filter 4 is of a switched capacitor type, providing an accumulation function, and its transfer function is $H_d(z)$, where z is the z-transform for discrete time systems. The transfer function for DAC 10 is $H_{dDAC}(z)$. Switched Capacitor filter circuits of DT

structures are insensitive to clock jitter and the frequency response of the noise-shaping filter can be relatively accurately set by capacitor ratios.

For the purposes of the present specification, and in the context of ΔΣ modulation, the terms Analog to Digital Converter, ADC, and quantizer are regarded as having the same meaning.

Referring to Figure 1b, a CT ΔΣ modulator has an input signal x(t) applied to a single loop comprising a Continuous Time (CT) integrator filter 3 in its feed forward path 2, providing an output $q_c(t)$ followed by a sample and hold switch 5, providing an output $q_c(nT)$, which is fed to ADC (quantizer) 6. ADC 6 provides an output y(n), which is fed back in feedback path 8 via DAC 9 to combiner 12, where it is subtracted from the input signal x(t).

Filter 3 and DAC 9 in the feedback path 8 are represented by Laplacian transfer functions in the continuous time domain $H_c(s)$, $H_{cDAC}(s)$. Filter 3 provides an integration function. CT ΔΣ modulators benefit from operating at higher sampling frequencies in comparison to their DT counterparts. The errors of the sample-and-hold circuit are shaped by the loop filter and CT ΔΣ modulators have an implicit anti-aliasing filter in their forward signal path. However, CT ΔΣ modulators suffer from several drawbacks: excess loop delay, jitter sensitivity and RC time constant variations.

The signal bandwidth that ΔΣ modulators can deal with is narrow and is restricted by the OverSampling Ratio (OSR) and deployed technology. To increase the signal bandwidth the modulator can process, a variety of methods are used. The first one is to increase the order of the modulator. ΔΣ modulators commonly have a filter (accumulator or integrator) in the forward signal path. Inserting a second integrator in the feed forward path converts the modulator from first order to second order. The order may be increased at will, but at a price, where the stability problem needs to be dealt with very carefully.

The second is to increase the number of bits for the ADC/quantizer, which makes the modulator more complicated. The third is to increase the sampling frequency. However, the most serious disadvantage of the third method is the technology limitations.

A fourth method to increase bandwidth is to employ the time-interleaving (TI) technique. This is a known technique which is based on a concept of an array or plurality of ΔΣ modulators coupled in parallel to an input sampled

signal, each modulator providing a respective processing channel. The input samples are distributed cyclically to the modulator channels, one sample to the first modulator channel, the next sample to the second, etc., In this way, for M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR become M times the clock rate and the OSR of each modulator respectively. It should be noted that the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer. Much work has been carried out to simplify the design of TI ΔΣ modulators, see M. Kozak, M. Karaman, and I. Kale, "Efficient Architectures for Time-Interleaved Oversampling Delta-Sigma Converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 8, pp. 802–810, Aug. 2000; M. Kozak and I. Kale, "Novel Topologies for Time-Interleaved Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 47, no. 7, pp. 639–654, Jul. 2000. It has been demonstrated that a TI structure with a number of processing channels or paths may be simplified so that the paths are integrated in a single ΔΣ modulator structure. Each modulator path is routed to a respective ADC (quantizer), each ADC (quantizer) having a respective feedback path including a DAC. Hence for a Time Interleaved ΔΣ modulator, which will have at least two paths, there are at least two quantizers working in parallel, each with a respective feedback path including a DAC. This is more fully explained below.

As explained more fully below, a problem arises with time interleaved ΔΣ modulators, in that with two quantizers operating in parallel paths, there is necessarily a critical path, or so-called delayless path, between the output of one quantizer to the input of the other quantizer. Because of delays arising in paths of the modulators, this may prevent correct operation. One method to eliminate the delayless path problem is to move feedback to the digital domain instead of performing it in the analog domain: see K. S. Lee, Y. Choi and F. Maloberti," Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator," *IEEE ISCAS,* pp. 473-476, 2004 which discloses a four path discrete time TI modulator where, instead of directly generating the 4-consecutive modulator outputs for time slot n, n+1, n+2, n+3 for each of four quantizers, only the n-th time slot modulator output and three predictive terms are generated by the quantizers. The disadvantage of this method is that the

first quantizer requires more comparators than the number of the comparators in the second quantizer.

A second method is to use a sample-and-hold in front of the first quantizer and quantizing the signal when the output of the second DAC is ready [T. C. Caldwell and D. A. Johns," A Time-Interleaved Continuous-Time ΔΣ Modulator with 20-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits,* vol. 41, no. 7, pp. 1578-1588, July 2006.]. This method needs a complicated timing generator, a sample-and-hold and also faster integrators.

The problem therefore remains of overcoming the delayless path problem in a comparatively simple and efficient manner

Summary of the Invention

An embodiment of the invention is based on an error correction technique for overcoming the delayless path issue in time interleaved delta sigma modulators. An error is intentionally induced in the analog domain through the use of the output of one DAC in one feedback path from a first quantizer, which is applied to the input of a second quantizer associated with another feedback path and DAC. Although this output may relate to a previous time sample, the error thus created is then substantially corrected in the digital domain at the outputs of the quantizers, which may effectively eliminate the delayless feedback path.

Accordingly in one embodiment the invention provides a time interleaved delta sigma modulator including:

a plurality of paths for respective time interleaved data channels, which paths comprise a respective feed forward path arrangement including at least one filter stage, a first one of said paths including a first quantizer means being connected to a first feedback path including a first digital to analog conversion means, a second one of said paths including a second quantizer means being connected to a second feedback path including a second digital to analog conversion means, and

the output of the first digital to analog conversion means having a coupling to the input of the second quantizer means, and the output of the first quantizer being coupled to the output of the second quantizer means via a correction means for correcting errors introduced by said coupling.

The invention recognises that errors are created by delays causing timing misalignment, but because input signals vary relatively slowly in comparison to the clocking of the modulator, said coupling may provide the signal value from the first digital to analog conversion means (DAC) obtained at a previous clock interval. This will permit the second quantizer means to perform its quantisation operation. The error induced may then be corrected in the digital domain by means of an error correction circuit coupled between the outputs of the first and second quantizers means. Conveniently, said coupling is a direct coupling, not incorporating any delay or filtering circuits. Conveniently, the correction may be of the differencing form $(1-z^{-1})$, representing the difference between the present time sample, and the previous one.

The present invention is applicable to any number of channels/paths, two or more, in a time interleaved arrangement. Preferably the paths of the modulator share the same filter (integrator/ accumulator) stages in the feed forward arrangement. The invention is applicable to modulators having one or more modulator loops, although the invention is particularly applicable to a single loop arrangement in a time interleaved arrangement. Further the invention is applicable to both DT and CT modulators, although it is particularly useful with CT modulators, as will become clear below.

Brief Description of the Drawings

Preferred embodiments of the invention will now be described by way of example with reference to the accompanying drawings, wherein:

Figure 1 comprises Block diagrams of a) the known DT Single-Loop ΔΣ modulator and b) the known CT Single-Loop ΔΣ modulator r;

Figure 2 is a block diagram of a 3^{rd}-order single-loop DT ΔΣ modulator;

Figure 3 is a block diagram of a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators;

Figure 4 is a waveform diagram showing the outputs of Q1, Q2, DAC1 and DAC2 of Figure 3;

Figure 5 is a block diagram of a first embodiment of the invention, comprising a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators and digital correction network;

Figure 6 are block diagrams of a) a Single-Loop Two-Path DTTI ΔΣ modulator and b) a Single-Loop Two-Path CTTI ΔΣ modulator;

Figure 7 is a block diagram of a second embodiment of the invention comprising a 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator with shared integrators;

Figure 8 shows the signal transfer functions of the 3rd-order Single-Loop Two-Path DTTI and the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulators. of Figures 5 and 7;

Figure 9 shows noise transfer functions of the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator of Figure 7 and a 3rd-order Single-Loop Two-Path DTTI ΔΣ modulator;

Figure 10 is a block diagram of a third embodiment of the invention comprising a 4th-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators; and

Figure 11 is a block diagram of a fourth embodiment of the invention comprising a 3rd-order Single-Loop Four-Path DTTI ΔΣ modulator with shared accumulators.

Description of the Embodiments

CT ΔΣ modulators benefit from operating at higher sampling frequencies in comparison to their DT counterparts. The errors of the sample-and-hold circuit are shaped by the loop filter and the CT ΔΣ modulators have an implicit anti-aliasing filter in their forward signal path. However, CT ΔΣ modulators suffer from several drawbacks: excess loop delay, jitter sensitivity and RC time constant variations.

One way to convert a DT ΔΣ modulator to an equivalent CT ΔΣ modulator is the known impulse-invariant transformation [M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. Berlin: Springer, 2006]. Another is the use of the modified z-transform. The impulse-invariant transformation is employed below. A DT ΔΣ modulator and a CT ΔΣ modulator are shown in Figure 1, and are said to be equivalent when their quantizer inputs are equal at the sampling instants.

$$q(n) = q_c(t)\big|_{t=nT} \quad (1)$$

The procedure for the design of a ΔΣ modulator is based on choosing: the order and architecture of the ΔΣ modulator, the OverSampling Ratio (OSR) and the number of bits for the quantizer. By using the time-interleaving technique and M interconnected parallel modulators that are working concurrently, the effective sampling rate and the OSR become M times the clock rate and the OSR of each modulator respectively; it should be noted with this technique the required resolution can be acquired without increasing the order of the modulator or the number of bits for the quantizer and also without utilizing a state of the art technology.

A 3rd-order single loop two path Discrete-Time Time-Interleaved (DTTI) ΔΣ modulator (below, Figure 3) may be derived from the time domain node equations of a conventional DT ΔΣ modulator, which is shown in Figure 2. In Figure 2, a first accumulator filter 4a obtains an input from combiner 12a, and has a transfer function $az^{-1}(1-z^{-1})^{-1}$, i.e.an accumulation function, with scaling a. Second and third accumulators 4b and 4c with respective transfer functions $bz^{-1}(1-z^{-1})^{-1}$, $cz^{-1}(1-z^{-1})^{-1}$ obtain inputs from respective combiners 12b, 12c. In this Figure, single step quantizer 6 represents the ADC. It is assumed that the DAC 10 in the feedback loop 8 is ideal ($H_{DAC}(z) = 1$). The time domain equations of the modulator are written for two consecutive time slots as (2n)th and (2n+1)th as follows:

$$v_1(2n) = ax(2n-1) - ay(2n-1) + v_1(2n-1) \quad (2.a)$$

$$v_2(2n) = bv_1(2n-1) - by(2n-1) + v_2(2n-1) \quad (2.b)$$

$$v_3(2n) = cv_2(2n-1) - cy(2n-1) + v_3(2n-1) \quad (2.c)$$

$$y(2n) = Q[v_3(2n)] \quad (2.d)$$

and

$$v_1(2n+1) = ax(2n) - ay(2n) + v_1(2n) \quad (3.a)$$

$$v_2(2n+1) = bv_1(2n) - by(2n) + v_2(2n) \quad (3.b)$$

$$v_3(2n+1) = cv_2(2n) - cy(2n) + v_3(2n) \quad (3.c)$$

$$y(2n+1) = Q[v_3(2n+1)] \quad (3.d)$$

where $Q[.]$ represents the quantization function. The input $x(n)$ is distributed between two channels through an input multiplexer which operates at twice the clock frequency of each channel. The input $x(n)$ is relabelled as follows:

$$x_1(n) = x(2n) \quad , \quad x_2(n) = x(2n-1) \quad (4)$$

Similarly, the other nodes of the modulator are relabelled:

$$v_{11}(n) = v_1(2n) \quad , \quad v_{12}(n) = v_1(2n-1) \quad (5.a)$$

$$v_{21}(n) = v_2(2n) \quad , \quad v_{22}(n) = v_2(2n-1) \quad (5.b)$$

$$v_{31}(n) = v_3(2n) \quad , \quad v_{32}(n) = v_3(2n-1) \quad (5.c)$$

$$y_1(n) = y(2n) \quad , \quad y_2(n) = y(2n-1) \quad (5.d)$$

By sharing only one set of accumulators, the input demultiplexer is removed and the input $x(n)$ is shared between channels. Hence equation (4) results in (6) as follows:

$$x_1(n) = x_2(n) = x(n) \quad (6)$$

Equation sets (7) and (8) are derived by substituting equation set (5) and equation (6) into equation sets (2) and (3) respectively as follows:

$$v_{11}(n) = ax(n) - ay_2(n) + v_{12}(n) \quad (7.a)$$

$$v_{21}(n) = bv_{12}(n) - by_2(n) + v_{22}(n) \quad (7.b)$$

$$v_{31}(n) = cv_{22}(n) - cy_2(n) + v_{32}(n) \quad (7.c)$$

and

$$v_{12}(n+1) = ax(n) - ay_1(n) + v_{11}(n) \quad (8.a)$$

$$v_{22}(n+1) = bv_{11}(n) - by_1(n) + v_{21}(n) \quad (8.b)$$

$$v_{32}(n+1) = cv_{21}(n) - cy_1(n) + v_{31}(n) \quad (8.c)$$

Equation set (8) can be rewritten as equation set (9):

$$v_{12}(n) = ax(n-1) - ay_1(n-1) + v_{11}(n-1) \quad (9.a)$$

$$v_{22}(n) = bv_{11}(n-1) - by_1(n-1) + v_{21}(n-1) \quad (9.b)$$

$$v_{32}(n) = cv_{21}(n-1) - cy_1(n-1) + v_{31}(n-1) \quad (9.c)$$

Equation set (10) is derived by further substituting equation set (7) into equation set (8).

$$v_{12}(n) = 2ax(n-1) - a(y_1(n-1) + y_2(n-1)) + v_{12}(n-1) \quad (10.a)$$

$$v_{22}(n) = abx(n-1) + 2bv_{12}(n-1) - by_1(n-1) - b(1+a)y_2(n-1) + v_{22}(n-1) \quad (10.b)$$

$$v_{32}(n) = bcv_{12}(n-1) + 2cv_{22}(n-1) - cy_1(n-1) - c(1+b)y_2(n-1) + v_{32}(n-1) \quad (10.c)$$

The DTTI ΔΣ modulator which is shown in Figure 3 is derived directly from the time domain equation sets (7) and (10). The motive behind sharing one set of accumulator filters in a single feed forward path is to eliminate the instability that can arise due to the DC offset mismatch of the two individual accumulator set based two channel interleaving case. Known DTTI ΔΣ modulators need an input demultiplexer which samples the input signal at the highest clock frequency of the DTTI ΔΣ modulator and distributes it between channels. This fast demultiplexer is a limiting factor for the performance of the DTTI ΔΣ modulators. The architecture shown in Figure 3 does not need an input demultiplexer and the input signal is shared between channels. Removing the input demultiplexer has no effect on the NTF of the DTTI ΔΣ modulator but it causes some notches in its STF at the following frequencies $^{0.5F_{clk}}$, $^{1.5F_{clk}}$, $^{2.5F_{clk}}$, $^{3.5F_{clk}}$, ... which is shown in Figure 10 where $^{F_{clk}}$ is the clock frequency of the DTTI ΔΣ modulator.

Referring to the 3rd-order single-loop two-path DTTI ΔΣ modulator with shared accumulators Figure 3, the two paths comprise a feed forward path arrangement 2 having three accumulator filters 4a, 4b, 4c each with a respective transfer function $az^{-1}(1 - z^{-1})^{-1}$, $bz^{-1}(1 - z^{-1})^{-1,}$ $cz^{-1}(1 - z^{-1})^{-1}$, thus

providing a third order arrangement. Each accumulator is preceded by a respective signal combiner 12a, 12b, 12c. The input signal x(n) is fed to signal combiners 12a, 12b via respective scalers 2, a. The output of accumulator 4a, $v_{12}(n)$ is fed to combiners 12b, 12c via scalers 2, b. The output of accumulator 4b, $v_{22}(n)$ is fed to combiners 12c, 12d via respective scalers 2, c, and the output of accumulator 4c, $v_{32}(n)$ is fed direct to combiner 12d and quantizer Q2.

The output of accumulator 4c is fed direct to a second path quantizer (ADC) Q2 62, and, via signal combiner 12d, to the input of a first path quantizer (ADC) Q1 64. The output of Q2 62 is fed in a second feedback path 8 to DAC 102 and then to subtracting inputs of each signal combiner 12a - 12c, via scaling amplifiers 14, having respective values 1, 1+a, 1+b. The output of Q1 64 is fed in a first feedback path 8 to DAC 101 and then to subtracting inputs of each signal combiner 12a - 12c, via scaling amplifiers 16, having values 1. The output of Q2 62, $y_2(n)$, is fed in a Delayless Path 30 having a scaler c, to a summing input of combiner 12d. The output $y_1(n)$ is fed via a x2 scaler 32 and delay circuit 34, to a signal combiner 36, where it is combined with the output $y_2(n)$, scaled by 2 as at 38 to provide the output signal y(n).

As regards operation of the single path Time Interleaved modulator, it will be noted there is an analog adder 12d in front of quantizer Q1 and the input signal there generated is then applied to the quantizer Q1. In discrete time delta-sigma modulators, quantizers sample this input. As stated in the above formulas, v32(n) and v31(n) are the respective inputs of the second and first quantizers. v32(n) is the output of third accumulator 4c but v31(n) is: (v31(n)=c*v22(n)-c*y2(n)+v32(n)) (We will use an analog adder to generate v31(n) from v32(n), v22(n) and y2(n)). That means that v31(n) is generated by the outputs of the second and third accumulators 4b, 4c and also the output of the second quantizer Q2. The direct relation between v31(n) to y2(n) comprises the “delayless path”.

An issue which makes implementation of the single-path TI ΔΣ modulators impractical is this so-called “delayless feedback path” problem that comes from equation (7.c) above in which $v_{31}(n)$ (the input of quantizer Q1) is directly linked to $y_2(n)$. This means that the output of the second quantizer (Q2) is connected to the input of another quantizer (Q1) without any delay. One

method to eliminate the delayless path is to move this feedback to the digital domain instead of performing it in the analog domain [K. S. Lee, referenced above]. The disadvantage of this method is that the first quantizer (Q1) requires more comparators than the number of the comparators in the second quantizer (Q2) . Another second method is to use a sample-and-hold in front of the first quantizer (Q1) and quantizing the signal when the output of DAC2 is ready [T. C. Caldwell, referenced above]. This method needs a complicated timing generator, a sample-and-hold and also faster accumulators.

An embodiment of the invention, as shown in Figure 5, overcomes the delayless path issue by an error correction technique. We intentionally induce an error in the analog domain through the use of the output of DAC2 102 as shown in Figure 5. The error is substantially corrected in the digital domain which effectively eliminates the delayless feedback path.

To better understand how this works we shall perform a step by step analysis of what happens. A timing diagram as depicted in Figure 4 shows the delay from the outputs of quantizers Q1 and Q2 and their propagation through to the outputs of DAC1 and DAC2 as δ. As a result the output of DAC2 that is sampled at the nth time slot is $y_2(n-1)$ where we should have had $y_2(n)$. To overcome this inconsistency we look at the input and output of Q1, as depicted in Figure 4. Quantizer Q1 quantizes the signal $v_{31}(n)$ as follows:

$$y_1(n) = Q[v_{31}(n)] \quad (11)$$

Equation (12) is derived by substituting (7.c) into (11):

$$y_1(n) = Q[cv_{22}(n) - cy_2(n) + v_{32}(n)] \quad (12)$$

The output of DAC2 is used in (13) and equation (12) is rewritten as:

$$y_1(n) = Q[cv_{22}(n) - cy_2(n-1) + v_{32}(n)] + cy_2(n-1) - cy_2(n) \quad (13)$$

The output of Q1 is called $y_{1e}(n)$ in (14):

$$y_1(n) = y_{1e}(n) + cy_2(n-1) - cy_2(n) \quad (14)$$

$$error = c\Delta y = c(y_2(n) - y_2(n-1)) \quad (15)$$

$$Y_1(z) = Y_{1e}(z) - c(1 - z^{-1})Y_2(z) \quad (16)$$

As appears from (14), $y_{1e}(n)$ (the output of Q1) needs to be corrected before it is applied to the input of DAC1; otherwise it causes instability in the modulator as it will change the modulators dynamics by increasing its order. A first order differencer block $(1-z^{-1})$ is used to perform this correction as described in (16). Equation (16) illustrates the point that Q1 is able to quantize its input without any additional circuit in the analog domain by merely using the output of DAC2. The differencer block $(1-z^{-1})$ only corrects the error in equation (14) and it has no effect on the quantization error or the signal.

The 3rd order single-loop two path DTTI ΔΣ modulator forming a first embodiment of the invention is shown in Figure 5. Referring to Figure 5, feed forward path arrangement comprises three accumulator filters 4a, 4b, 4c each with a respective transfer function $az^{-1}(1 - z^{-1})^{-1}$, $bz^{-1}(1 - z^{-1})^{-1}$, $cz^{-1}(1 - z^{-1})^{-1}$, thus providing a third order arrangement. Each accumulator is preceded by a respective signal combiner 12a, 12b, 12c. The input signal x(n) is fed to signal combiners 12a, 12b via scalers 2, a. The output of accumulator 4a, $v_{12}(n)$ is fed to combiners 12b, 12c via scalers 2, b. The output of accumulator 4b, $v_{22}(n)$ is fed to combiners 12c, 12d via scalers 2, c, and the output of accumulator 4c, $v_{32}(n)$ is fed direct to combiner 12d and quantizer Q2.

The output of accumulator 4c is fed direct to second path quantizer Q2 62, and, via signal combiner 12d, to the input of first path quantizer Q1 64. The output of Q2 is fed in a second feedback path 8 to DAC 102 and then to subtracting inputs of each signal combiner 12a-12d, via scaling amplifiers 14 having values1, 1+a, 1+b, and c. It will be noted there is a direct coupling 31 from the output of DAC 102 to the input of Q1 64. The output of Q1 is fed in a first feedback path 8 to DAC 101 and then to subtracting inputs of each signal combiner 12a-12c, via scaling amplifiers 1. The output of Q2, $y_2(n)$ is fed via an error correction circuit 50 having the transfer function $c(1-z^{-1})$ to a subtracting input of a signal combiner 51, where it is combined with the output of Q1, $y_{1e}(n)$,

to give output $y_1(n)$. The output $y_1(n)$ is fed via a x2 scaler 52 and delay circuit 54, to a signal combiner 56, were it is combined in combiner 56 with the output $y_2(n)$, scaled by 2 as at 58.

The significant advantages and disadvantages of the Lee paper, referenced above, the Caldwell paper, referenced above, and the present invention are summarized in the Table below:

Method	Comparator count for Q1	Comparator count for Q1	Advantage	Disadvantage
Lee	48	16	Additonal analog blocks not needed	More comparators for Q1 required
Caldwell	16	16	Fewer comparators	Sample/Hold, complex timing generator and fast integrators required
Invention	32	16	Additonal analog blocks not needed	More comparators required for Q1 than Caldwell

The signal swing at the input of quantizer Q1 is increased in the first and the present methods because scaling is not an option and it will lead to loss of Signal-to-Noise Ratio (SNR), the first and the present methods require 48 and 32 comparators for quantizer Q1 respectively, in comparison to the second method which requires 16 comparators as depicted in Table I.

The CTTI ΔΣ modulator equivalent of the DTTI ΔΣ modulator of Figure 5 can be obtained in three steps as follows: The first step is to determine the loop filters of the DTTI ΔΣ modulator. In this design, the DTTI ΔΣ modulator has six loop filters ($FF_{1d}(z)$, $FF_{2d}(z)$, $H_{1d}(z)$, $H_{2d}(z)$, $H_{3d}(z)$ and $H_{4d}(z)$) These loop filters for the DTTI ΔΣ modulator are as depicted in Figure 6(a). The second step is to convert the DT loop filters into equivalent CT loop filters by using the impulse-invariant transformation. The equivalent CTTI ΔΣ modulator is shown in Figure 6(b) where the DT loop filters of Figure 6(a) have been replaced with the equivalent CT loop filters $FF_{1c}(s)$, $FF_{2c}(s)$, $H_{1c}(s)$, $H_{2c}(s)$, $H_{3c}(s)$ and $H_{4c}(s)$.

The third step is to convert the modulator of Figure 6(b) into a 3rd order CTTI ΔΣ modulator as shown in Figure 7. To overcome the excess-loop delay issue, two additional feedback paths from the outputs of DAC1 and DAC2 to the inputs of each quantizer (Q1 and Q2) are used. The loop filters of the modulator as shown in Figure 7 can be found and matched to those in Figure 6(b) to determine the coefficients f_{1c}, f_{2c}, f_{3c}, f_{4c}, f_{5c}, f_{6c}, f_{7c}, f_{8c}, f_{9c} and f_{10c} in Figure 7.

Referring to the 3rd-order Single-Loop Two-Path CTTI ΔΣ modulator with shared integrators of Figure 7, three sets of integrator filters 3a, 3b, 3c, in a feed forward path arrangement have their inputs provided by signal combiners 12a, 12b, 12c, combiners 12b and 12c each comprising two combiners in series. Each integrator filter has a transfer function of the form 1/Ts, with respective scaling coefficients a, b, c. The input signal x(t) is fed to signal combiners 12a, 12b, 12c via scaling amplifiers having respective values 2, a, 2/3(ab). The output of integrator 3a, $v_{12}(t)$ is fed to combiners 12b, 12c via respective scaler amplifiers 2, b, the output of integrator 4b, $v_{22}(t)$ is fed to combiners 12c, 12d via scaling amplifiers 2, c, and the output of integrator 4c, $v_{32}(n)$ is fed direct to combiners 12d, 12e.

The output of integrator 3c is fed via signal combiner 12d to first path quantizer (ADC) Q1 64, and via signal combiner 12e to the input of second quantizer (ADC) Q2 62. The output of Q2 62 is fed in a second feedback path 8 to DAC 92 and then to subtracting inputs of each signal combiner 12a - 12e, via respective scaling amplifiers f_{c2}, f_{c4}, f_{c6}, f_{c10}, f_{c8}. It will be noted there is a direct coupling 31 from the output of DAC 92 to the input of Q1 64. The output of Q1 64, modified as at 51, is fed in a first feedback path 8 to DAC 94 and then to subtracting inputs of each signal combiner 12a - 12e, via scaling amplifiers f_{c1}, f_{34}, f_{c5}, f_{c9}, f_{c7}. The output of Q2, $y_2(n)$ is fed via an error correction circuit 50 having the transfer function $c(1-z^{-1})$ to a subtracting input of a signal combiner 51, where it is combined with the output of Q1, $y_{1e}(n)$, to give output $y_1(n)$. The output $y_1(n)$ is fed via a x2 scaler 52 and delay circuit 54, to a signal combiner 56, were it is combined in combiner 56 with the output $y_2(n)$, scaled by 2 as at 58 to give the final output y(n).

It will be noted that the outputs of DAC 92, 94 are each fed to each of quantizers Q1, Q2, via signal combiners 12d, 12e, to overcome excess loop delay.

The OSR of the overall modulator shown in Figure 7 from $x(t)$ to $y(n)$ is 16 and has been designed to operate at 320MHz clock frequency for a 10MHz signal bandwidth. The resolution of Q1 and Q2 are 5bits and 4bits respectively. After correcting the error as stated by equation (21) in the digital domain, $y_1(n)$ will be 4bits in length. Therefore, DAC1 and DAC2 both require 4bit DACs. To

simplify the design, generally, the coefficient c scaling the first order differencer $(1-z^{-1})$ in the digital domain should be chosen to be a number which is a power of two. This choice results in replacing the potentially complicated multiplier with a simple hard-wired shift.

The STFs of the DTTI and CTTI ΔΣ modulators are plotted in Figure 8. Since the $NTF_{1d}(z)$ and $NTF_{2d}(z)$ both have an identical amplitude, only the $NTF_{1d}(z)$ is plotted in Figure 9 and is compared to the NTF of the conventional DT ΔΣ modulator of Figure 4.

Referring now to Figure 10, which shows a third embodiment of the invention comprising a 4th-order Single-Loop Two-Path DTTI ΔΣ modulator with shared accumulators, similar parts to those of previous embodiments, in particular Figure 5, are denoted by the same reference numeral. In contrast to Figure 5, Figure 10 comprises a 4th order single-path DTTI ΔΣ modulator, having four accumulator filter stages 4a, 4b, 4c, 4f. Accumulator 4f has a transfer function $dz^{-1}(1 - z^{-1})^{-1}$, and has an input fed by combiner 12f, which receives a feedback signal from second path DAC 102, scaled by (1+c), a feedback signal from first path DAC 101, and the output from accumulator 4c, $v_{32}(n)$. The output of accumulator 4f, $v_{42}(n)$, is applied direct to the input of quantizer Q2 62, and to signal combiner 12g, where it is combined with the output $v_{32}(n)$, scaled by d, and by the feedback signal from DAC 102, scaled by d, to provide a resultant signal $v_{41}(n)$ to the input of quantizer Q1 64. The output of quantizer Q1 is combined at 51 with the output of Q2, digitally corrected in correction circuit 50d by a factor $d(1-z^{-1})$.

Referring now to Figure 11, which shows a fourth embodiment of the invention comprising a 3rd-order Single-Loop Four-Path DTTI ΔΣ modulator with shared accumulators, similar parts to those of previous embodiments, in particular Figure 5, are denoted by the same reference numeral. Figure 10 comprises a 3rd order four-path DTTI ΔΣ modulator, having three accumulator stages 4a, 4b, 4c in a feed forward path arrangement. Four quantizers of respective first, second, third and fourth paths are employed operating in parallel, Q1 64, Q2 62, Q3 66, Q4 68. Quantizer Q1 64 accepts an input from signal combiner 70, Quantizer Q2 62 accepts an input from signal combiner 72,

Quantizer Q3 66 accepts an input from signal combiner 74, and Quantizer Q4 68 accepts an input direct from accumulator 4c.

The output of quantizer Q4 68 is applied direct to signal combiner 56 via a x4 scaler, which provides the final output y(n), and to a fourth feedback path which include a DAC 104. The output of quantizer Q3 66 is applied to a signal combiner 71, and thence to a third feedback path which include a DAC 103. The output of quantizer Q2 62 is applied to a signal combiner 73, and thence to a second feedback path which include a DAC 102. The output of quantizer Q1 64 is applied to a signal combiner 75, and thence to a first feedback path which include a DAC 101.

The input signal x(n) is split into four parallel paths and is applied to combiners 12a, 12b, 12c, 12d, via respective scalers 4, 6a, 4ab, abc. The output of accumulator 4a, $v_{14}(n)$, is applied to combiners 12b, 72, 70 via respective scalers 4, bc, 3bc. The output of accumulator 4b, $v_{24}(n)$, is applied to combiners 12c, 74, 72, 70 via respective scalers 4, c, 2c, 3c. The output of accumulator 4c, $v_{34}(n)$, is applied directly to combiners 74, 72, 70.

The output of quantizer Q4 68 is applied to signal combiner 56, scaled by a factor of 4, and via digital correction circuit 80, to signal combiners 71, 73, 75, via respective scalers c, c(b+1), c(b(a+2) +1). The output of quantizer Q3 66 is applied to signal combiner 71, the output of 71 being scaled by a factor of 4, and applied to combiner 56 via a delay circuit z^{-1}. The output of 71 is also applied via digital correction circuit 82 to combiners 73, 75 via respective scalers c, c(b+1). The output of quantizer Q2 62 is applied to signal combiner 73, the output of 73 being scaled by a factor of 4, and applied to combiner 56 via two delay circuits z^{-1}. The output of 73 is also applied via digital correction circuit 84 to combiner 75 via respective scaler c. The output of quantizer Q1 64 is applied to signal combiner 75, the output of 75 being scaled by a factor of 4, and applied to combiner 56 via three delay circuits z^{-1}. The output of 73 is also applied via digital correction circuit 84 to combiner 75 via respective scaler c.

The feedback signal in the first path from DAC 101 is applied directly to combiners 12a, 12b, 12c. The feedback signal in the second path from DAC 102 is applied to combiners 12a, 12b, 12c, 70, via respective scalers (none), 1+a, 1+b, c. The feedback signal in the third path from DAC 103 is applied to combiners 12a, 12b, 12c, 70, 72 via respective scalers (none), 1+2a, 1+ab+2b,

c(b+1), c. The feedback signal in the fourth path from DAC 104 is applied to combiners 12a, 12b, 12c, 70, 72, 74 via respective scalers (none), 1+3a, 1+3ab+3b, c+2bc+abc, c(b+1), c. It will be noted there are direct couplings from the outputs of DACs 102 -104 to quantizers Q1-Q3.

In the single path modulator embodiments above, sharing the integrators/ accumulators between the input paths makes them robust to path mismatch effects compared to the typical Time-Interleaved (TI) modulators which have individual integrators in all paths. Practical issues like finite dc gain and bandwidth of the opamps, the DAC mismatches and offsets of the quantizers may not introduce any noticeable degradation in performance. For an OverSampling Ratio (OSR) of 16 and a clock frequency of 320MHz with all practical non-idealities the maximum SNDR of this modulator may be 78dB.

The present invention at least in embodiments provides a mechanism for resolving the delayless feedback path issue in TI ΔΣ modulators with reduced comparator count.

CLAIMS

1. A time interleaved delta sigma modulator including:

a plurality of paths for respective time interleaved data channels, said paths comprising a feed forward path arrangement, including at least one filter stage, a first one of said paths including a first quantizer means being connected to a first feedback path including a first digital to analog conversion means, a second one of said paths including a second quantizer means being connected to a second feedback path including a second digital to analog conversion means, and

the output of the first digital to analog conversion means having a coupling to the input of the second quantizer means, and the output of the first quantizer means being coupled to the output of the second quantizer means via a correction means for correcting errors introduced by said coupling.

2. A time interleaved sigma delta modulator, according to claim 1, wherein the modulator is a discrete time modulator.

3. A time interleaved sigma delta modulator, according to claim 2, wherein said feed forward path arrangement has at least first and second accumulator stages, and the output of the second stage is coupled to the input of the second quantizer means, and the outputs of both the first and second stages are coupled to the input of the first quantizer means.

4. A time interleaved sigma delta modulator, according to claim 2, wherein said feed forward path arrangement has at least first, second and third accumulator stages, wherein an input signal is fed to the first and second stages, an output from the first stage is fed to the second and third stages, an output from the second stage is fed to the third stage and said first quantizer means, and an output from the third stage is fed to said first quantizer means, and directly or via further accumulator stages to said second quantizer means.

5. A time interleaved sigma delta modulator, according to claim 3 or 4, wherein said feed forward path arrangement has at least first, second and third accumulator stages, wherein said first feedback path and said second feedback path are each coupled to each of said first, second and third accumulator stages.

6. A time interleaved sigma delta modulator, according to claim 1, wherein the modulator is a continuous time modulator.

7. A time interleaved sigma delta modulator, according to claim 6, wherein said feed forward path arrangement has at least first and second integrator stages, and the output of the second stage is coupled to the input of the second quantizer means, and the outputs of both the first and second stages are coupled to the input of the first quantizer means.

8. A time interleaved sigma delta modulator, according to claim 6, wherein said feed forward path arrangement has at least first, second and third integrator stages, wherein an input signal is fed to the first, second and third stages, an output from the first integrator stage is fed to the second stage and to the third stage, an output from the second integrator stage is fed to the third stage and said first quantizer means, and an output from the third integrator stage is fed to said first quantizer means, and directly or via further integrator stages to said second quantizer means.

9. A time interleaved sigma delta modulator, according to claim 7 or 8, wherein said feed forward path arrangement has at least first, second and third integrator stages, wherein said first feedback path and said second feedback path are each coupled to each of said first, second and third integrator stages.

10. A time interleaved sigma delta modulator, according to any of claims 7 to 9, wherein said first feedback path and said second feedback path are each coupled to each of the inputs of said first and second quantizer means.

11. A time interleaved sigma delta modulator, according to any preceding claim, wherein said correction means is a digital differencing circuit having a transfer function of the form $(1-z^{-1})$.

12. A time interleaved sigma delta modulator, according to claim 11, wherein a coefficient scaling said transfer function of the form $(1-z^{-1})$ comprises a number which is a power of two.

13. A time interleaved sigma delta modulator, according to any preceding claim, wherein the modulator has at least three paths with respective first, second and third quantizer means, said third quantizer means being connected to a third feedback path including a third digital to analog conversion means, the output of the third digital to analog conversion means

having a further coupling to the inputs of the first and second quantizer means, and the output of the third quantizer means being coupled to the outputs of the first and second quantizer means via respective further correction means for correcting errors introduced by said further coupling.

5

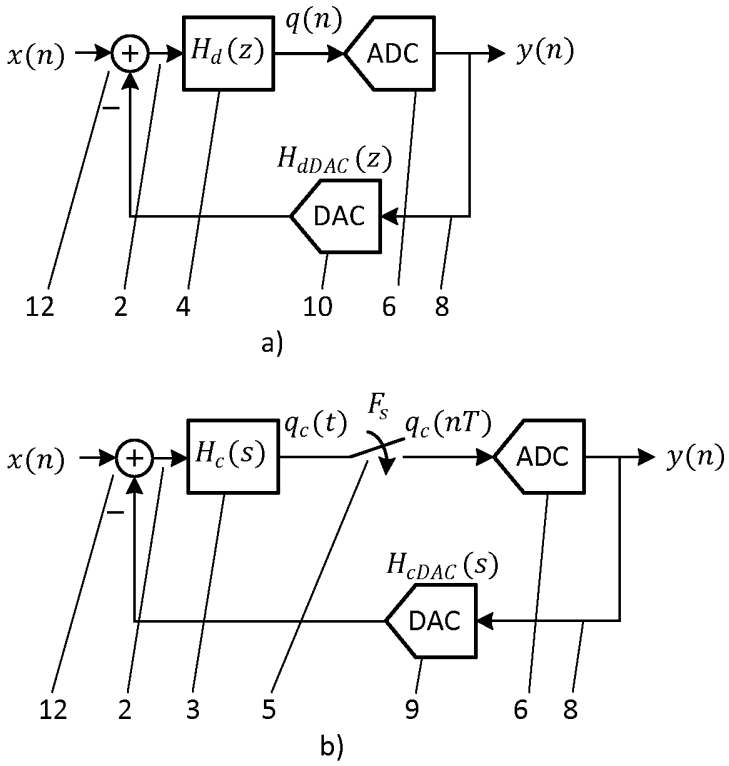


Figure 1: Block diagrams of a) The DT ΔΣ modulator and b) The CT ΔΣ modulator.

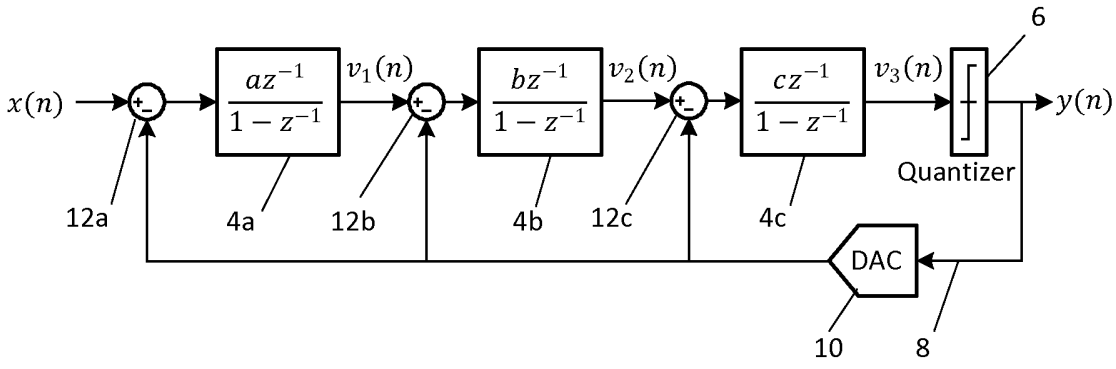


Figure 2: Block diagram of a 3rd-order single-loop DT ΔΣ modulator.

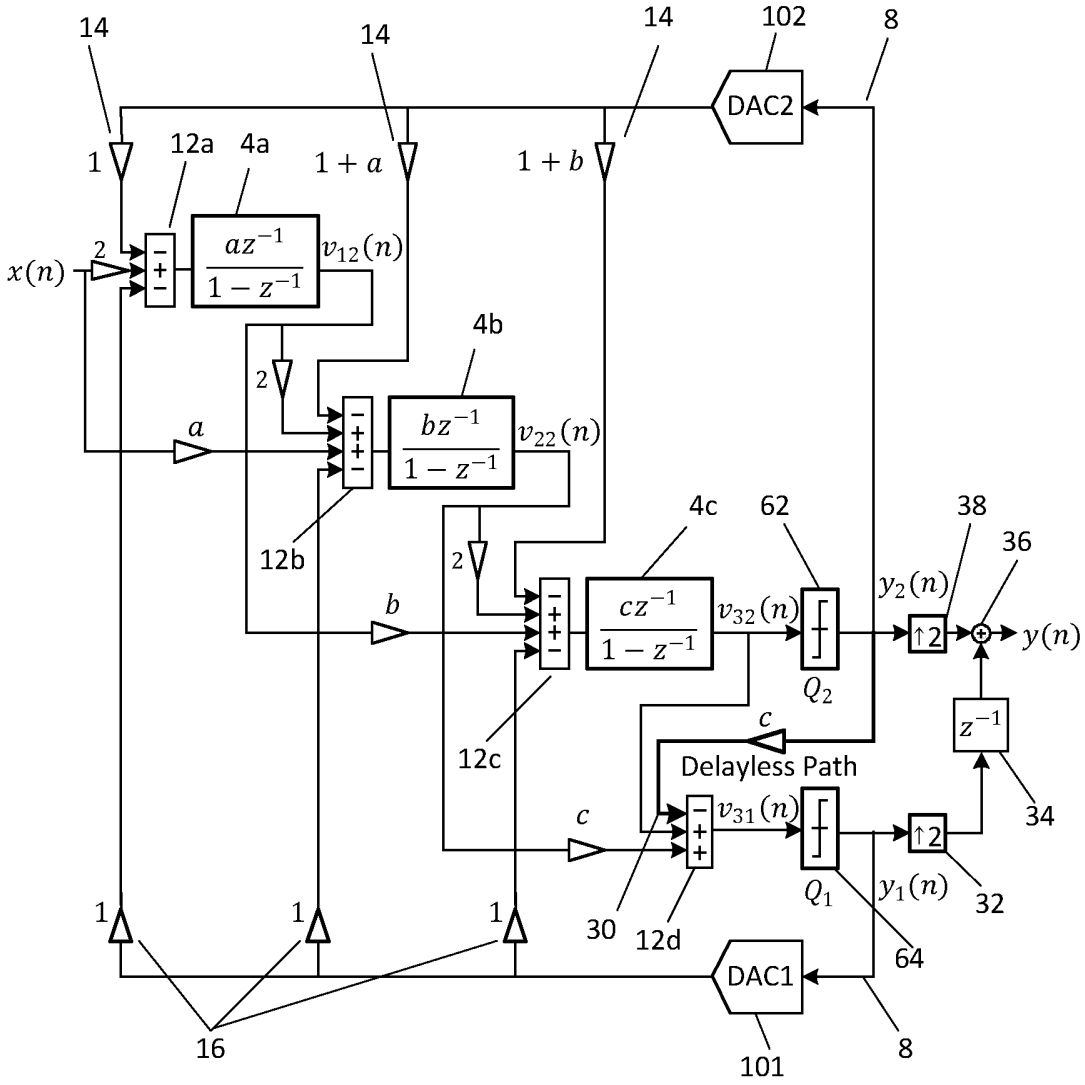


Figure 3: A 3rd-order single-loop two path DTTI ΔΣ modulator.

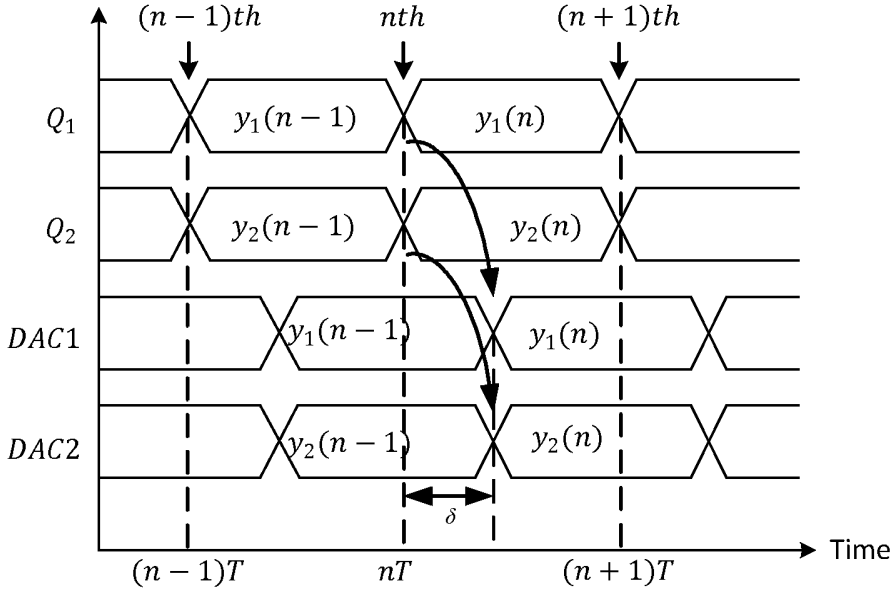


Figure 4: The outputs of Q1, Q2, DAC1 and DAC2.

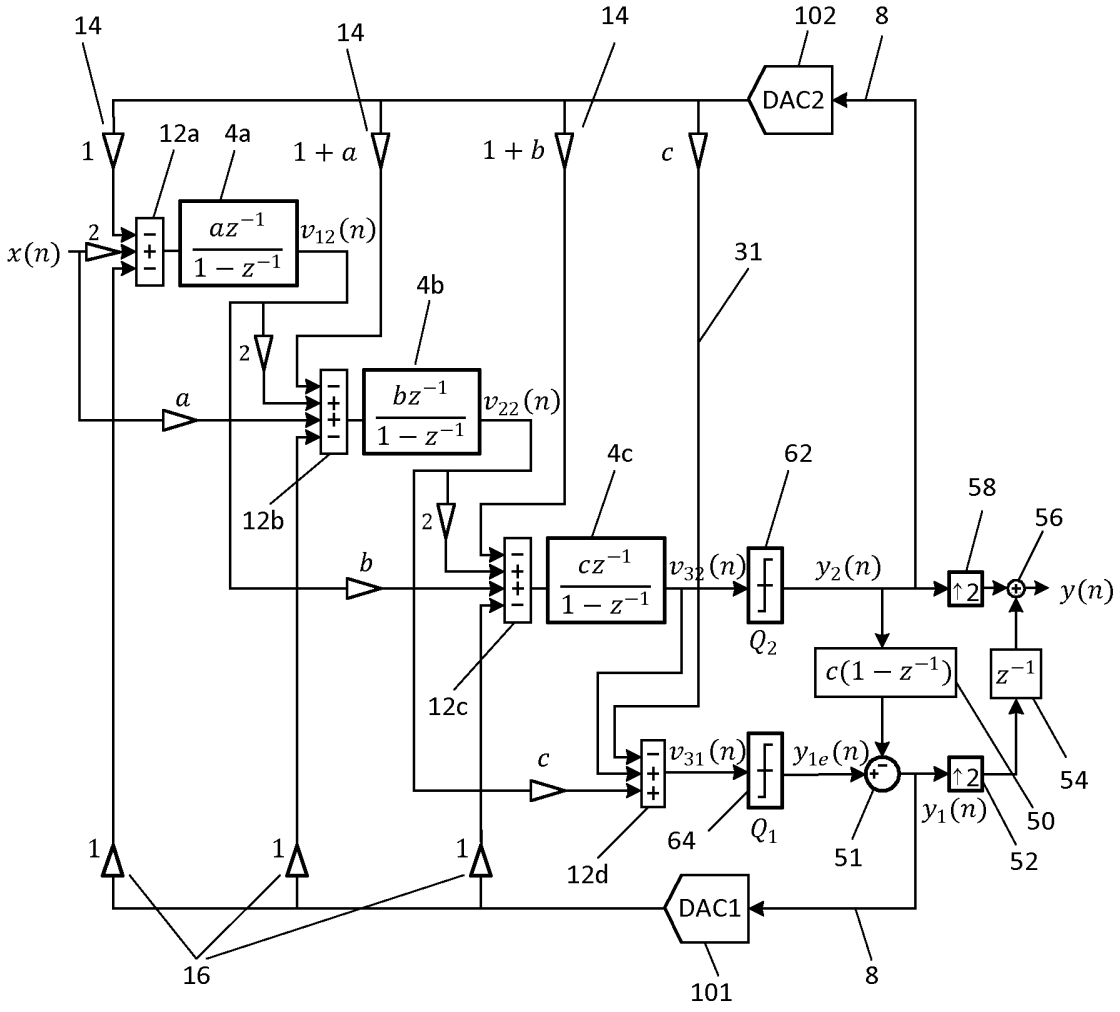


Figure 5: A 3rd-order single-loop two path DTTI ΔΣ modulator

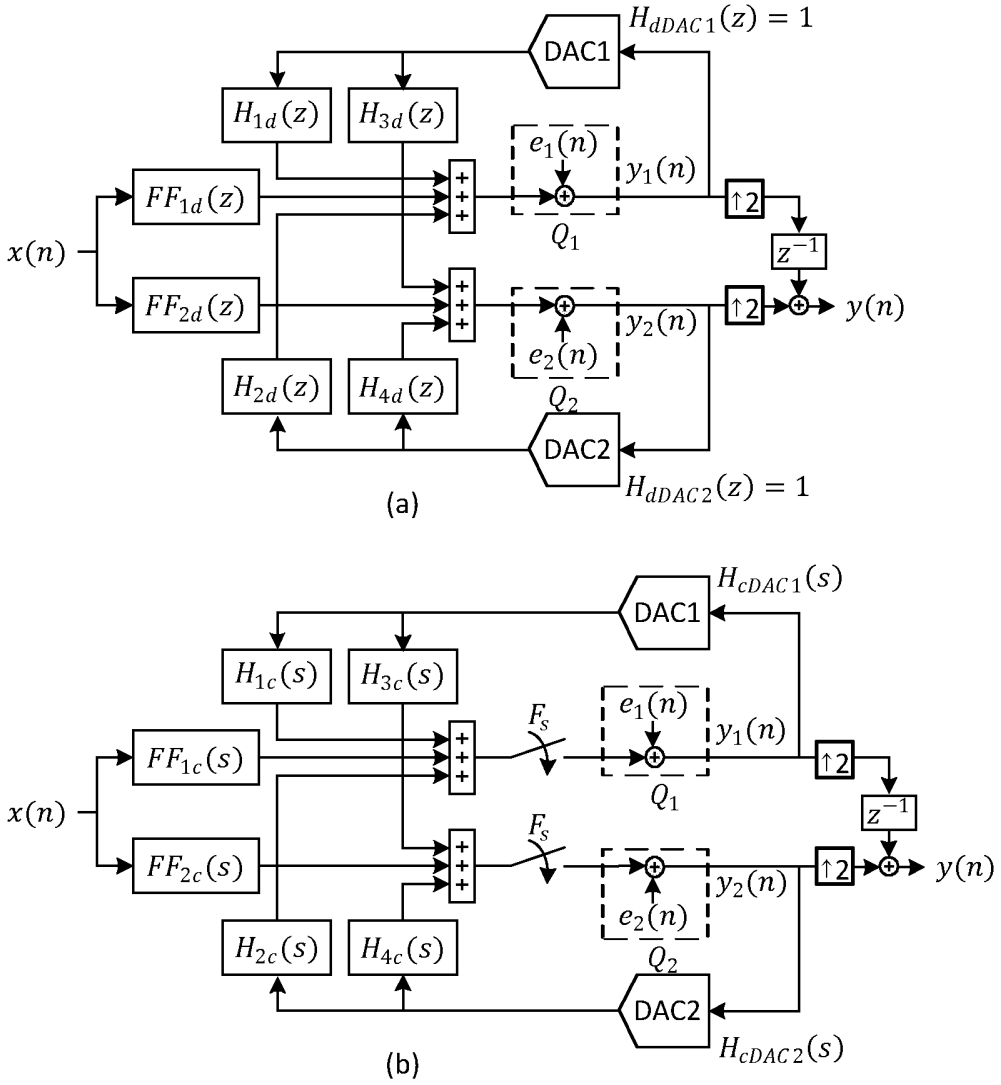


Figure 6: Block diagrams of a) a DTTI ΔΣ modulator and b) a CTTI ΔΣ modulator.

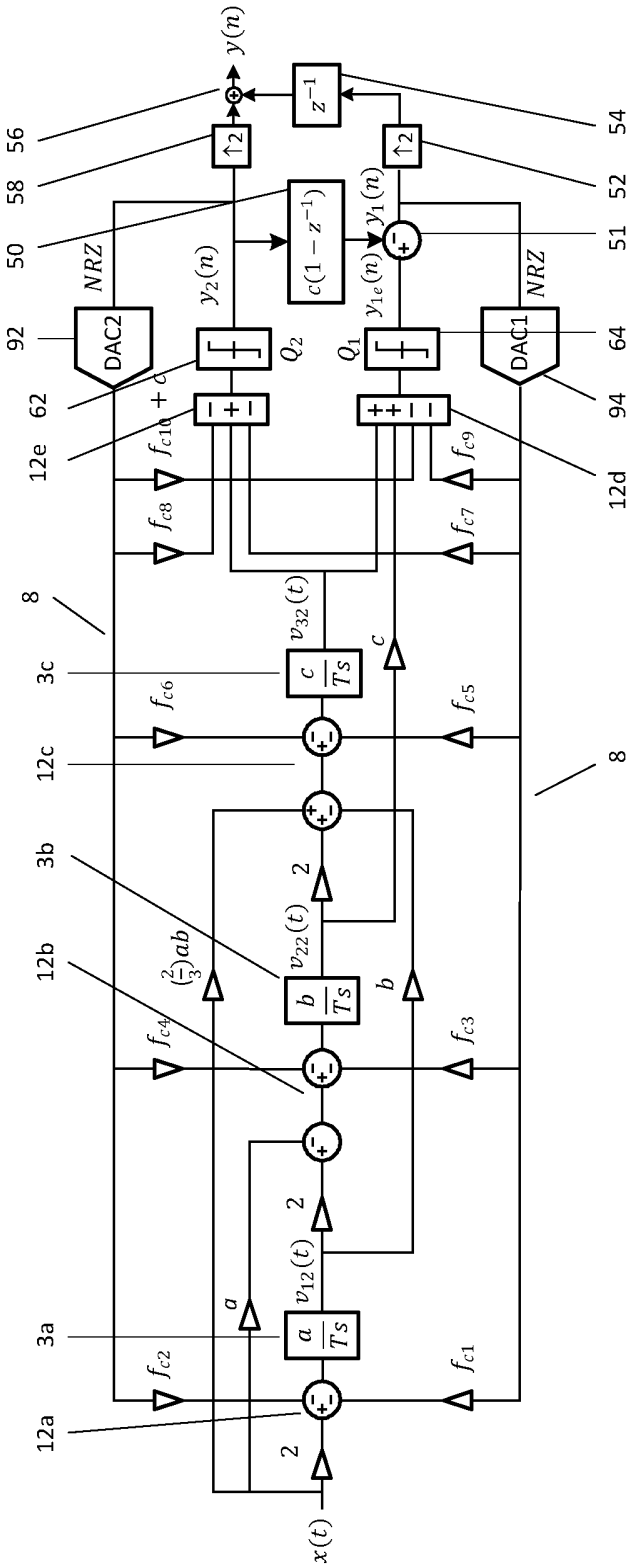


Figure 7: A 3rd-order single-loop two path CTTI ΔΣ modulator.

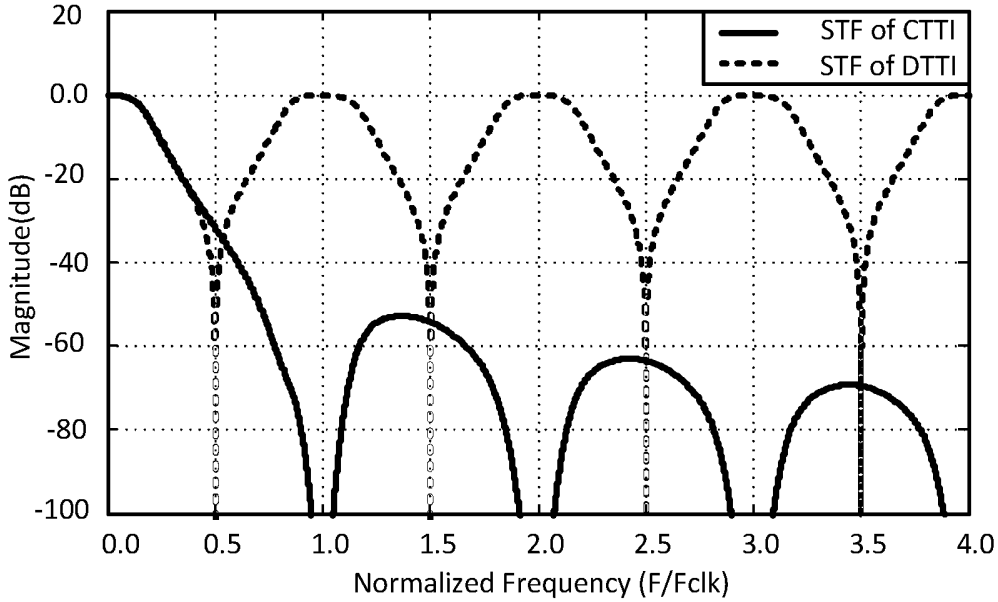


Figure 8: Signal transfer functions of DTTI and CTTI ΔΣ modulators.

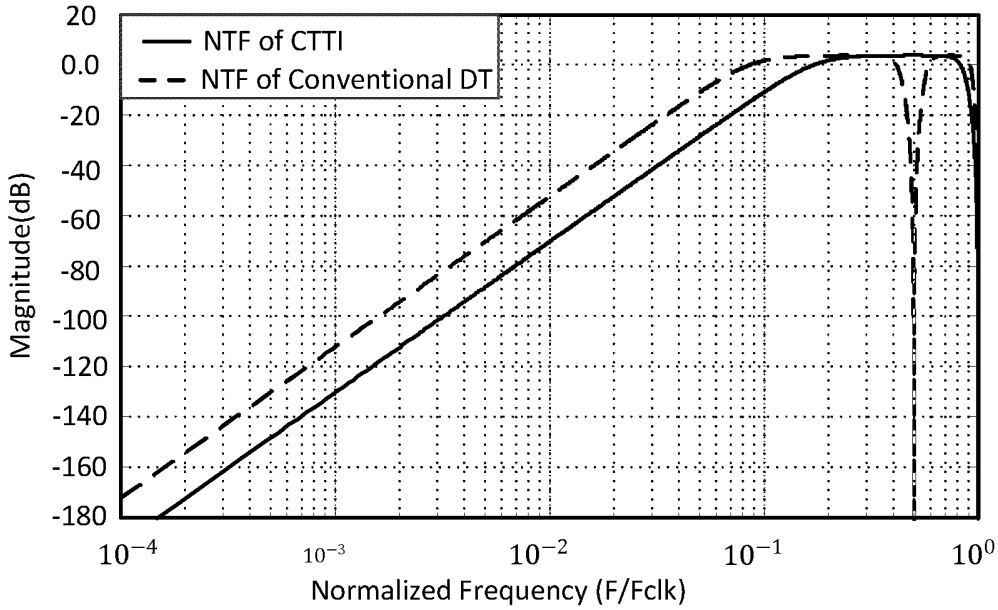


Figure 9: Noise transfer functions of the CTTI and the DT ΔΣ modulators.

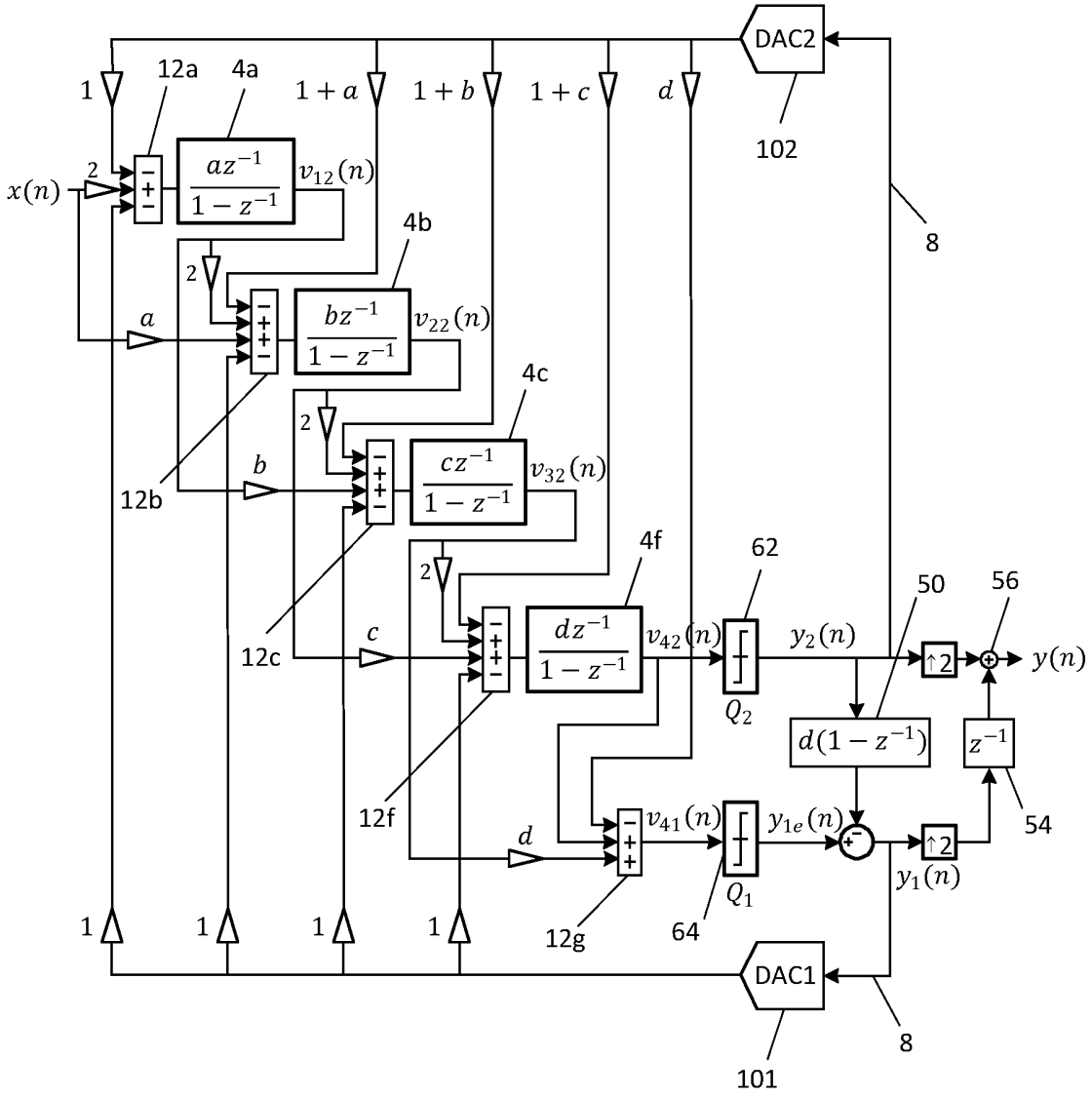


Figure 10: A 4th-Order Two-Path Discrete-Time Time-Interleaved Delta Sigma Modulator

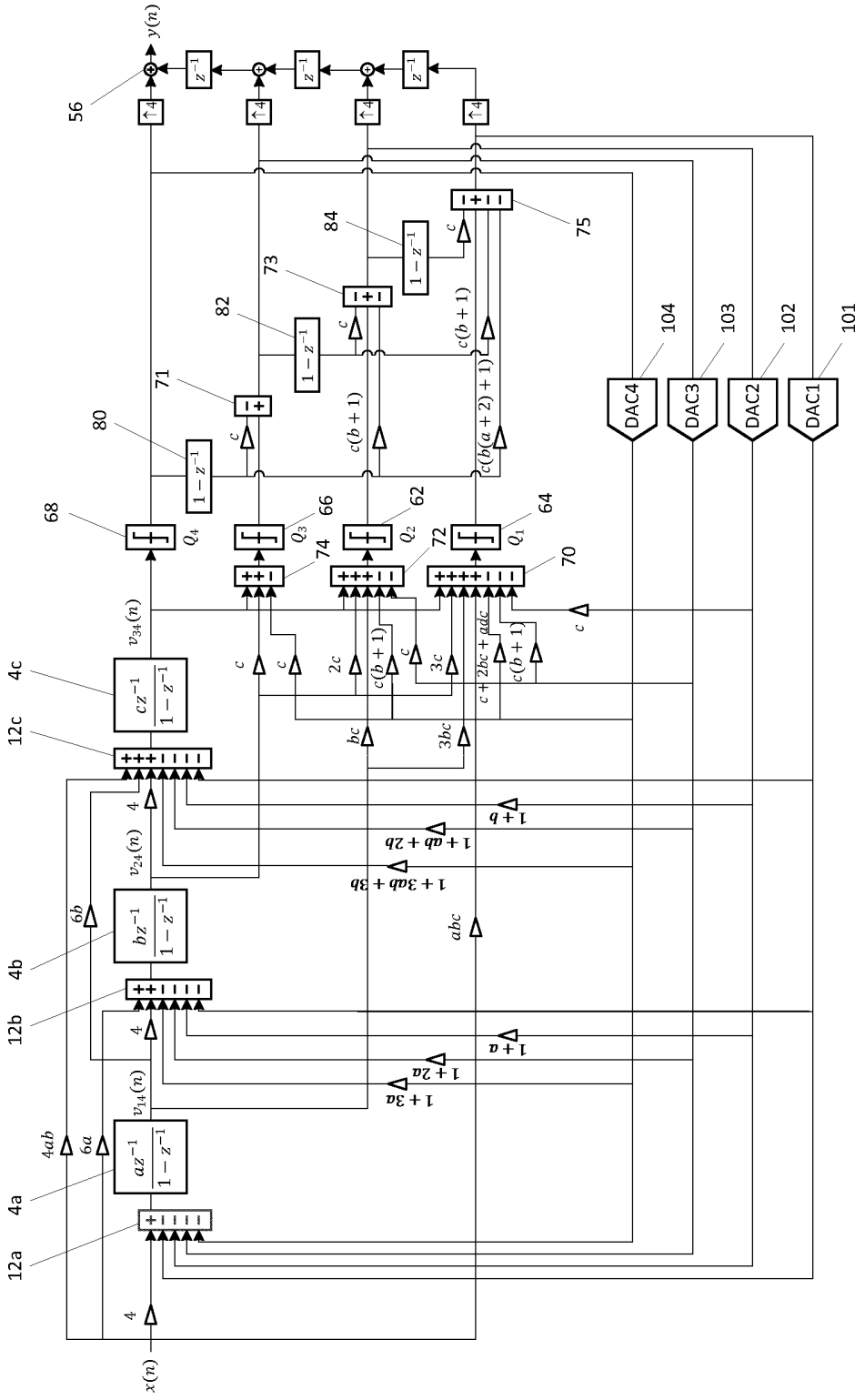


Figure 11: A 3rd-Order four-Path Discrete-Time Time-Interleaved Delta Sigma Modulator.

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/056425

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M3/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KYE-SHIN LEE ET AL: "Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator", ANALOG INTEGRATED CIRCUITS AND SIGNAL PROCESSING, KLUWER ACADEMIC PUBLISHERS, BO, vol. 43, no. 3, 1 June 2005 (2005-06-01), pages 225-235, XP019204021, ISSN: 1573-1979, DOI: 10.1007/S10470-005-1604-3 cited in the application the whole document ----- -/--	1-13

[X] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 2015	02/07/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Galardi, Leonardo

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2015/056425

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CALDWELL T C ET AL: "A time-interleaved continuous-time /spl Delta//spl Sigma/ modulator with 20MHz signal bandwidth", SOLID-STATE CIRCUITS CONFERENCE, 2005. ESSCIRC 2005. PROCEEDINGS OF THE 31ST EUROPEAN, IEEE, PISCATAWAY, NJ, USA, 12 September 2005 (2005-09-12), pages 447-450, XP010854998, DOI: 10.1109/ESSCIR.2005.1541656 ISBN: 978-0-7803-9205-2 cited in the application the whole document -----	1-13