Low power, reduced complexity filtering and improved tracking accuracy for GNSS

Sevket Cetinsel

Faculty of Science and Technology

UNIVERSITY OF WESTMINSTER

Low Power, Reduced Complexity Filtering and Improved Tracking Accuracy for GNSS

Sevket CETINSEL

A thesis submitted in partial fulfilment of the requirements of the University of Westminster for the degree of Doctor of Philosophy

May 2014

Authors Declaration

I hereby certify that the research work presented in this thesis is, to the best of my knowledge and belief, original except as referenced in the thesis. I hereby declare that I have not submitted this material, either completely or in part, for a degree at this or any other institution.

Abstract

This thesis addresses the power consumption problems resulting from the advent of multiple GNSS satellite systems which create the need for receivers supporting multi-frequency, multi-constellation GNSS systems. Such a multi-mode receiver requires a substantial amount of signal processing power which translates to increased hardware complexity and higher power dissipation which reduces the battery life of a mobile platform. During the course of the work undertaken, a power analysis tool was developed in order to be able to estimate the hardware utilisation as well as the power consumption of a digital system. By using the power estimation tool developed, it was established that most of the power was dissipated after the Analog to Digital Converter (ADC) by the filters associated with the decimation process. The power dissipation and the hardware complexity of the decimator can be reduced substantially by using a minimum-phase Infinite Impulse Response (IIR) filter. For Global Positioning System (GPS) civilian signals, the use of IIR filters does not deleteriously affect the positional accuracy. However, in the case where an IIR filter was deployed in a GLObalnaya NAvigatsionnaya Sputnikovaya Sistema (GLONASS) receiver, the pseudorange measurements of the receiver varied by up to 200 metres. The work undertaken proposes various methods that overcomes the pseudorange measurement variation and reports on the results that are on par with linear-phase Finite Impulse Response (FIR) filters. The work also proposes a modified tracking loop that is capable of tracking very low Doppler frequencies without decreasing the tracking performance.

Acknowledgements

I would like to express my sincere gratitude to my supervisors Prof. Izzet Kale and Prof. Richard C. S. Morling for giving me the opportunity to carry out this work. Without their support, guidance and patience since the beginning to all the way to the very end my PhD thesis wouldn't be possible.

Once again, I would like to thank to my supervisors Prof. Izzet Kale and Prof. Richard C. S. Morling for offering me part time employment at the university which alleviated financial difficulties.

Also, I would like to take this opportunity to thank all the lecturers and other members of staff at the Department of Engineering where I have spent my last 9 years since I joined as a Foundation year student. They provided me with constant encouragement and motivation and valuable support that kept me pursuing further.

I also would like to thank Elgin Candoleta for her excellent friendship, continuous support and understanding.

Lastly but most importantly, I would like to thank to my parents for their faith, support and guidance that have kept me on the right path. Without my parents, I would have never reached this far.

Table of Contents

List of Figures

List of Tables

List of Acronyms

ADVRG	Applied DSP and VLSI Research Group
AGC	Automatic Gain Control
ADC	Analog to Digital Converter
ALP	Almost Linear Phase
ARNS	Aeronautical Radio Navigation Services
bps	bits per second
BOC	Binary Offset Carrier
BPSK	Binary Phase Shift Keying
C/A	Coarse/Acquisition
CS	Commercial Service
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CORDIC	COordinate Rotation DIgital Computer
CT	Continuous-Time
$\Sigma\Delta$	Sigma-Delta
DLL	Delay Locked Loop
DMAC	Difference Multiply Accumulate
DSP	Digital Signal Processor

DT	Discrete-Time
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FLL	Frequency Locked Loop
FPGA	Field Programmable Gate Array
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HOW	Hand Over Word
Hz	Hertz
IF	Intermediate Frequency
IFFT	Inverse Fast Fourier Transform
IIR	Infinite Impulse Response
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LUT	Look Up Table
MAC	Multiply Accumulate
MEO	Medium Earth Orbit
NAVSTAR	NAVigation System with Time and Ranging
NCO	Numerically Controlled Oscillator
ND	Numerator-Denominator
OS	Open Service

OSR	Oversampling Ratio
PDM	Pulse Density Modulation
PLL	Phase Locked Loop
PRN	Pseudo-Random Noise
PRS	Public Regulated Service
PSD	Power Spectral Density
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTL	Register Transfer Level
SaR	Search and Rescue
Sat-Nav	Satellite Navigation
SoL	Safety-of-Life
TDA	Time Delay and Accumulate
TDL	Tapped Delay Line
TLM	Telemetry
TMBOC	Time Multiplexed Binary Offset Carrier
TSMC	Taiwan Semiconductor Manufacturing Company
US	United States
VHSIC	Very High Speed Integrated Circuit
VHDL	VHSIC Hardware Description Language

Chapter 1

Introduction

In recent years the usage of Global Navigation Satellite System (GNSS) systems has become commonplace and receivers are being deployed in more and more everyday devices [2]. Also the advent of multiple GNSS satellite systems create the need for receivers to support multi-frequency, multi-constellation GNSS systems in order to provide the best solution possible [3–5]. This multi-mode receiver requires a substantial amount of signal processing power which translates to increased hardware complexity as well as higher power dissipation which reduces the battery life of a mobile platform. The research reported here investigates where most of the power is dissipated and proposes alternative methods to minimize the power dissipation without degrading the performance of the overall GNSS receiver.

The work presented in this thesis utilised a real-time development platform that was designed and implemented at the University of Westminster by the Applied DSP and

VLSI Research Group (ADVRG) that provided real-time GNSS signal access from the GNSS aerial on the roof of Cavendish Campus.

All the real-time experiments were implemented using a Xilinx Virtex 5 ML506 Field Programmable Gate Array (FPGA) development board together with a custom Radio Frequency (RF) Front-End that was developed within the ADVRG research group.

1.1 Research Aims

The aim of the research undertaken can be summarised as follows:

- The added functionality required to process multiple GNSS standards increases the computational load of the receiver. This requirement increases the power consumption and so there is a need to offset this reducing the overall power consumption. Therefore the first aim was to identify the sub-sections that consume most power.

- The subsequent aim was to investigate more efficient methods of implementing the most power-hungry parts and assess their applicability and suitability for GNSS receivers.

- Not all alternative methods may be suitable for the GNSS receiver. So the next aim was to investigate the performance of the alternative methods. If satisfactory, then it would be possible to have a GNSS receiver with reduced complexity and lower power.

1.2 Original Contributions

The main contributions resulting from this research can be summarised as:

- A Doppler frequency related problem has been identified in the tracking loop in the GNSS receiver. Existing solution is studied and an improved solution has been proposed. The proposed solution improved the tracking performance with fixed-point arithmetic but with floating-point accuracy and it also has less complexity than the existing solutions available [6].

- A power estimation tool was developed where a user can define the hardware complexity of a design in terms of required design blocks and the proposed tool estimates its power dissipation as well as the hardware complexity. By using this developed power analysis tool, the designer can estimate how much power will be consumed and how much hardware resources will be required for a given digital design without having to design the circuit at the detailed Register Transfer Level (RTL).

- It was established that most power efficient decimator used for the incoming multi-standard GNSS signal to do processing was the minimum-phase Infinite Impulse Response (IIR) filter of decimation combination 6 by 2 by 2 for the overall decimation ratio 24.

- It has been established that using a minimum-phase IIR filter does not deteriorate positioning accuracy for Global Positioning System (GPS).

- Non-linear phase IIR filters can now be used in Frequency Division Multiple Access (FDMA) systems such as GLObalnaya NAvigatsionnaya Sputnikovaya Sistema (GLONASS). Previously it was not possible without degrading the positioning performance of the overall system. The proposed method greatly overcomes this problem where the distortion of GLONASS pseudorange can be compensated by negligible computational load.

1.3 Author's Publications

- Cetinsel, S.; Morling, R. C. S.; Kale, I., "Nonlinear Phase Filtering Effects on GNSS Receiver Positioning Accuracy",Journal of Navigation 2014, in preparation

- Cetinsel, S.; Morling, R. C. S.; Kale, I., "Nonlinear Phase Filtering Effects on GNSS Receiver Positioning Accuracy",To be presented at 7th ESA Workshop on Satellite Navigation Technologies and European Workshop on GNSS Signals and Signal Processing (NAVITEC), 3-5 December 2014.

- Cetinsel, S.; Morling, R. C. S.; Kale, I., "A comparative study of a low Doppler shift in a carrier tracking loop for GPS", 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp.220-223, 2-5 Dec. 2012.

- Cetinsel, S.; Morling, R. C. S.; Kale, I., "An FPGA based decimation filter processor design for real-time continuous-time Σ - Δ modulator performance measurement and evaluation", 20th European Conference on Circuit Theory and Design (ECCTD), pp.397-400, 29-31 Aug. 2011.

1.4 Thesis outline

The aims and original contributions of this work are presented in Chapter 1.

Chapter 2 provides an introduction to GNSS and explains some basic concepts of positioning. It also outlines various GNSS systems that exist today and summarises their signal characteristics.

Chapter 3 begins by giving an overview of various GPS L1 acquisition methods in which it explains how a signal is processed in order to determine if there are any satellites visible to the receiver. Then it continues with the tracking process where a novel tracking processor is proposed that overcomes the problems related to Doppler frequency.

Chapter 4 describes the development of the power estimation tool that has been developed in order to estimate the power dissipation as well as the area utilisation of a digital circuit without designing the actual circuit.

Chapter 5 describes the development of alternative decimation and filter techniques for the GNSS receivers with their characteristics, their hardware implementation, power consumption and area utilisation.

Chapter 6 explains the experiments carried out with the filters designed in Chapter 5 and shows the positioning measurements using the designed filters. It also reports on the performance evaluation of pseudorange measurements for GPS and GLONASS using linear-phase Finite Impulse Response (FIR) and minimum-phase IIR filters.

Chapter 7 explains the low frequency implementation details of the filters that were used in the decimation and filtering chain of the GNSS receiver. It shows how the structure converted into hardware that makes it power as well as resource usage efficient.

Chapter 8 presents the summary of the thesis, the conclusions drawn from this research and proposes future research directions.

Chapter 2

Introduction to GNSS

This chapter provides an introduction to research on GNSS and explains some basic concept of positioning with GNSS and various GNSS systems' signal characteristics.

GNSS is a generic term for Satellite Navigation (Sat-Nav) Systems that provide geo-spatial positioning with global coverage [7]. It allows portable electronic receivers to determine their location in terms of longitude, latitude and altitude [8]. Currently, only the United States (US) NAVigation System with Time and Ranging (NAVSTAR) GPS and Russia's GLONASS are the positioning services that are fully operational with global coverage [9]. However, there are other GNSS systems that are currently under development. These are GALILEO and BeiDou/COMPASS and they are planned to be fully operational by 2020 [10, 11].

GNSS satellites transmit information from space that are located at Medium Earth Orbit (MEO) level. However most of the receivers currently available on the market are using only the L1 band of GPS. The forthcoming GNSS system, GALILEO, will

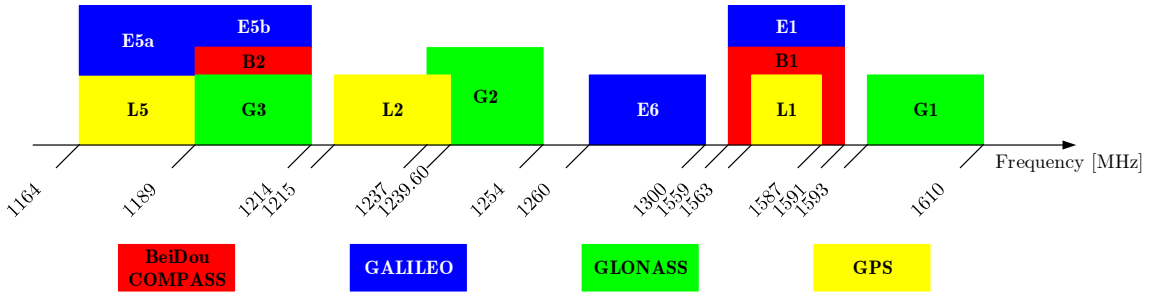


FIGURE 2.1: GNSS Frequency Plan

provide better accuracy and performance compared with GPS and GLONASS [12]. However, a new generation of GNSS receivers will be required to handle these multiple systems and achieve the improved accuracy.

Figure 2.1 shows the GNSS spectral allocation at the present time. It can be seen from Figure 2.1 that most of the individual bands for each link overlap. There are two reasons for this: firstly the frequency band is overcrowded and, secondly transmitting different constellations in the same frequency band reduces the extra hardware requirements for receiving the RF signal. However, this creates an additional problem: providing signal structures that can co-exist without undue mutual interference. The signal structure is an important issue and the following sections give the details of the signal structure of different GNSS systems.

It is necessary to start by explaining some basic common characteristics of the GNSS signal.

2.1 Navigation Data

The navigation data contains the information about the satellites. The data that creates the navigation message is uploaded to the satellites from the ground station. Each GNSS band and system have their own specific bit rate and therefore more detail is given in the sections which describe specific GNSS bands.

Navigation data provides information about the satellite that is necessary to calculate the precise location of the satellites that are visible to the receiver. Figure 2.2 shows the overall navigation structure that is transmitted on GPS L1 C/A channel with a bit rate of 50 bps. The navigation data is composed of 25 1500-bit frames in which each frame contains 5 subframes of 300-bits. One subframe has 10 words and each word is 30 bits long. For further details regarding the exact contents of the navigation message please refer to [1].

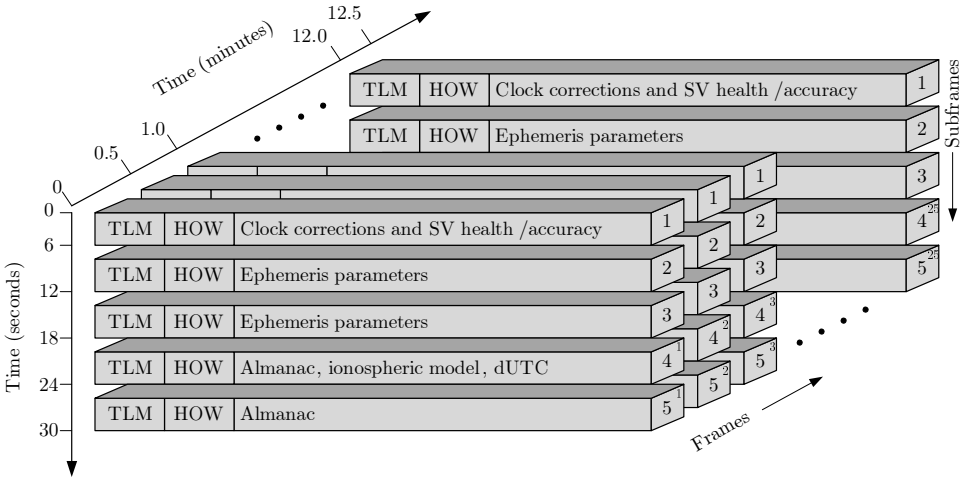


FIGURE 2.2: GPS Navigation Structure

2.2 Spreading Code

GPS and Galileo use a spread-spectrum technique called Code Division Multiple Access (CDMA) [13, 14] whereas GLONASS uses FDMA. The main reason for using spread-spectrum is that it provides robustness against interference and jamming [15]. Also for CDMA type of multiple access all the satellite transmits at a particular frequency that have same carrier frequency but each satellite is distinguished by their unique Pseudo-Random Noise (PRN) code [16]. These PRN codes are generated by using Linear Feedback Shift Registers (LFSRs) with specific register outputs are modulo two summed and fed back to the input of the shift register.

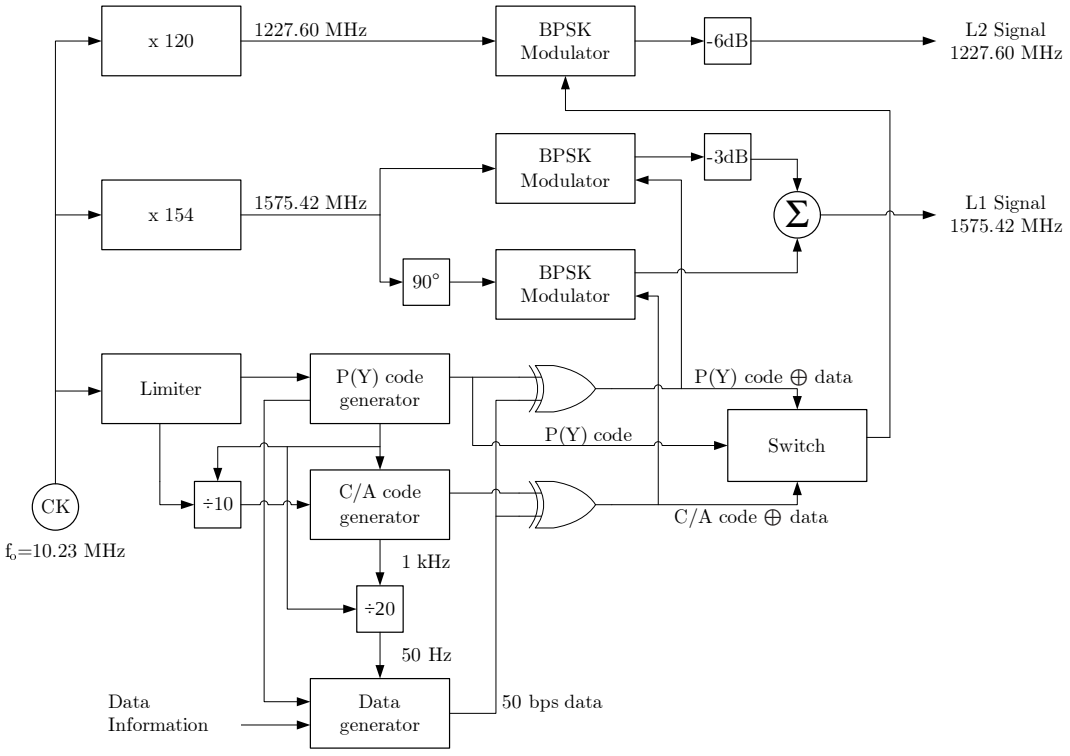


FIGURE 2.3: GPS Signal Generation in a satellite [1].

Figure 2.3 shows how a GPS signal is generated in a satellite. The GPS signal is generated as follows: First the 10.23 MHz fundamental base clock is generated and

it is multiplied with 154 and 120 in order to generate L1 frequency of 1575.42 MHz and L2 frequency of 1227.60 MHz respectively. Then the P(Y) code and C/A code are generated which each of them are modulo-2 summed with the 50 bps data. Finally for L2 Signal, only P(Y) code and for L1 signal, C/A code mixed with 3 dB attenuated P(Y) code and each are individually Binary Phase Shift Keying (BPSK) modulated and transmitted at their corresponding L bands. C/A code is a pseudorandom binary sequence that is used to generate a unique PRN code for each GPS satellite. For GPS L1 band the C/A code is 1023-bit long binary sequence and has a chipping rate of 1.023 Msps. P(Y) code is $6.1871 \text{x} 10^{12}$ bits long and it is encrypted to prevent unauthorised access. The navigation message is then modulated on top of these codes. This type of modulation is a CDMA and makes it possible for the receiver to receive data from multiple satellites that transmit at same frequency.

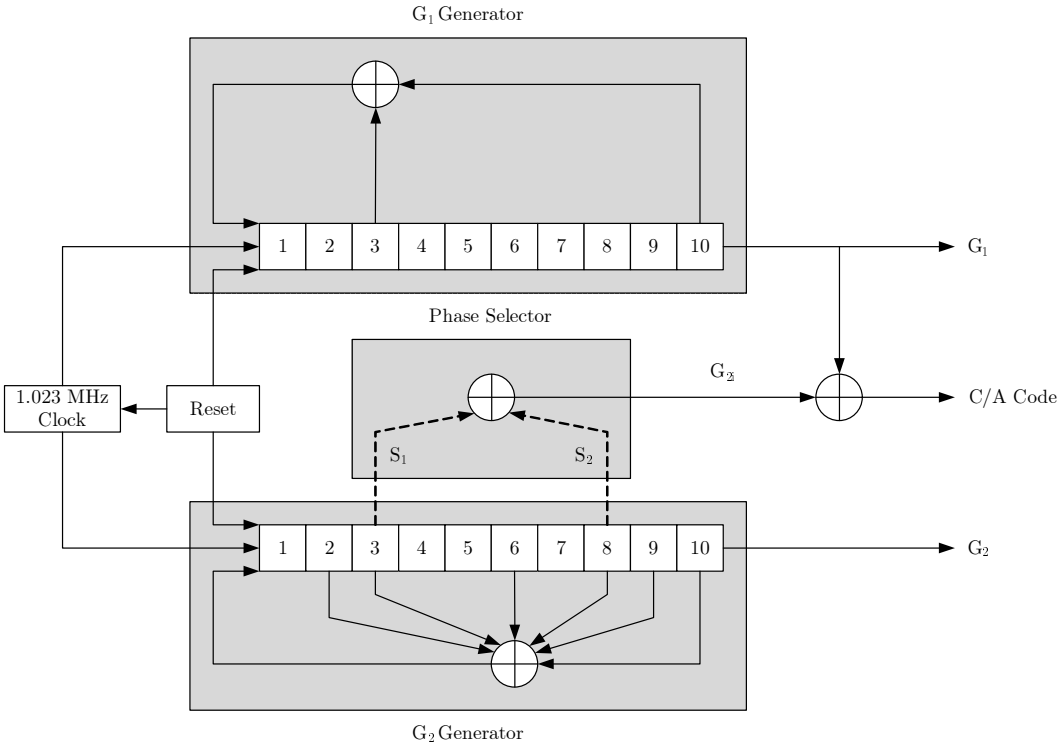


FIGURE 2.4: GPS C/A Code Generator

Figure 2.4 shows how to generate a PRN code for Coarse/Acquisition (C/A) code based on the specification given [17]

2.3 GPS Signal Structure

GPS has been operational since 1995 [18]. Each GPS satellite transmits two radio frequencies in the L-Band; L1 and L2 that are fully operational. This section gives the details the structure of a GPS signal.

2.3.1 GPS L1 Signal

GPS L1 is the band that is most widely used and it transmits two types of signal. One is open for public use and it is called the C/A code and it is transmitted as the Quadrature-Phase of the GPS L1 signal. There is also a P(Y) Code that is encrypted and it is used by the US military which has better positioning accuracy then the C/A code. This P(Y) code is transmitted as the in-phase component of the signal. Recently there have been plans to change the signal characteristics in order to improve position accuracy and enable interoperability between other GNSS systems.

The GPS L1 signal transmits at 1575.42 MHz with the C/A and P(Y) codes modulated using BPSK type of modulation technique. Under the modernisation plan, in the future the GPS L1 C/A code will be replaced with L1C code and it will use variants of Binary Offset Carrier (BOC) modulation [19]. The navigation message will also change. Currently this is transmitting with the C/A code which does not have any

error correction but the upcoming L1C code will transmit the navigation message that is Forward Error Correction (FEC) encoded using convolution encoder. Further details are summarised in Table 2.1.

Table 2.1: Detailed GPS L1 Signal Properties

GPS					
Frequency Band	L1				
Access Technique	CDMA				
Carrier [MHz]	1575.42				
Service Name	C/A	L1C		P(Y) Code	M-Code
Signal Component	Data	Data	Pilot	Data	N.A.
Modulation	BPSK	TMBOC(6,1,1/11)		BPSK	BOCsin(10,5)
Sub-carrier [MHz]	–	1.023	1.023 & 6.138	–	10.23
Chipping Rate [Mcps]	1.023	1.023		10.23	5.115
Primary PRN Code Length	1023	10230		6.19×10^{12}	N.A.
Code Family	Gold Codes	Weil Codes		Combination of short-cycling of M-sequences	N.A.
Secondary PRN Code Length	–	–	1800	–	N.A.
Data rate	50 bps / 50 sps	50 bps / 100 sps	–	50 bps / 50 sps	N.A.

2.3.2 GPS L2 Signal

GPS L2 signal transmits at 1227.60 MHz and it was initially designed for military use along with the P(Y) Code in order to improve position accuracy by comparing the ionospheric effects on L1 and L2 bands in order to remove the error introduced by the ionosphere. Under the GPS modernisation plan the new GPS L2 band will be structured as follows:

The signal is modulated using BPSK modulation. The military encrypted P(Y) code is modulated in the in-phase channel while two signals: L2CM and L2CL are modulated in the quadrature channel. These are L2 Civilian Moderate and L2 Civilian Long respectively. The L2CM code has a code length of 10230 chips and the L2CL code has a code length of 767250. These two signals are multiplexed chip by chip. The L2CM channel contains the navigation message data but the L2CL channel does not contain any data instead it is used as a pilot channel. Further details are given in Table 2.2 [20].

Table 2.2: Detailed GPS L2 Signal Properties

GPS				
Frequency Band	L2			
Access Technique	CDMA			
Carrier [MHz]	1227.60			
Service Name	L2CM	L2CL	P(Y) Code	M-Code
Signal Component	Data	Pilot	Data	N.A.
Modulation	BPSK	BPSK	BPSK	BOCsin(10,5)
Sub-carrier [MHz]	–	–	–	10.23
Chipping Rate [Mcps]	0.5115	0.5115	10.23	5.115
Primary PRN Code Length	10230	767250	6.19×10^{12}	N.A.
Code Family	M-sequence for a maxima polynomial of degree 27		Combination of short-cycling of M-sequences	N.A.
Secondary PRN Code Length	–	–	–	N.A.
Data rate	IIF: 50 bps / 50 sps IIRM: 25 bps / 50 sps	–	50 bps / 50 sps	N.A.

2.3.3 GPS L5 Signal

The GPS L5 signal is another GPS signal that is to be used as a Safety-of-Life (SoL) signal for aircraft and maritime navigation. GPS L5 signal has started transmitting in satellite blocks GPS IIF. Table 2.3 summarises some details of the GPS L5 signal structure.

Table 2.3: Detailed GPS L5 Signal Properties

GPS		
Frequency Band	L5	
Access Technique	CDMA	
Carrier [MHz]	1176.45	
Service Name	L5I	L5Q
Signal Component	Data	Pilot
Modulation	BPSK	BPSK
Sub-carrier [MHz]	–	–
Chipping Rate [Mcps]	10.23	10.23
Primary PRN Code Length	10230	10230
Code Family	Combination of short-cycling of M-sequences	
Secondary PRN Code Length	10	20
Data rate	50 bps / 100 sps	–

2.4 Galileo Signal Structure

Galileo is Europe's initiative for GNSS system that is designed to be interoperable with other GNSS systems such as GPS and GLONASS [21]. It will provide various different services which are listed below [22–24]:

- **Open Service (OS):** Open service is aimed for mass market that is free to the user providing positioning informaion with accuracy to 1 metre.
- **Safety-of-Life (SoL):** The Safety of Life service aims to update the user in case of any problem occurs with any satellite that affects the performance.
- **Commercial Service (CS):** An encrypted service that is designed to achieve centimetre accuracy for commercial use with improved performance compared to open service.
- **Public Regulated Service (PRS):** PRS is restricted to only government-authorised users that require high level of service. The service is designed to have higher robustness against interference and jamming.
- **Search and Rescue (SaR):** A worldwide service to help distress signals to a rescue points.

2.4.1 Galileo E1 Signal

Galileo E1 signal is an open service signal that transmits on the same frequency as GPS L1 band. Galileo E1 band uses BOC modulation in order to split the spectrum into two side lobes. Table 2.4 summarises some details of the Galileo E1 signal structure.

2.4.2 Galileo E5 Signal

Galileo E5 signal is divided into two sub-bands E5a and E5b. They are both open access signals that each carry a data channel and a pilot channel.

TABLE 2.4: Detailed Galileo E1 Signal Properties

Galileo			
Frequency Band	E1		
Access Technique	CDMA		
Carrier [MHz]	1575.42		
Service Name	E1 OS		PRS
Signal Component	Data	Pilot	Data
Modulation	CBOC(6,1,1/11)		BOCcos(15,2.5)
Sub-carrier [MHz]	1.023 & 6.138		15.345
Chipping Rate [Mcps]	1.023	1.023	2.5575
Primary PRN Code Length	4092	4092	N.A.
Code Family	Random Codes		N.A.
Secondary PRN Code Length	–	25	N.A.
Data rate	250 sps	–	N.A.

E5a signal transmits unencrypted ranging codes as well as navigation data. The transmitted data though E5a signal is used to support navigation and timing functions.

E5b signal also transmits unencrypted ranging codes and navigation data. Like E5a it also contains unencrypted data as well as commercial data that are encrypted. Table 2.5 summarises some details of the Galileo E5 signal structure.

2.4.3 Galileo E6 Signal

Galileo E6 signal contains two CS and one PRS bands. The CS band has one one data and one pilot signal components where the PRS has one data channel. Table 2.6 summarises some details of the Galileo E6 signal structure.

TABLE 2.5: Detailed Galileo E5 Signal Properties

Galileo				
Frequency Band	E5			
Access Technique	CDMA			
Carrier [MHz]	1191.795			
Service Name	E5a		E5b	
Signal Component	Data	Pilot	Data	Pilot
Modulation	AltBOC(15,10)			
Sub-carrier [MHz]	15.345			
Chipping Rate [Mcps]	10.23			
Primary PRN Code Length	10230			
Code Family	Combination of short-cycling of M-sequences			
Secondary PRN Code Length	20	100	4	100
Data rate	50 sps	–	250 sps	–

TABLE 2.6: Detailed Galileo E6 Signal Properties

Galileo			
Frequency Band	E6		
Access Technique	CDMA		
Carrier [MHz]	1278.75		
Service Name	E6 CS		PRS
Signal Component	Data	Pilot	Data
Modulation	BPSK	BPSK	BOCcos(10,5)
Sub-carrier [MHz]	–	–	10.23
Chipping Rate [Mcps]	5.115 MHz		
Primary PRN Code Length	5115	5115	N.A.
Code Family	Memory Codes		N.A.
Secondary PRN Code Length	–	100	N.A.
Data rate	1000 sps	–	N.A.

2.5 GLONASS Signal Structure

GLONASS is the second oldest GNSS system that was initial created by the Soviet Union but later it is developed under the Russian Federation [25, 26]. Although other

GNSS systems use CDMA type of access technique GLONASS is the only system which uses FDMA. It uses 24 satellites in orbit. Unlike other GNSS systems in which they use CDMA access technique and each satellite transmits on the same frequency , GLONASS uses FDMA access technique that uses different frequency for different the satellites. This section gives the details the structure of the GLONASS bands.

2.5.1 GLONASS L1 Signal

GLONASS L1 band is open for public use. It uses 15-channel FDMA access technique ranging from 1598.0625 MHz to 1605.375 MHz with 0.511 MHz intervals. Since there is only 15 frequency channels assigned to 24 satellites some satellites have to transmit at the same frequency. This is achieved by assigning two same transmit frequency to the satellites that are opposite side of the planet. Therefore the interference is minimal. Under the GNSS modernization programme the Russian government have decided to switch to CDMA access technique however at the time of writing there wasn't any details available yet. Table 2.7 summarises some details of the GLONASS L1 signal structure.

2.5.2 GLONASS L2 Signal

GLONASS L2 band also uses 15-channel FDMA access technique that ranges from 1242.9375 MHz to 1248.625 MHz with 0.511 MHz intervals. Similar to GLONASS L1 band since there is only 15 frequency channels assigned to 24 satellites some satellites

Table 2.7: Detailed GLONASS L1 Signal Properties

GLONASS		
Frequency Band	L1	
Access Technique	FDMA	
Carrier [MHz]	(1598.0625 – 1605.375) ± 0.511	
Service Name	C/A	P-Code
Signal Component	Data	Data
Modulation	BPSK	BPSK
Sub-carrier [MHz]	–	–
Chipping Rate [Mcps]	0.511	5.11
Primary PRN Code Length	511	N.A.
Code Family	Combination of short-cycling of M-sequences	
Secondary PRN Code Length	–	N.A.
Data rate	50 bps	N.A.

transmit at the same frequency. Table 2.8 summarises some details of the GLONASS L2 signal structure.

Table 2.8: Detailed GLONASS L2 Signal Properties

GLONASS		
Frequency Band	L2	
Access Technique	FDMA	
Carrier [MHz]	(1242.9375 – 1248.625) ± 0.511	
Service Name	C/A	P-Code
Signal Component	Data	Data
Modulation	BPSK	BPSK
Sub-carrier [MHz]	–	–
Chipping Rate [Mcps]	0.511	5.11
Primary PRN Code Length	511	N.A.
Code Family	Combination of short-cycling of M-sequences	
Secondary PRN Code Length	–	N.A.
Data rate	50 bps	N.A.

2.5.3 GLONASS L3 Signal

GLONASS L3 band also uses FDMA access technique. Unlike other GLONASS bands, L3 band has In-phase and Quadrature channels. The in-phase band contains the navigation data however the quadrature phase contains dataless signal. GLONASS L3 band transmits at 1201 MHz and it uses BPSK data modulation. Table 2.9 summarises some details of the GLONASS L3 signal structure.

Table 2.9: Detailed GLONASS L3 Signal Properties

GLONASS		
Frequency Band	L3	
Access Technique	FDMA	
Carrier [MHz]	1201	
Service Name	L3I	L3Q
Signal Component	Data	–
Modulation	BPSK	BPSK
Sub-carrier [MHz]	–	–
Chipping Rate [Mcps]	4.092/ 8.184	4.092/ 2.046
Primary PRN Code Length		
Code Family		
Secondary PRN Code Length		
Data rate	100 bps or 125 bps	N.A.

2.6 Generic GNSS Receiver

Before going into more detail of the research it is important to explain some essential information about GNSS signals. Figure 2.5 shows the overall diagram for a generic GNSS receiver showing the signal and data flow from the signal reception to position calculation. The operation of a generic GNSS is as follows: the RF signal is received via

an antenna and it is then filtered to remove the out of band of interest noise. Then the filtered signal is amplified with a Low Noise Amplifier (LNA) since the received signal is arriving from a satellite in space located at MEO which is around 20200 km above sea level and therefore it is highly attenuated [27, 28]. Then, depending on the receiver architecture type, the signal is shifted towards baseband in the analog domain [29, 30]. Then the analog signal is digitized with an Analog to Digital Converter (ADC). In some receivers it is useful to have Automatic Gain Control (AGC). This regulates the gain of the variable gain LNA which helps to utilize the analog to digital conversion dynamic range better. After the signal is digitized, the next step is to decimate and filter the incoming signal. Decimation reduces the sampling rate of the received data thus reducing the computational speed required to process it so reducing power consumption [31, 32]. Of course, filtering is required beforehand in order to avoid aliasing. The next step is to check which satellites are available within the received signal. This task is accomplished by the acquisition block. If there is any visible satellite that is acquired during this process then its satellite vehicle number, initial Doppler frequency and initial code offset are extracted and then this information is passed to the tracking block. Giving these initial parameters helps the tracking system to lock on the incoming signal faster. Tracking block keeps track of the satellites acquired as long as they are visible to the receiver. It keeps track of the received signal's code and carrier components which extract the navigation data that is required for the position calculation. For further information regarding the details of position calculation please refer to [1, 18].

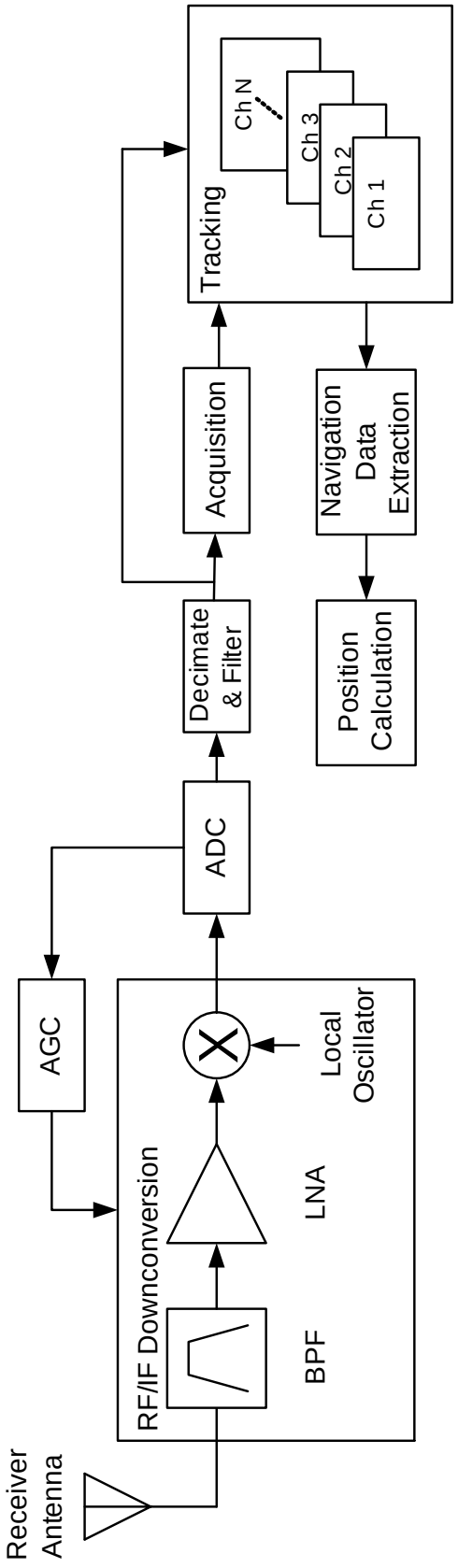


FIGURE 2.5: Generic GNSS Receiver

Chapter 3

GPS L1 Signal Acquisition & Tracking

This chapter gives an insight to GPS L1 acquisition which explains how a signal is processed in order to determine if there are any visible satellites. Then the next part explains tracking a GPS signal. Afterwards an experiment is carried out for tracking channel that exploits a weakness for a particular Doppler frequency. The chapter explains what the problem is and analyses any existing solutions and then it concludes with a proposed method to overcome the problem in hand.

3.1 Acquisition

As shown in Figure 2.5, acquisition is the first step to start the GNSS sequence. The acquisition process identifies the satellites that are visible to the receiver and calculates

each satellite's initial code phase and carrier Doppler frequency as well as their initial signal strength.

In the open literature, there are 3 types of acquisition techniques. Each acquisition technique has its own advantages and disadvantages. The following sections gives a brief description of these acquisition techniques. All 3 methods explained in the following subsections, they have a common property that is only one satellite can be identified at a time.

3.1.1 Serial Search Acquisition

The serial search acquisition method identifies the visible satellites sequentially. It should be noted that the serial search acquisition method performs a 2 dimensional search per satellite in order to find if there are any visible satellites. It begins the satellite search by first multiplying the incoming signal with a locally generated PRN code for a given satellite with a zero code offset. Then the resulting signal is multiplied with the locally generated carrier wave. The carrier wave that is multiplied with the received signal does not have a fixed but it usually has a range of ±5kHz that varies around the Intermediate Frequency (IF) with a given step size(e.g. steps of 500Hz). This means that 21 different carrier wave signals will be generated in order to multiply the received signal for a single code phase. Each time the locally generated PRN code's phase is shifted until an alignment occurs between the local PRN code and the incoming signal. Then the signal is multiplied with the local carrier wave. This removes any existing carrier Doppler frequency and creates two baseband signals, In-phase and

Quadrature. Each baseband signal is then accumulated at least over 1 PRN code period (that is 1ms worth of samples for GPS L1 C/A code). These accumulations are squared and then added together to provide an estimate of the signals power. Figure 3.1 shows the block diagram visualisation of this method [1].

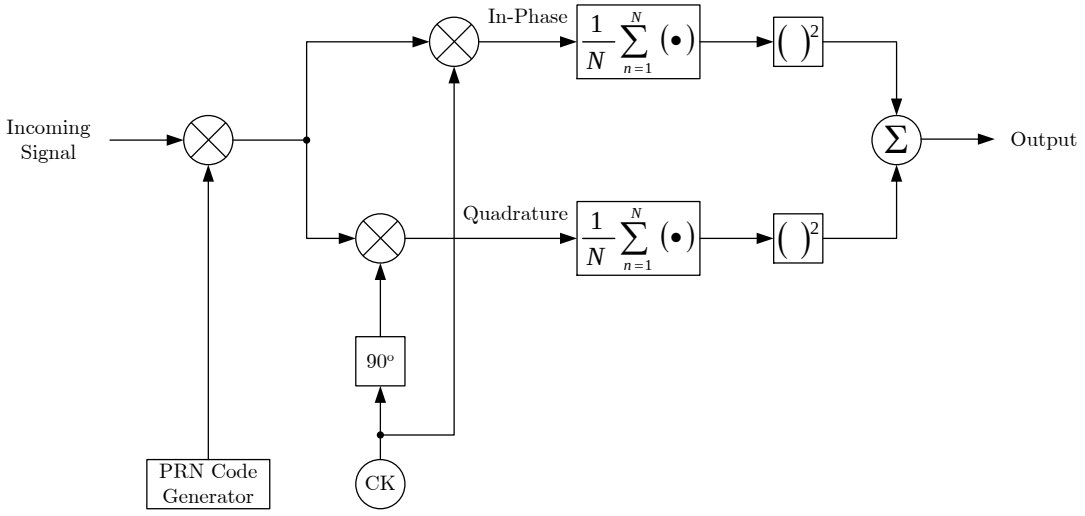


FIGURE 3.1: Block diagram of Serial Search Acquisition

The advantage of this method of acquisition is its simplicity. Therefore, the cost of implementing this method is the lowest among the acquisition methods. However, it has a big disadvantage which is due to its simplistic architecture in that it takes the most number of iterations per satellite in order to give an output.

3.1.2 Parallel Frequency Search Acquisition

The serial search acquisition algorithm is an exhaustive and time consuming method. This is the parallel frequency search acquisition method which is shown in Figure 3.2 [1]. The parallel frequency search acquisition method simplifies the carrier Doppler frequency search by taking the incoming signal from the time domain into the frequency

domain and identifying the frequency shift in one shot. This reduces the frequency search time by keeping the code phase search same as it is in the serial search method (shifting the locally generated PRN code by one sample until the perfect alignment occurs, which corresponds to the code phase in the received signal).When the received signal's code phase matches with the locally generated PRN code's phase a peak occurs at the output of the multiplier which is in the time domain. The position of the peak determines the code phase however it does not give any information about the carrier Doppler frequency. Because of this the multiplication result that is in time domain is taken to the frequency domain which reveals the carrier Doppler frequency. The disadvantage of this method is the implementation complexity. Compared to serial search acquisition, parallel frequency search acquisition has higher complexity due to the cost of the Fourier transformation algorithm. Despite using the efficient Fast Fourier Transform (FFT), this part of the system uses the most hardware resources.

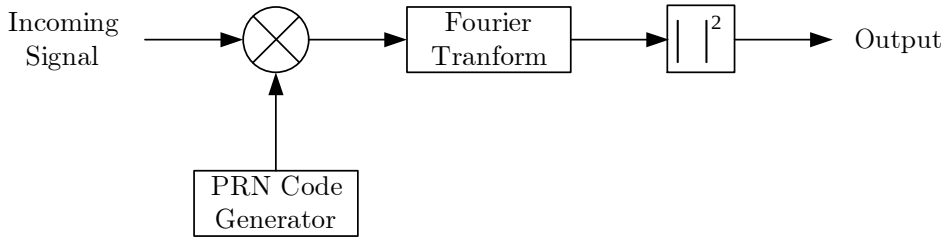


FIGURE 3.2: Block diagram of Parallel Frequency Search Acquisition

3.1.3 Parallel Code Phase Search Acquisition

Although parallel frequency search method reduces the execution time by doing a parallel frequency search, performing a serial code phase search still takes considerable execution time. Hence the method of parallel code phase search algorithm has been

developed. Compared to parallel frequency search method it searches the code phase in parallel but keeps the frequency search serial. This increases the execution speed because the code phase search step is much smaller compared with the frequency search step [33–36]. Figure 3.3 shows the block diagram of this method of acquisition [1]. As it can be seen from the figure, there are 2 different FFT and one Inverse Fast Fourier Transform (IFFT) blocks. In practice rather than taking the FFT of the locally generated PRN code, they are locally stored in a memory and read during the acquisition process. Although this saves 1 FFT, the complexity of this method is the highest compared to the other previously shown methods. However the execution time is the fastest [37, 38].

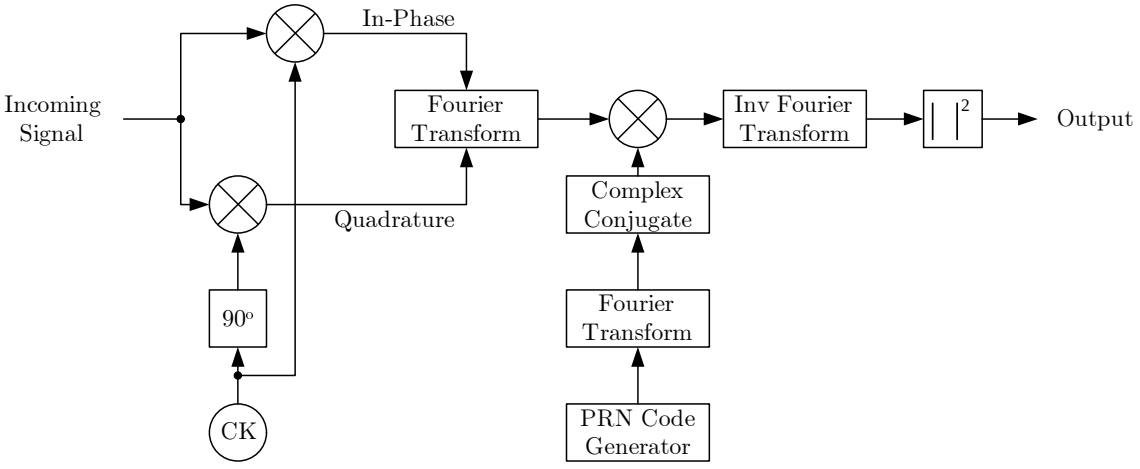


FIGURE 3.3: Block diagram of Parallel Code Phase Search Acquisition

3.2 Tracking

During acquisition, the device tracks satellites which are visible to the device and determines their initial carrier Doppler frequency and initial code phase. Then acquisition passes the initial information to tracking processor where the acquired satellites

are tracked as long as they are visible to the receiving system. Figure 3.4 shows the overall diagram of a generic tracking-loop processor [39]. The following subsections explains the parts of the tracking loop in more detail.

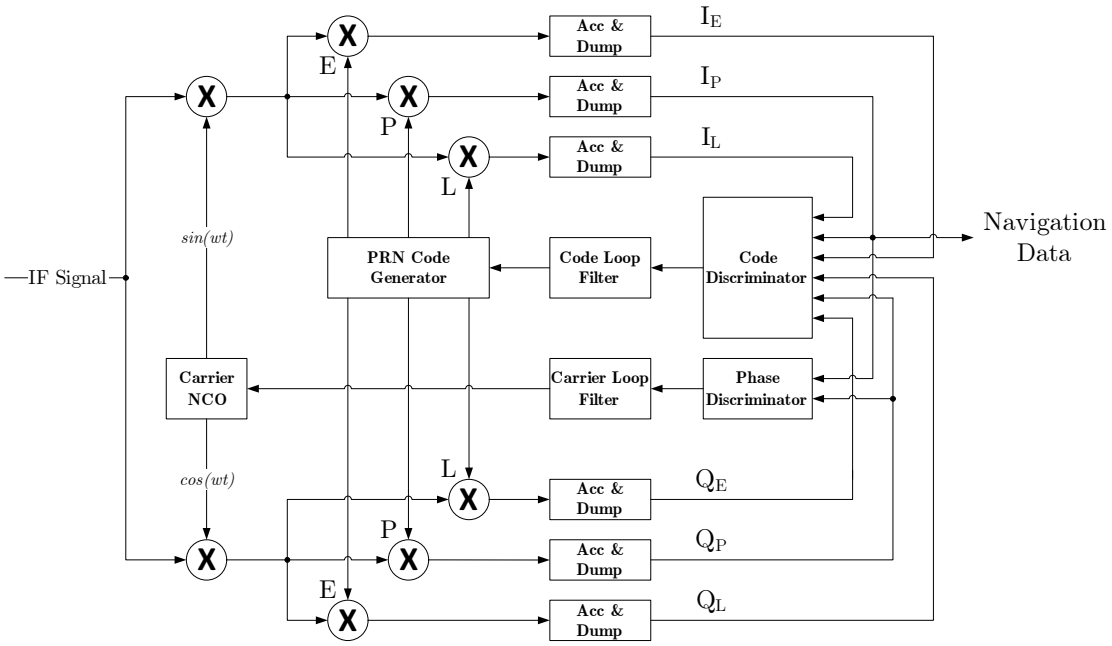


FIGURE 3.4: Block diagram of a generic tracking loop processor

3.2.1 Carrier Tracking with low Doppler Frequency

The discriminator is at the heart of the tracking engine. There are two types of discriminators which can be used for tracking; The Costas Phase Locked Loop (PLL) and the Frequency Locked Loop (FLL). A Costas PLL delivers phase error as an output where as an FLL delivers a frequency error. The Costas PLL type of discriminators can track more accurately compared with the FLL type of discriminator. However, they have higher sensitivity to dynamic stress in comparison to the FLL [12]. Traditionally, the Costas PLL is used for tracking GPS signals because they are insensitive to data

modulation [40]. A generic GNSS tracking loop is depicted in Figure 3.5 which is part of the overall tracking loop processor.

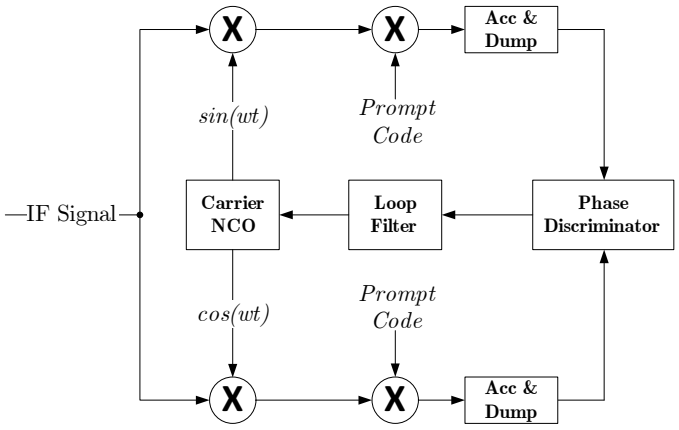


FIGURE 3.5: Generic GNSS Carrier tracking loop

As it can be seen in Figure 3.5, the GNSS tracking loop is different to a conventional Costas PLL in that it has an extra pair of multipliers and Accumulation and Dump blocks. This is because the incoming signal is modulated with a PRN sequence and this needs to be stripped off during the tracking process.

In a direct sampling type of receiver, the incoming signal is down converted to a low IF. Then this IF signal is further translated to the baseband by multiplying it with a locally generated Numerically Controlled Oscillator (NCO) using the carrier tracking loop. According to Tsui [41] a Doppler shift of up to ±5 kHz is possible including 0 Hz which means no Doppler shift. However if the Doppler frequency is lower than the loop bandwidth of the PLL the tracking loop is highly likely to have difficulty keeping in lock with the incoming signal. This is the case when the number of bits is 1-bit for the NCO output. Having 1-bit at the NCO output can reduce the complexity of the mixer (multipliers) as well as the subsequent circuitry. As can be seen from figure 3.6 when the NCO output is quantized to 1-bit the PLL oscillates around the residual

Doppler frequency of 10Hz. The amount of the swing is determined by the loop filter's bandwidth. The same approach is applied with same parameters when the incoming signal has a Doppler frequency of 3kHz. This time, as it can be seen from the figure 3.7, the PLL is able to track without any problem.

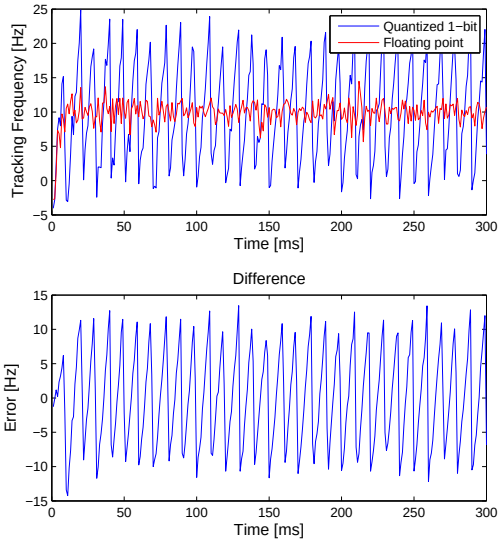


FIGURE 3.6: Tracking low frequency Doppler shift (10 Hz) with quantized NCO output

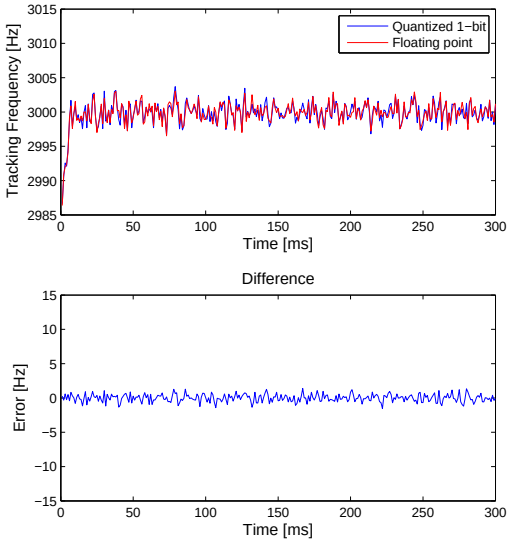


FIGURE 3.7: Tracking high frequency Doppler shift (3 kHz) with quantized NCO output

3.2.2 Existing Solution

One solution to overcome this problem without increasing the NCO output word length is the technique used by Weiler [6]. In [6], firstly, the local carrier wave is generated in high resolution and then quantized to a lower resolution. The modified tracking loop structure is shown in Figure 3.8. The modulation algorithm used for this technique for a 1-bit output is given in Equation 3.1.

$$S_i = \begin{cases} -1 & o_i < n_i \\ +1 & o_i \geq n_i \end{cases} \tag{3.1}$$

where s_i, o_i and n_i are the modulated signal, high resolution carrier wave and noise, each at ith sample, respectively.

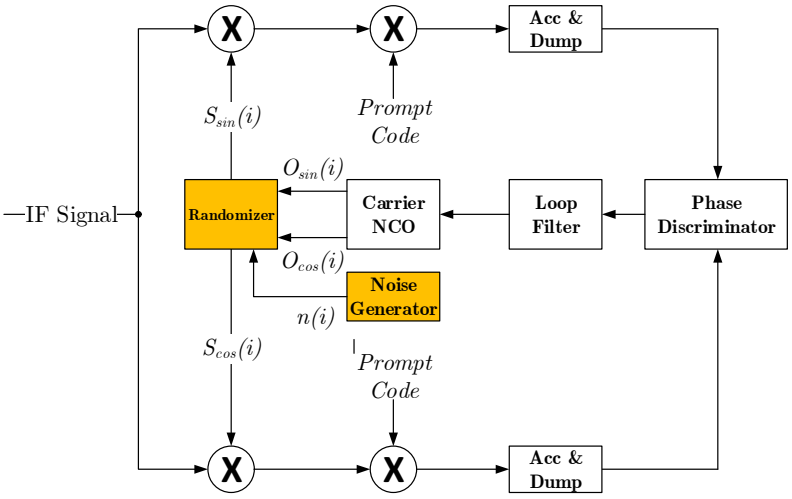


FIGURE 3.8: Modified tracking loop structure with noise modulated local carrier wave

The result of the noise modulated carrier wave for a 1-bit output is shown in Figure 3.9. Figure 3.9 (a) shows the high resolution sine wave in red and the modulated noise is shown with two levels (±1) in blue. The bottom plot shows the result after filtering the modulated signal with a low-pass filter. This filter emulates the characteristic of the tracking loop filter which shows us the output of the loop filter. As it can be seen from Figure 3.9 (b), some of the noise injected to the system cannot be filtered since it is in the passband of the loop filter. Standard deviation, shown as Std:0.082, shows how much the error fluctuates around the high sampled carrier wave. Integrating this

modification into the tracking loop and simulating gives the results which are presented in Figure 3.10.

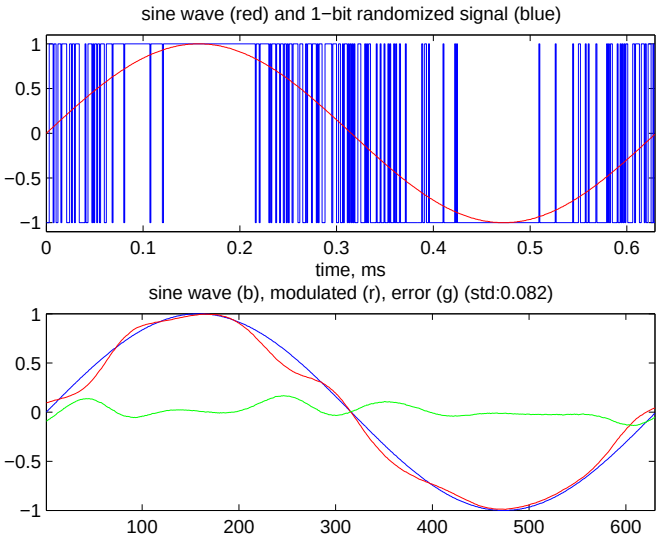


FIGURE 3.9: High resolution local carrier wave and modulated with 1 bit random noise

3.2.3 Proposed Solution

Results that are presented in [6] show that the problem with low Doppler frequency can be avoided by oversampling the locally generated carrier wave of the NCO and then modulating it with a random noise generator. However, the introduction of noise which cannot be filtered completely produces results which are worse than the floating point results. Recalling the main aim of this modification which was to reduce the complexity for the mixer multiplication inside the carrier tracking loop, having a good random noise generator with near ideal flat noise distribution requires hardware which may not reduce the complexity in the overall tracking circuit, but on the contrary increase the overall complexity.

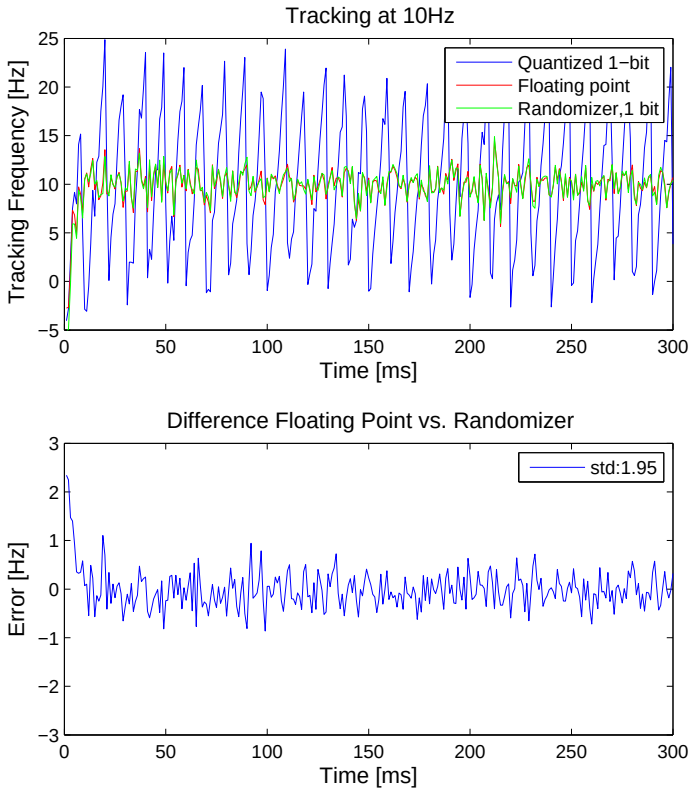


FIGURE 3.10: Tracking Carrier Frequency with Randomizer at 10Hz

Instead of using a random noise generator and modulating the carrier wave, a better approach could be modulating the locally generated carrier wave with a Discrete-Time (DT) low pass Sigma-Delta ($\Sigma\Delta$) Modulator [42]. $\Sigma\Delta$ modulators are good for modulating a high resolution data into a lower resolution in the form of Pulse Density Modulation (PDM) without compromising the quality of the original data [43]. This is because the noise generated from the quantizer of the lowpass $\Sigma\Delta$ modulator is shaped away from the lower frequencies which enables the carrier wave to have a higher dynamic range. Figure 3.11 shows the proposed modification to the carrier tracking loop with $\Sigma\Delta$ modulator at the output of the NCO where Figure 3.12 shows the structure of the $\Sigma\Delta$ modulator used in order to overcome the problem associated with the 1-bit modulated carrier wave. Figure 3.13 (a) depicts the high-resolution sine wave in red

and the ΣΔ modulated data in blue. As it can be seen the ΣΔ modulator can modulate the input data with much higher density and, since it shapes the noise away from the low frequency range after passing it through a lowpass filter, it leaves a much cleaner sine wave as shown in Figure 3.13(b) [44].

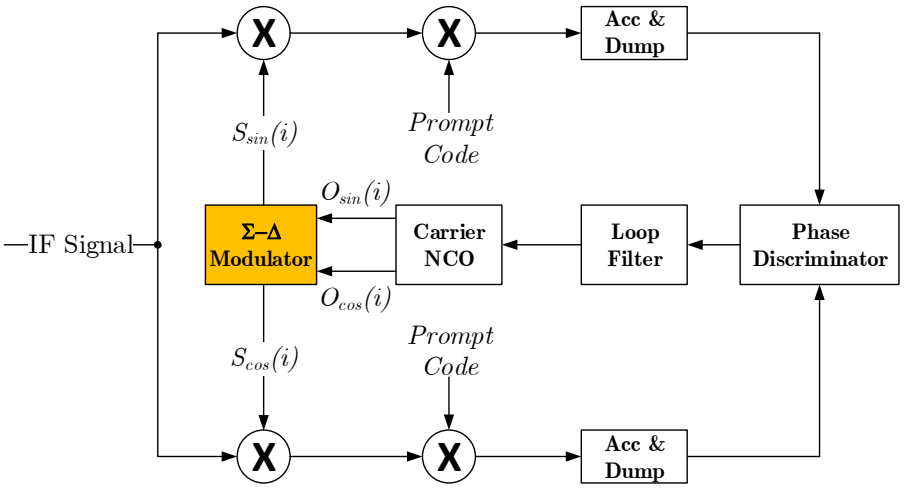


FIGURE 3.11: Modified tracking loop structure with ΣΔ modulated local carrier wave

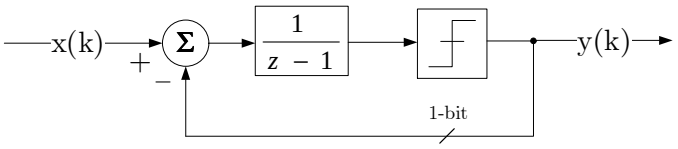


FIGURE 3.12: 1st order low pass DT ΣΔ modulator with 1-bit quantizer

3.2.4 Results

Intuitively an improvement was expected from the ΣΔ modulator as it shaped the noise away from the input tone, rendering the in-band noise of the 1-bit ΣΔ modulated carrier wave smaller than the random noise modulated counterpart. By running the tracking loop with the ΣΔ modulator it has been shown that the tracking is improved compared with randomizer (random noise modulated) structure. Figure 3.14 shows the tracking

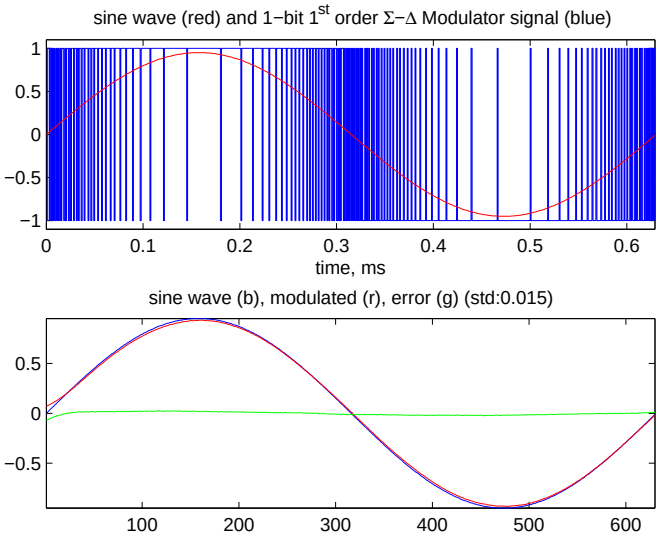


FIGURE 3.13: High resolution local carrier wave and modulated with 1st order ΣΔ modulator

results for identical input conditions with the proposed modification that deploys the ΣΔ modulator modulated carrier wave.

If a higher order ΣΔ modulator is deployed instead of a simple 1st order one, higher dynamic range can be achieved for the carrier wave. However, as the noise in the band of interest gets lower, the out-of-band noise gets higher. When demodulated, this noise in the higher frequencies folds back in to the band of interest which deteriorates the tracking performance. Table 3.1 shows the study where 1st, 2nd and 3rd order ΣΔ modulator is deployed at the output of the NCO and the tracking performance measured. As it can be seen from Table 3.1 having higher order ΣΔ modulator deteriorates the tracking performance as measured by the standard deviation of the tracked frequency.

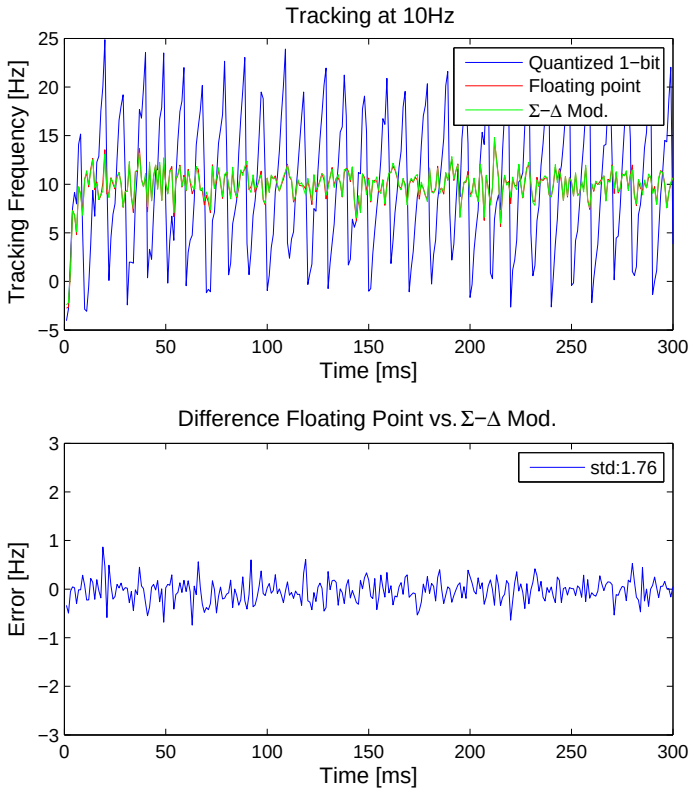


FIGURE 3.14: Tracking Carrier Frequency with ΣΔ Modulator at 10Hz

TABLE 3.1: Comparison of Various ΣΔ Modulator Performance

	Standard Deviation, σ	
NCO output resolution	**10Hz Doppler**	**3kHz Doppler**
Floating Point	1.7897 Hz	1.7282 Hz
1^{st} order ΣΔ modulator 1 bit	1.7588 Hz	1.7291 Hz
2^{nd} order ΣΔ modulator 1 bit	1.9192 Hz	1.9124 Hz
3^{rd} order ΣΔ modulator 1 bit	1.9284 Hz	1.9237 Hz

3.3 Chapter Conclusion

It has been shown that the problems associated with tracking a GPS signal when a low carrier Doppler frequency is present with the minimum number of bits used at the NCO output. The results show that when the output of the NCO is quantized to 1 bit leaves the tracking loop oscillating around the Doppler frequency of 10 Hz. However, one solution to the problem found in the literature suggests modulating the local carrier

wave of the NCO with a random signal generator. Although this method appears to work it injects extra noise to the system that cannot be fully filtered. Also, in order to generate a truly random tone free noise generator the computational complexity is increased.

An alternative to a randomizer has been presented which uses a simple 1^{st} order $\Sigma\Delta$ modulator with a 1 bit quantizer instead of a random signal generator. By using a $\Sigma\Delta$ Modulator, instead of injecting noise to the system, the $\Sigma\Delta$ Modulator shapes the noise away from the local carrier wave allowing it to be eliminated by the loop filter. Table 3.2 shows the comparison of the overall tracking performance in terms of standard deviation in the tracking of carrier Doppler frequency. As can be seen from Table 3.2, using a 1st order $\Sigma\Delta$ results in tracking performance as good as the floating point results. Furthermore, it has lower computational complexity than the Randomizer approach.

In summary the solution presented has lower noise, hence better performance. Tracking works with less jitter. Also this is done with less computational complexity. So it gives better performance with less cost.

TABLE 3.2: Various methods performance comparison

	Standard Deviation, σ	
NCO output resolution	**10Hz Doppler**	**3kHz Doppler**
Quantized 1-bit	7.1660 Hz	1.7282 Hz
Floating point	1.7887 Hz	1.7744 Hz
Randomizer 1-bit	1.9523 Hz	1.9423 Hz
1^{st} order $\Sigma\Delta$ modulator 1 bit	1.7588 Hz	1.7291 Hz

Chapter 4

Area utilisation & Power dissipation of a GNSS Receiver

In order to be able to reduce the power consumption and be able to minimize the computational complexity in a GNSS receiver it is important to look at the individual blocks along the receiver chain. This will help to identify where most of the power is dissipated. This chapter explains the development of an area utilisation and power estimation tool that has been developed during the research in order to have a better understanding of the power dissipation and resources required for a GNSS receiver. Therefore this chapter begins by explaining the details of the appropriate tool that has been developed in order to be able to carry out the power and area estimation. Then the results of the power and area estimation are presented.

In the open literature, there is not much available resources that estimates the power dissipation in a digital circuit especially for decimation filters. For example in a

decimation processor there are flip-flops where the data input pin have higher switching activity than the clock and output pin. Usually the existing power estimation tools use different methods to calculate the average activity for the data input pin which is actually slower than the clock pin [45–47]. However the equation 4.2 overcomes this problem by describing the input pins independently.

4.1 Power Analysis Tool

In a given circuit power is only dissipated when a load charges or discharges [48, 49]. This is usually represented with a Complementary Metal Oxide Semiconductor (CMOS) inverter circuit as shown in Figure 4.1. The power calculation is based on the load capacitance C_L, the supply voltage Vdd, and the switching frequency, f_{on}, of the output Out_L which is shown in Equation 4.1.

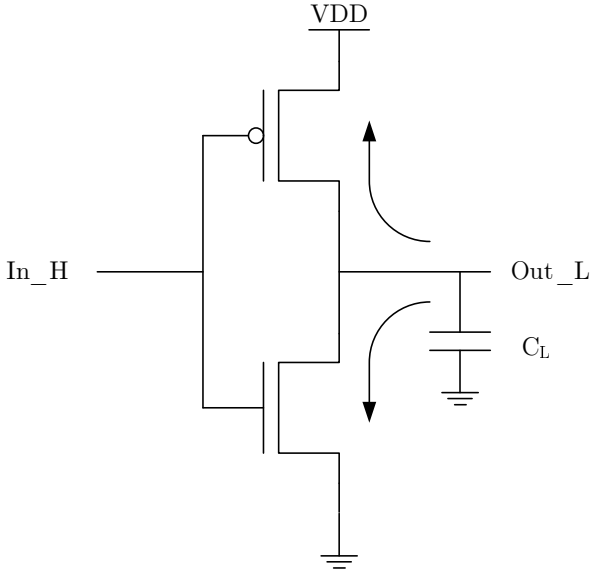


FIGURE 4.1: Power dissipation in a CMOS Inverter

$$P_{avg} = C_L.{V_{dd}}^2.\frac{1}{2}f_{on} \tag{4.1}$$

However, it is very laborious and complicated to estimate the power dissipation of a digital design using the formula given above. It is more convenient to estimate the power dissipation in a digital circuit at the gate or RTL level. When the power is estimated at the gate/RTL, the equation 4.1 becomes insufficient. This is because the logic gates contain multiple transistors that are cascaded and depending on the input behaviour the internal transistor notes switches as well which this formula does not cover.

This means power is dissipated not only by the output load but also it is depends on the input as well. Therefore a more accurate equation for power dissipation calculation is given in equation 4.2 [50]. This uses the energy value for each input pin that is the average energy of an input transition that results in an output transition.

$$P_{avg} = \sum_{n=1}^{x}(E_{in}.f_{in}) + \sum_{n=1}^{y}(C_{on}.{V_{dd}}^2.\frac{1}{2}f_{on}) + E_{os}.f_{o1} \tag{4.2}$$

where:

P_{avg} = average power (μW);
x = number of input pins;
E_{in} = energy associated with the nth input pin (μW/MHz);
f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);
y = number of output pins;
C_{on} = external capacitive loading of the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

Vdd	=	operating voltage = 1.8V (technology: 180nm);
f_{on}	=	frequency at which the nth output pin changes state during the normal operation of the design (MHz);
E_{os}	=	energy associated with the output pin for sequential cells only (μW/MHz);
f_{o1}	=	frequency at which the nth output pin for sequential cells changes state during the normal operation of the design (MHz);

The power analysis tool is developed using Taiwan Semiconductor Manufacturing Company (TSMC) 180nm technology components using basic building blocks such as Adders, Multipliers, Registers, Quantizers, etc... It requires to describe the hardware complexity using these basic building blocks and it outputs the estimated power dissipation in microwatts (μW) and equivalent logic gate count which represents the estimated area utilisation of the circuit. With this developed tool, most parts of the GNSS receiver was analysed in order to have an estimate of the power dissipation as well as the hardware resource requirement when implemented. The tool has the flexibility to enter independently each basic element's input/output activity speed, clocking speed if exists, number of input/output widths as well as their utilisation percentage. The list of components are listed below:

- Full Adder (signed & unsigned)
- Modified Booth Multiplier
- Non-transparent register with clear facilities (DFF)
- Transparent register with clear facilities (Latch)
- 2:1 and 4:1 multiplexer

- 2-input combinational logic (OR, AND, XOR, XNOR, INVERTER)
- Counter (with load & without load)
- Quantize (truncate, round, convergent and return-to-zero).

In order to demonstrate how the power analysis tool is used an example is given below. For this example an Accumulation and Dump block used in the tracking loop as shown in 3.4 is chosen. The hardware for implementing Accumulation and Dump is shown in Figure 4.2.

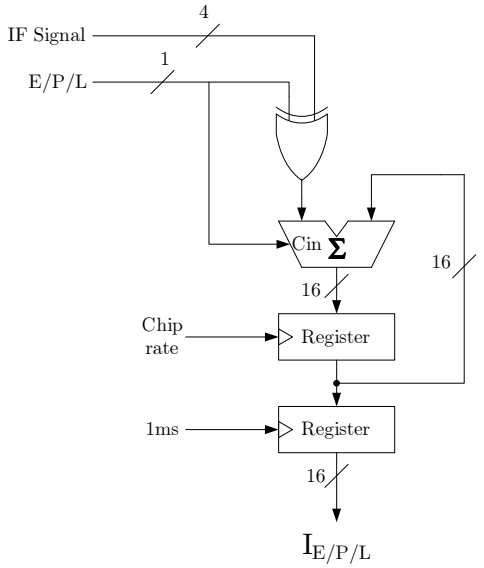


FIGURE 4.2: Circuitry for an Accumulation and Dump in the GNSS tracking loop

Each individual Accumulation and Dump block as shown in Figure 4.2 is realized in terms of hardware as one 4-bit 2-input XOR gate, one 16-bit signed Adder and two 16-bit registers that operate at different clock rates. Also for every Early, Prompt and Late signals one Accumulation and Dump block is required totalling 3 blocks.

Figure 4.3 shows the screen shot of the power analysis tool developed for the example of an Accumulation and Dump block found in the tracking loop. When the hardware

complexity is entered as given above it calculated the power and hardware complexity in terms of μW and equivalent logic gate respectively. For this particular example the power estimation tool has estimated the hardware complexity to be 1410 logic gate equivalent that dissipates 257μW as shown in Figure 4.3.

Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Iterations / ms of data	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	
Adder (RCA)	Signed	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Unsigned	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
Acc Adder	Signed	3	16-bit	x	10000	100	10.000 MHz	x	10.000 MHz	246	164.06	
Multiplier	Dynamic	0	5-bit	4-bit	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Constant	0	1-bit		1	100	10.000 MHz	x	10.000 MHz			
								x				
Register	Latch	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
	DFF	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
Acc Reg	DFF	3	16-bit	x	10000		10.000 MHz	10.000 MHz	10.000 MHz	576	60.09	
O/P Reg	DFF	3	16-bit		1		10.000 MHz	0.001 MHz	0.001 MHz	576	23.43	
Multiplexer	2:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	4:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
Combinational Logic	OR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	AND2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XNOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
	INV	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00	
XOR for Sub	XOR2	3	4-bit				10.000 MHz	x	10.000 MHz	12	9.40	
			x	x								
									TOTAL =	1410	256.97	µW

FIGURE 4.3: Screen shot of the Power Analysis tool

Although the technology used to develop the power estimation tool is chosen to be 180nm, it can easily be adapted to a different technology by providing appropriate input energy consumption and load capacitances of the basic building blocks used. Also the power tool is developed in order to have a relative comparison of power dissipation and hardware complexity between different parts of the GNSS receiver in order to establish where the most of the power is dissipated. Therefore using technology scale that is smaller or higher is irrelevant.

4.2 Power Budget of a GNSS Receiver

After the power analysis tool is developed, the next step was to look into individual sub-systems in the GNSS receiver in order to see where the most of the power is dissipated. A detailed power analysis was undertaken in order to assess how much power is dissipated in each of the digital sub-systems in the GNSS receiver (i.e. after the analog to digital conversion). The part of the system that is always operational is the Decimation and Filtering part where the signal is being constantly received. Therefore it is useful to have an estimated power dissipation analysis of this part. Yet another part of the receiver that is operating for most of the time is the tracking loop. The tracking loop has to operate as long as there are visible satellites. Therefore these two parts of the system have been analysed and following subsections explain the power and hardware usage estimation in detail.

4.2.1 Accumulation & Dump

This block is responsible for accumulating the number of received data samples over 1 code period of the GPS L1 C/A code. Each individual Accumulation and Dump block as shown in Figure 4.2 is realised in terms of hardware as one 4-bit 2-input XOR gate, one 16-bit signed Adder and two 16-bit registers that operate at different clock rates. Also for every Early, Prompt and Late signals one Accumulation and Dump block is required totalling 3 blocks. On top of that, tracking channel has two branches, in-phase and quadrature, so in total there are 6 Accumulation and Dump blocks in

tracking processor. Figure 4.4 reflects the power and hardware usage estimation based on the structure shown in Figure 4.2.

Tracking - Acc & Dump

Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
Acc Adder	Signed	6	16-bit	x	100	10.000 MHz	x	10.000 MHz	492	328.13	
Multiplier	Dynamic	0	5-bit	4-bit	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Constant	0	1-bit		100	10.000 MHz	x	10.000 MHz			
							x				
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
Acc Reg	DFF	6	16-bit	x		10.000 MHz	10.000 MHz	10.000 MHz	1152	120.18	
O/P Reg	DFF	6	16-bit			10.000 MHz	0.001 MHz	0.001 MHz	1152	46.86	
Multiplexer	2:1	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	4:1	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
Combinational Logic	OR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	AND2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XOR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XNOR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	INV	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
XOR for Sub	XOR2	6	4-bit			10.000 MHz	x	10.000 MHz	24	18.79	
			x	x							
								TOTAL =	2820	513.95	µW

FIGURE 4.4: Power usage estimation of Accumulation & Dump

4.2.2 Carrier Discriminator

Carrier discriminator in a tracking loop keeps track of the received signal's carrier wave by adjusting the phase in every iteration. The structure shown in Figure 4.5 was realised in terms of hardware as a COordinate Rotation DIgital Computer (CORDIC) structure. CORDIC structure is an efficient processor that can implement trigonometric functions without using any multipliers therefore they consume less power [51, 52]. As can be seen from the Figure 4.5, to implement the carrier discriminator, 2 2-to-1 multiplexers, 3 negators, 3 registers, 3 adders, a counter and 2 shifters are required. For the power estimation tool, ROM or RAM structures are not implemented as they are more complex and their power consumption are based on the actual data written/read as well as many other factors. Nevertheless, power consumption of the memory elements was not expected to dominate the power dissipation in decimation and filtering part of the receiver chain as will be explained in the following subsections. The power estimation is shown in Figure 4.6.

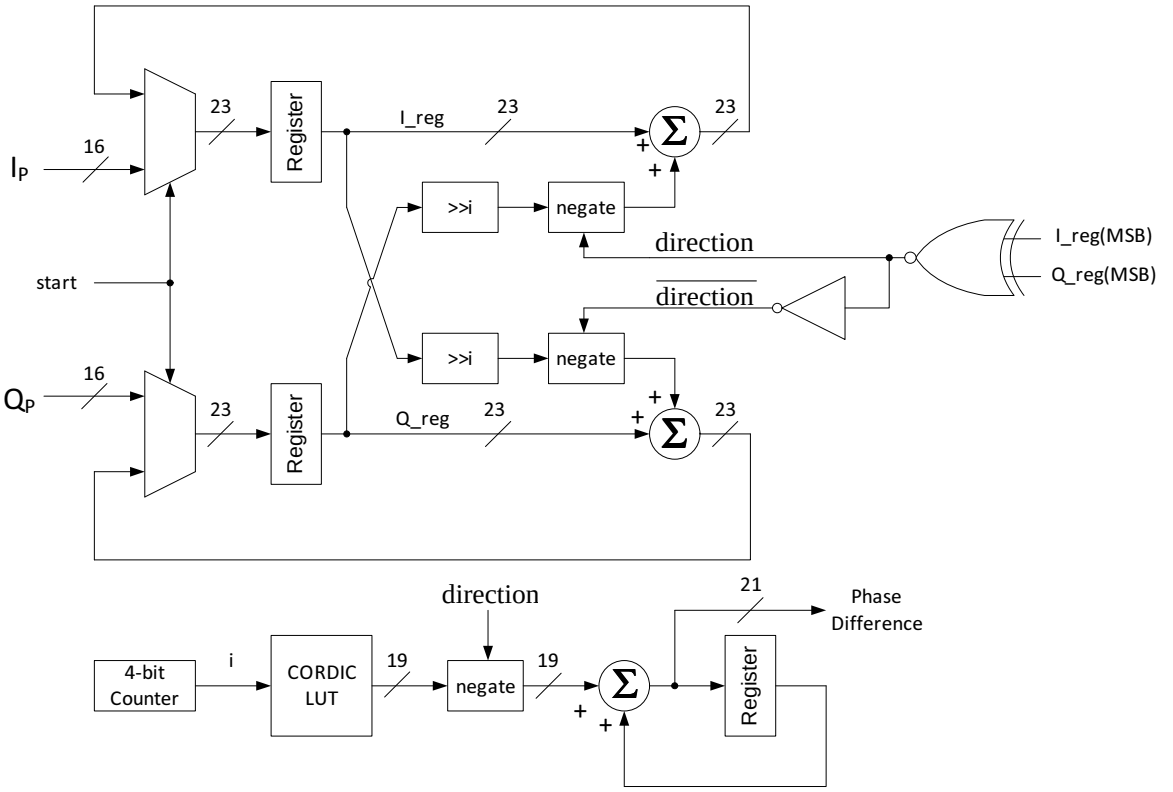


FIGURE 4.5: Structure of Carrier Discriminator

Tracking - Carrier Discriminator

Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Iterations / ms of data	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Unsigned	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Iterate Adder	Signed	2	23-bit	x	16		0.016 MHz	x	0.016 MHz	234	0.25120	
Count Adder	Signed	1	21-bit	x	16		0.016 MHz	x	0.016 MHz	107	0.11472	
Register	Latch	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	DFF	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
Iterate Reg	DFF	2	23-bit	x	16		0.016 MHz	0.016 MHz	0.016 MHz	552	0.09214	
Count Reg	DFF	1	21-bit	x	16		0.016 MHz	0.016 MHz	0.016 MHz	252	0.04206	
Multiplexer	2:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	4:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Input Mux	2:1	2	23-bit		16		0.016 MHz		0.016 MHz	142	0.06662	
Barrel Shift	2:1	184	1-bit		16		0.016 MHz		0.016 MHz	920	0.26649	
Combinational Logic	OR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	AND2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	XOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	XNOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	INV	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Direction	XOR2	1	1-bit		16		0.016 MHz		0.016 MHz	1	0.00125	
Direction Negate	INV	1	1-bit		16		0.016 MHz		0.016 MHz	1	0.00021	
	INV	2	23-bit		16		0.016 MHz		0.016 MHz	46	0.00950	
Negate LUT	INV	1	19-bit		16		0.016 MHz		0.016 MHz	19	0.00393	
Counter	No Load	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	Loadable	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
4-bit Counter	No Load	1	4-bit	x	16		0.016 MHz	0.016 MHz	0.016 MHz	56	0.01564	
			x	x								
									TOTAL =	2330	0.86376	µW

FIGURE 4.6: Power usage estimation of Carrier Discriminator

4.2.3 Code Discriminator

Code discriminator in a tracking loop keeps track of the received signal's code phase. The structure shown in Figure 4.7 is realised in terms of hardware as a CORDIC structure and it is similar to carrier discriminator structure with the exception that phase difference is not required for code discriminator therefore the Look Up Table (LUT) and the subsequent blocks were not implemented. The power and hardware utilisation is shown in Figure 4.8.

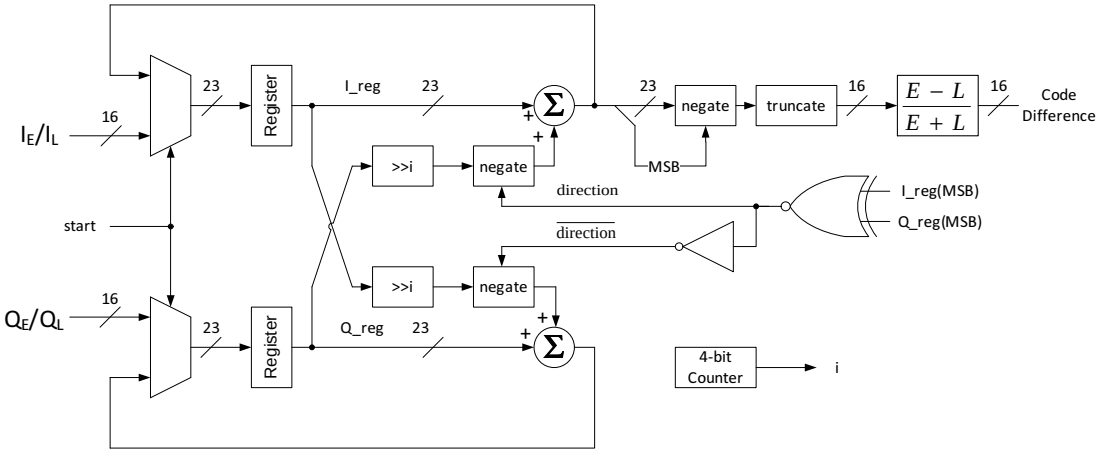


FIGURE 4.7: Structure of Code Discriminator

Tracking - Code Discriminator

Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Iterations / ms of data	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Unsigned	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Iterate Adder	Signed	2	23-bit	x	32		0.032 MHz	x	0.032 MHz	234	0.50240	
Register	Latch	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	DFF	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
Iterate Reg	DFF	2	23-bit	x	32		0.032 MHz	0.032 MHz	0.032 MHz	552	0.18427	
Count Reg	DFF	1	21-bit	x	32		0.032 MHz	0.032 MHz	0.032 MHz	252	0.08412	
Multiplexer	2:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	4:1	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Input Mux	2:1	2	23-bit		32		0.032 MHz		0.032 MHz	142	0.13325	
Barrel Shift	2:1	184	1-bit		32		0.032 MHz		0.032 MHz	920	0.53298	
Combinational Logic	OR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	AND2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	XOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	XNOR2	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	INV	0	1-bit	x	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
Direction	XOR2	1	1-bit		32		0.032 MHz		0.032 MHz	1	0.00251	
Direction	INV	1	1-bit		32		0.032 MHz		0.032 MHz	1	0.00041	
Negate	INV	2	23-bit		32		0.032 MHz		0.032 MHz	46	0.01901	
Negate O/P	INV	1	23-bit		32		0.032 MHz		0.032 MHz	23	0.00950	
Counter	No Load	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	Loadable	0	1-bit	x	1	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
4-bit Counter	No Load	1	4-bit	x	32		0.032 MHz	0.032 MHz	0.032 MHz	56	0.03128	
Quantizer	Truncate	0	24-bit	16-bit	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Round	0	24-bit	16-bit	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Convergent	0	24-bit	16-bit	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	RTZ	0	24-bit	16-bit	1	100	10.000 MHz	x	10.000 MHz	0	0.00000	
truncate	Truncate	1	23-bit	16-bit	32		0.032 MHz	x	0.032 MHz	0	0.00000	
									TOTAL =	2227	1.49973	µW

FIGURE 4.8: Power usage estimation of Code Discriminator

4.2.4 Carrier Loop Filter

Carrier loop filter was used in order to filter out the phase error obtained from the carrier discriminator that was fed to the Carrier NCO. The structure used and its power and hardware estimation are shown in Figures 4.9 and 4.10 respectively.

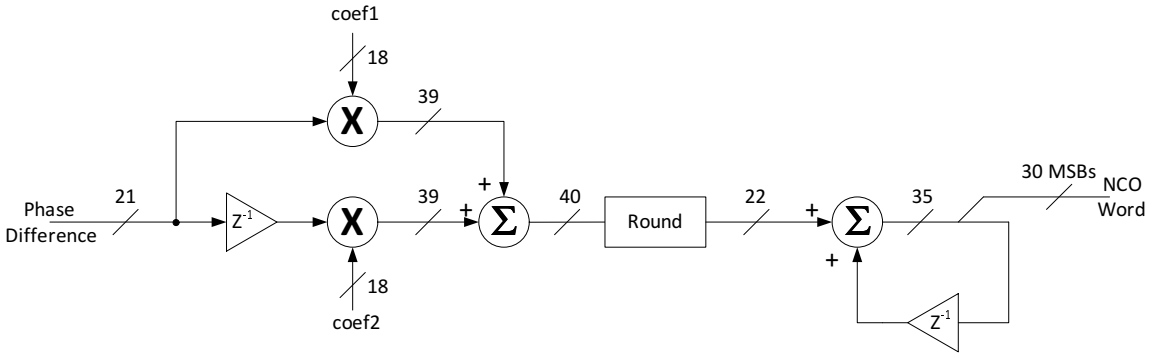


FIGURE 4.9: Structure of Carrier Loop Filter

Tracking - Carrier Loop Filter (PLL)											
Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00000	
FIR Adder	Signed	1	40-bit	x		0.001 MHz	x	0.001 MHz	202	0.01363	
Acc Adder	Signed	1	35-bit	x		0.001 MHz	x	0.001 MHz	177	0.01193	
Multiplier	Dynamic	0	5-bit	4-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Constant	0	1-bit		100	10.000 MHz	x	10.000 MHz			
Coef Mult	Dynamic	2	21-bit	18-bit		0.001 MHz	x	0.001 MHz	8636	0.27892	
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
FIR Reg	DFF	1	21-bit	x		0.001 MHz	0.001 MHz	0.001 MHz	252	0.00263	
Acc Reg	DFF	1	35-bit	x		0.001 MHz	0.001 MHz	0.001 MHz	420	0.00438	
Quantizer	Truncate	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Round	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Convergent	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	RTZ	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
FIR O/P Quan	Round	1	40-bit	22-bit		0.001 MHz	x	0.001 MHz	44	0.00453	
			x	x							
								TOTAL =	9731	0.31603	µW

FIGURE 4.10: Power usage estimation of Carrier Loop Filter

4.2.5 Code Loop Filter

Code loop filter was used in order to filter out the code error obtained from the carrier discriminator that was fed to the local PRN generator. The structure used, shown in Figure 4.11, is same as the carrier loop filter and only the parameters are different in order to adapt for filtering the code difference. Its power and hardware estimation is shown in Figure 4.12.

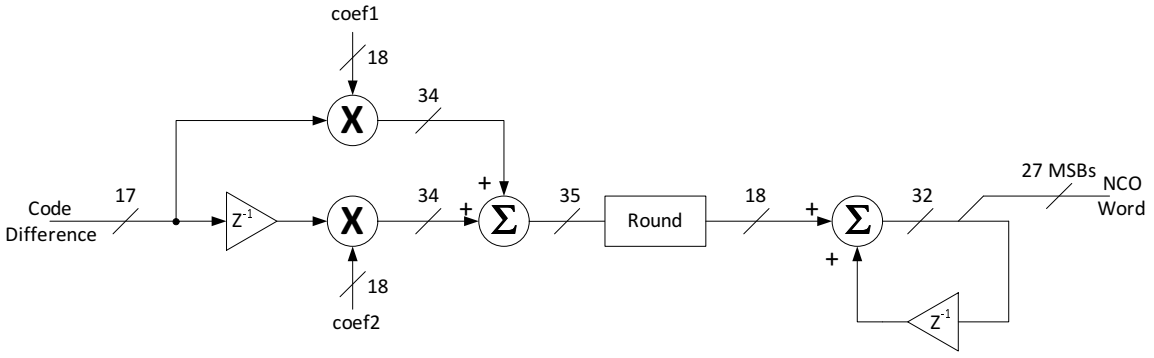


FIGURE 4.11: Structure of Code Loop Filter

Tracking - Code Loop Filter (DLL)

Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00000	
FIR Adder	Signed	1	35-bit	x		0.001 MHz	x	0.001 MHz	177	0.01193	
Acc Adder	Signed	1	32-bit	x		0.001 MHz	x	0.001 MHz	162	0.01091	
Multiplier	Dynamic	0	5-bit	4-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Constant	0	1-bit		100	10.000 MHz	x	10.000 MHz			
Coef Mult	Dynamic	2	17-bit	18-bit		0.001 MHz	x	0.001 MHz	7140	0.23101	
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00000	
FIR Reg	DFF	1	17-bit	x		0.001 MHz	0.001 MHz	0.001 MHz	204	0.00213	
Acc Reg	DFF	1	32-bit	x		0.001 MHz	0.001 MHz	0.001 MHz	384	0.00401	
Quantizer	Truncate	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Round	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	Convergent	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
	RTZ	0	24-bit	16-bit	100	10.000 MHz	x	10.000 MHz	0	0.00000	
FIR O/P Quan	Round	1	35-bit	18-bit		0.001 MHz	x	0.001 MHz	36	0.00371	
			x	x							
								TOTAL =	8103	0.26370	µW

FIGURE 4.12: Power usage estimation of Code Loop Filter

4.2.6 Carrier NCO

Carrier NCO generates a local oscillator that was used to demodulate the received GNSS signal. The structure for this block is shown in Figure 4.13. As mentioned in the previous subsections, the memory based elements are not ignored for the power estimation. Its corresponding power and hardware usage is shown in Figure 4.14.

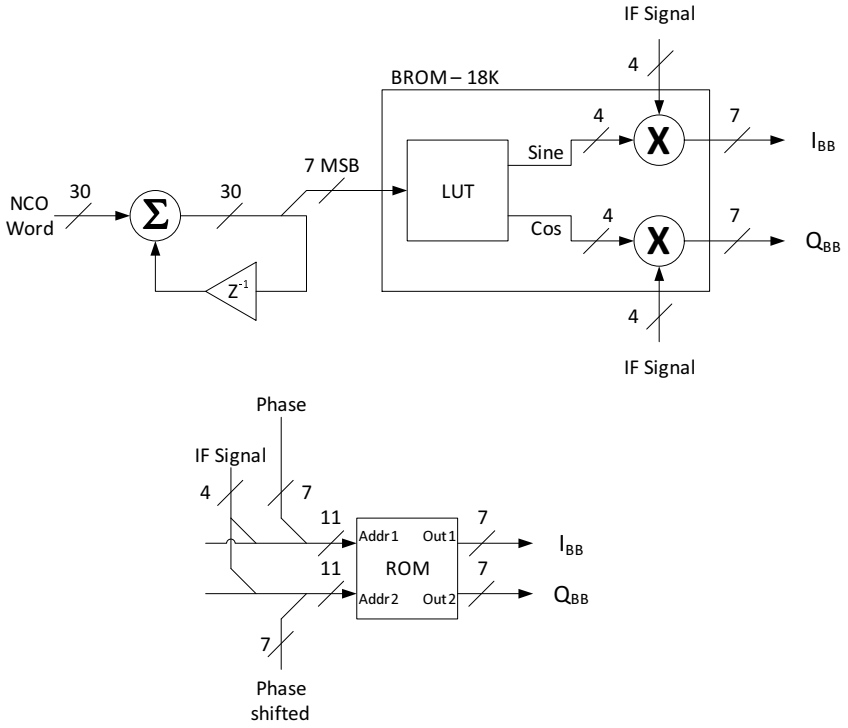
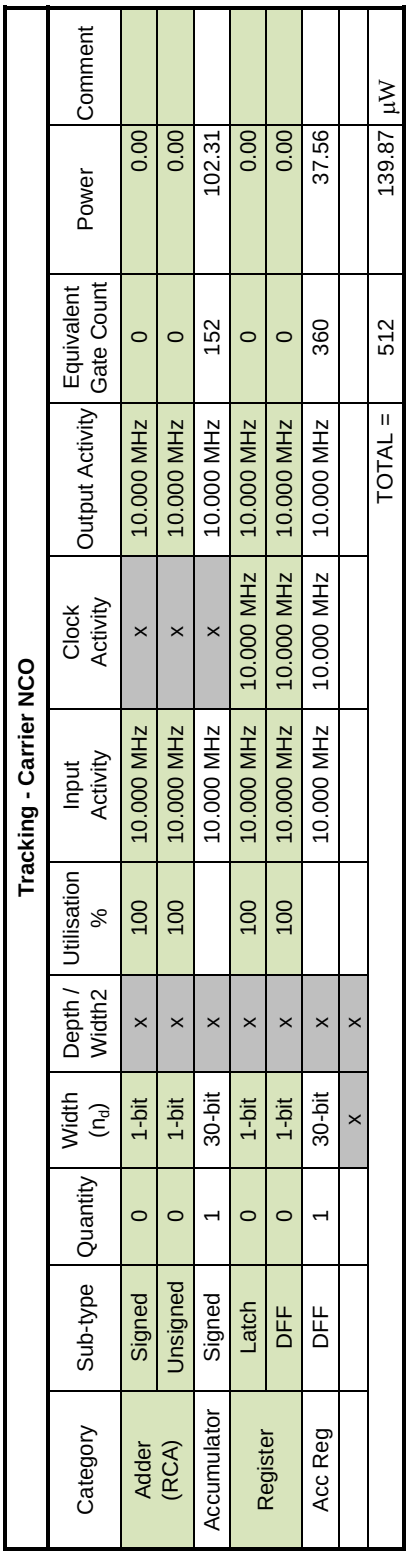


FIGURE 4.13: Structure of Carrier NCO



Tracking - Carrier NCO											
Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
Accumulator	Signed	1	30-bit	x		10.000 MHz	x	10.000 MHz	152	102.31	
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
Acc Reg	DFF	1	30-bit	x		10.000 MHz	10.000 MHz	10.000 MHz	360	37.56	
			x	x							
								TOTAL =	512	139.87	µW

FIGURE 4.14: Power usage estimation of Carrier NCO

4.2.7 Code NCO

Code NCO generates a local PRN code and their Early, Prompt and Late versions that is used to remove the PRN code from the received signal in order to obtain the navigation message. The structure for this block is shown in Figure 4.15. As mentioned in the previous subsections, the memory based elements are not ignored for the power estimation. Its corresponding power and hardware usage is shown in Figure 4.16.

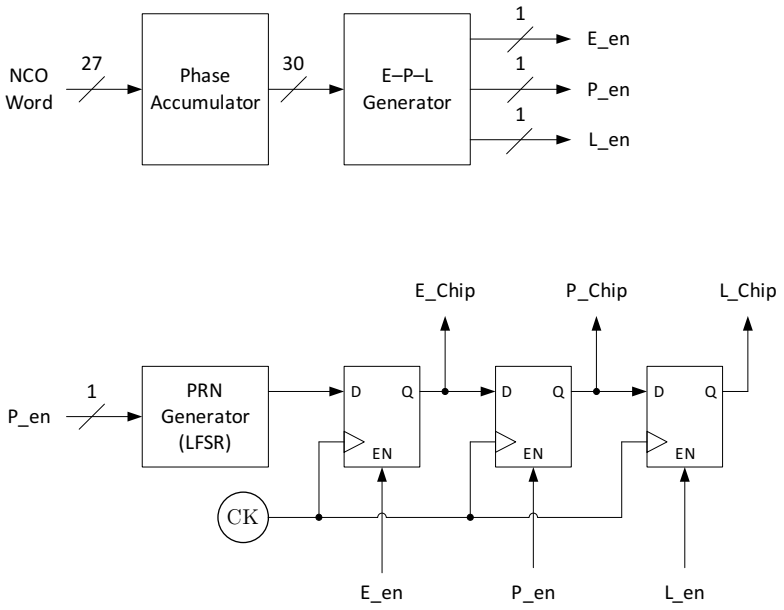


FIGURE 4.15: Structure of Code NCO

Tracking - Code NCO											
Category	Sub-type	Quantity	Width (n_a)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
Accumulator	Signed	1	30-bit	x		1.023 MHz	x	1.023 MHz	152	10.47	
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
Acc Reg	DFF	1	30-bit	x		1.023 MHz	1.023 MHz	1.023 MHz	360	3.84	
Chip Reg	DFF	3	1-bit			1.023 MHz	1.023 MHz	1.023 MHz	36	0.38	
LFSR	DFF	20	1-bit	x		1.023 MHz	1.023 MHz	1.023 MHz	240	2.56	
Combinational Logic	OR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	AND2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XOR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	XNOR2	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	INV	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
LFSR	XOR2	8	1-bit	x		1.023 MHz		1.023 MHz	8	0.64	
			x	x							
								TOTAL =	796	17.89	µW

FIGURE 4.16: Power usage estimation of Code NCO

4.2.8 Filtering and Decimation

Filtering and Decimation was used in order to reduce the sampling rate of the received signal since its sample rate of 240 MHz is much higher than the signal's bandwidth of 8 MHz. The filter was implemented as an FIR filter of order 215 and it was implemented with polyphase decomposition in order to be able to operate the filter at the output rate rather than the input rate, which was much faster. Due to the size of the FIR filter an example of the whole structure is given in Figure 4.17. In Figure 4.17 a decimation by 3 model is shown as an example, however for the actual implemented filter a decimation by 24 is used therefore the commutator is a 24 way switch and each polyphase path had 9 coefficients. The power estimation of the decimation and filtering stage is shown in Figure 4.18.

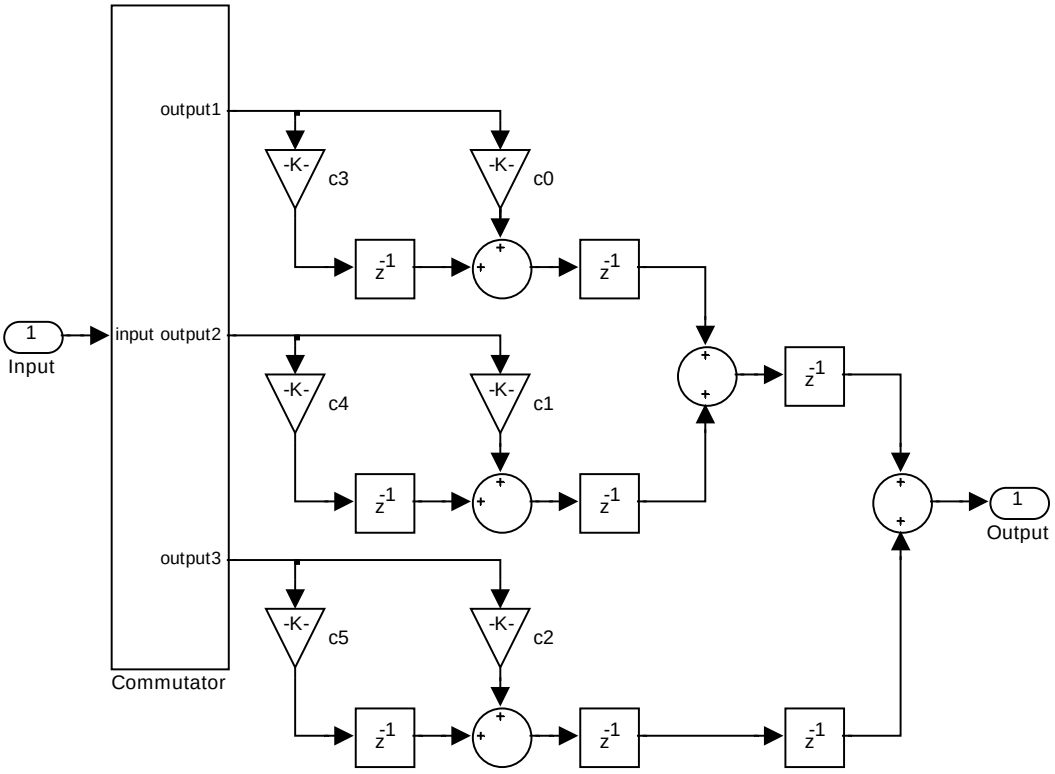


FIGURE 4.17: Simulink diagram of an FIR filter implementation for decimation by 3 with fully pipelined arithmetic

Decimation by 24 in 1 stage => 215th Order FIR Filter										
Category	Sub-type	Quantity	Width (n_d)	Depth / Width2	Utilisation %	Input Activity	Clock Activity	Output Activity	Equivalent Gate Count	Power	Comment
Adder (RCA)	Signed	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Unsigned	0	1-bit	x	100	10.000 MHz	x	10.000 MHz	0	0.00	
FIR1 MACAdd	Signed	192	28-bit	x		10.000 MHz	x	10.000 MHz	27264	18337.87	
FIR1 Poly Add	Signed	23	33-bit	x		10.000 MHz	x	10.000 MHz	3841	2587.94	
Multiplier	Dynamic	0	5-bit	4-bit	100	10.000 MHz	x	10.000 MHz	0	0.00	
	Constant	0	1-bit		100	10.000 MHz	x	10.000 MHz	0	0.00	
FIR1 Coef mlt	Dynamic	216	18-bit	7-bit		10.000 MHz	x	10.000 MHz	370440	116702.88	
Register	Latch	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
	DFF	0	1-bit	x	100	10.000 MHz	10.000 MHz	10.000 MHz	0	0.00	
FIR1 MACReg	DFF	192	28-bit	x		10.000 MHz	10.000 MHz	10.000 MHz	64512	6729.89	
FIR1 O/P Reg	DFF	1	33-bit			10.000 MHz	10.000 MHz	10.000 MHz	396	41.31	
			x	x							
								TOTAL =	466453	144399.89	µW

FIGURE 4.18: Power usage estimation FIR Filter

4.3 Chapter Conclusion

A power analysis tool has been developed and adapted to perform power dissipation and hardware resource utilization measurements for GNSS receivers. TSMC's 180nm components library was used to demonstrate the tool's performance and application, however the technology deployed can be easily changed. With the developed power analysis tool, the designer can estimate for a digital processing circuit how much power will be dissipated and how much resources will be required in a design without undertaking the detailed RTL level circuit design. Then individual GNSS receiver blocks were considered and their power consumption as well as hardware utilisation requirements were estimated.

Preliminary power analysis results show that most of the power is dissipated in the digital domain and it is dominated by the decimation part of the receiver chain as shown in Table 4.1. Table 4.1 shows a detailed power distribution and area utilisation in a tracking loop as well as in the decimation and filtering. As it can be seen from Table 4.1, the power dissipation in the tracking loop is much less than it is for the Decimation and Filtering stage. One main reason is that sampling rate at the decimation and filtering stage is much higher than it is in the tracking loop.

TABLE 4.1: Power Analysis in a GNSS Receiver

		Number of Gates	Power [μW]
Tracking	Acc & Dump	2820	514
	Carrier Loop Filter	9731	0.3
	Code Loop Filter	8103	0.2
	Carrier Discriminator	2330	0.9
	Code Discriminator	2227	1.5
	Carrier NCO	512	140
	Code NCO	796	18
Decimation and Filtering		2227	144400

Chapter 5

Decimating the GNSS Signal

After the power analysis tool was developed, the power dissipation and hardware complexity of the individual sub-blocks in the GNSS receiver were estimated as shown in Table 4.1. It was discovered that most of the power is dissipated at the decimation and filtering stage. This led to an investigation into the decimator and its associated operations in the GNSS receiver. This chapter investigated various decimation and filtering techniques for the GNSS receivers and presented the estimates of the associated power consumption.

5.1 Decimation

Decimation is the process of reducing the number of samples in an oversampled DT signal [53–56]. Decimation reduces the computational load of the following processing chain by reducing the number of samples to be processed as well as the processing rate,

making the hardware that does the downstream processing simpler, hence resulting in reduced computational complexity and lower power consumption [31, 57].

Decimation in GNSS receiver is used to decrease the sampling rate of the received GNSS signal as much as possible in order to reduce the computational burden in the subsequent blocks along the receiver chain. Figure 5.1 shows a generalised diagram for decimating a signal. As can be seen from the figure, the input signal needs to be filtered prior to being decimated in order to avoid aliasing due to sample rate reduction. Depending on the overall decimation ratio, as the number of stages increases the computational cost and the power dissipation reduces.

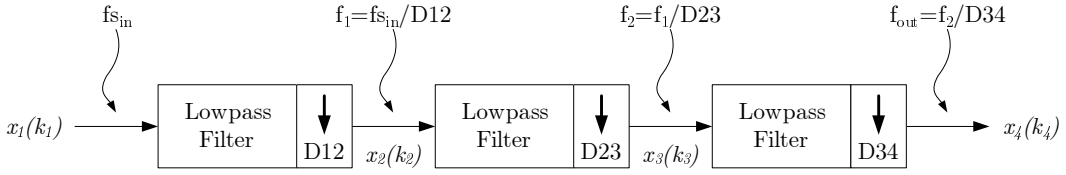


FIGURE 5.1: Decimating a signal

where fs_{in}, f_1, f_2 and f_{out} are the sampling frequencies at input, 1st stage, 2nd stage and output respectively. $D12$, $D23$ and $D34$ are the decimation ratios between 1st and 2nd stage, 2nd and 3rd stage, 3rd and 4th stage respectively. The relation between the decimation ratio and the input signal's bandwidth is as shown in equation 5.1.

$$B_{out} < \frac{D_{12}}{2} B_{in} \tag{5.1}$$

where $D12$, B_{in}, B_{out} are the decimation ratio between 1st stage and 2nd stage, the bandwidth of the input signal to be decimated and the bandwidth of the decimated output signal respectively.

According to this formula, if the input signal is not band limited, the decimation ratio should be less than half the bandwidth of the signal otherwise aliasing occurs.

After it has been realised that the highest power consumption is at the decimation and filtering part of the GNSS receiver, this led to an investigation to find out what type of filtering techniques are being used in the existing receivers. This investigation has led to a finding that all the GNSS receivers available in the market at the time of writing this thesis use only linear-phase FIR type of filters. The reason that they use FIR filters is because linear phase filters have constant group delay across all frequencies [54]. However, the overall delay is significantly greater than with a minimum-phase filter.

5.2 Decimating the GNSS Signal

After it has been established that all today's GNSS receivers use linear-phase FIR filter a study was carried out. The study involves investigating other alternatives to an FIR filter as well as using different combinations of decimation ratios in order to establish the effect of the filter types and the decimation ratio on the computational complexity and power dissipation. Then the filters were implemented using the VHSIC Hardware Description Language (VHDL) and tested on an FPGA in real-time with real-world signals, in order to establish the effects of these combinations on the positioning accuracy. The structures shown in this chapter were chosen specifically which results in efficient implementation on hardware. Also the FPGA implementation of filters are same as the structure. More information on the filter structure and their efficiency

are described in the following sections. Also the coefficients for the designed filters designed in this chapter are provided in Appendix A.

Since the filters will be implemented on an FPGA later on, the filter specifications have been chosen according to requirements of the test platform in order to be compatible. Table 5.1 summarises these specifications that are required to implement the filters.

Table 5.1: Decimation Properties

Property	**Value**
Decimation Ratio	24
Input Bandwidth	240.831 MHz
Output Bandwidth	10.034 MHz
Filter Bandwidth	4 MHz
Transition Bandwidth	1 MHz
Passband Ripple	2 dB
Stopband Attenuation	25 dB
Input Wordlength	7-bit
Output Wordlength	2-bit

The filters are designed to have 25 dB attenuation which matches the current receiver specification in order to be able to do a comparison [3]. Although different GNSS signals have different bandwidth, all the filters are designed to have a single-sided bandwidth of 4 MHz and are in a complex zero-IF receiver which gives a total 8 MHz bandwidth. This is to reduce the receiver computational complexity for the filtering part as well as the subsequent blocks. By using 4 MHz bandwidth filters, all the GNSS bands can be acquired.

It was realised that all the GNSS receivers use linear-phase FIR filters. Also some decimate the incoming signal using a single stage of decimation as opposed to multi-stage decimation. So a study was carried out where different filter types as well as different combination of multi-stage and single stage decimation is used.

5.2.1 Decimation with FIR filters

The first experiment was to use a linear phase FIR filter for decimation. Since the overall decimation ratio is fixed at 24, there are various possibilities. If the received signal is to be decimated in a single stage, the required FIR filter was used. If the experiment is to use multi-stage decimation, the first stage always used a slink filter. A slink filter is an N-point moving averager. Its z and frequency domain transfer functions are given in the equations 5.2 and 5.3 respectively [58–60].

$$H(z) = \left(\frac{1 - z^{-D}}{1 - z^{-1}}\right)^{n} \tag{5.2}$$

$$H(\nu) = slink^{n}\left(D, \nu\right).e^{-j2\pi\nu Dn} \tag{5.3}$$

where D, n and ν are the decimation ratio, the Slink filter order and the normalised frequency respectively.

The slink filter is very simple structure and requires no multipliers consequently it is a very low-power and low computational complexity alternative to other conventional filters which require multipliers for their filter coefficients. Therefore a slink lowpass filter has been used in the first stage of every decimation process in order to reduce power and computational complexity. The Simulink model of a second-order slink lowpass filter with a decimation ratio of 8 is given in Figure 5.2. The slink filter order, n, can be used in order to achieve required stopband attenuation. As the slink filter order is increase more stopband attenuation can be achieved however, pass roll-off will

also be increased. Figure 5.3 shows the frequency response of a second order Slink filter with D=8. The zeros of the Slink filter occurs at 1/Dth intervals therefore in this example the filter has notches at ν=0.125, 0.25, 0.375 and 0.5.

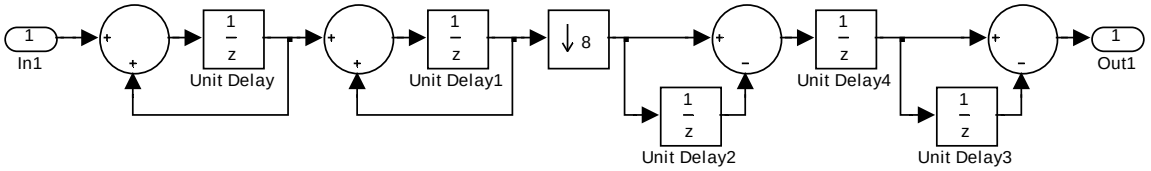


FIGURE 5.2: Simulink diagram of a second order Slink lowpass filter with D=8

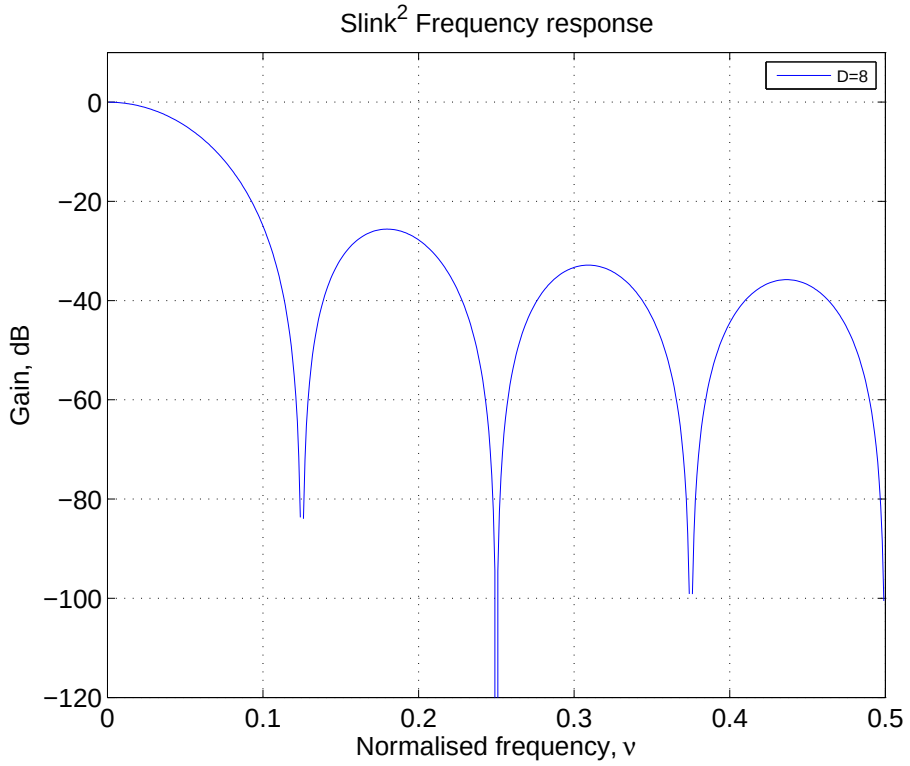


FIGURE 5.3: Frequency response of a second order Slink lowpass filter with D=8

Table 5.2 shows various combinations that has been used to filter the received signal using only linear phase FIR filters. In each combination, the first stage always has the highest decimation ratio in order to reduce the filter complexity and sample rate in the following stages.

TABLE 5.2: Possible Decimation Stages with FIR filters

Number of stages	**Decimation per stage**
3-stage	4 x 3 x 2
	6 x 2 x 2
2-stage	12 x 2
	8 x 3
	6 x 4
1-stage	24

The decimation filters were designed such that when implemented in real hardware they operate as efficiently as possible and use minimal hardware resources thus reducing power dissipation. To reduce the power dissipated by the decimation filters, all FIR filters were implemented using polyphase decomposition. Polyphase decomposition divides the filter into number of parallel paths operating at the lower output rate. The input samples are distributed to individual paths in turns. This reduction in the sampling rate of the filter reduces the power consumption [61]. Figure 5.4 shows an example of the decimation filter in which the decimation ratio is 3 which is designed in MATLAB/Simulink. As can be seen from the figure, the filter is decomposed into 3 paths by using a commutator switch. The input samples are distributed to each path which reduces the operating speed of the filter to 3 times the input sample rate. Furthermore, the FIR filters directly implement Time Delay and Accumulate (TDA) structure which places the registers in between the partial summation nodes as oppose to placing them along the input delay line. This has two advantages. The first advantage is that this type of architecture can operate at much higher speed than the counterpart, since the partial summation adders are pipelined. Second, placing a register at the output of the partial summation adder minimizes the bit transitions every time a input arrives to the adder. This also reduces the activity at the subsequent

adders as well as at the other components saving power even further.

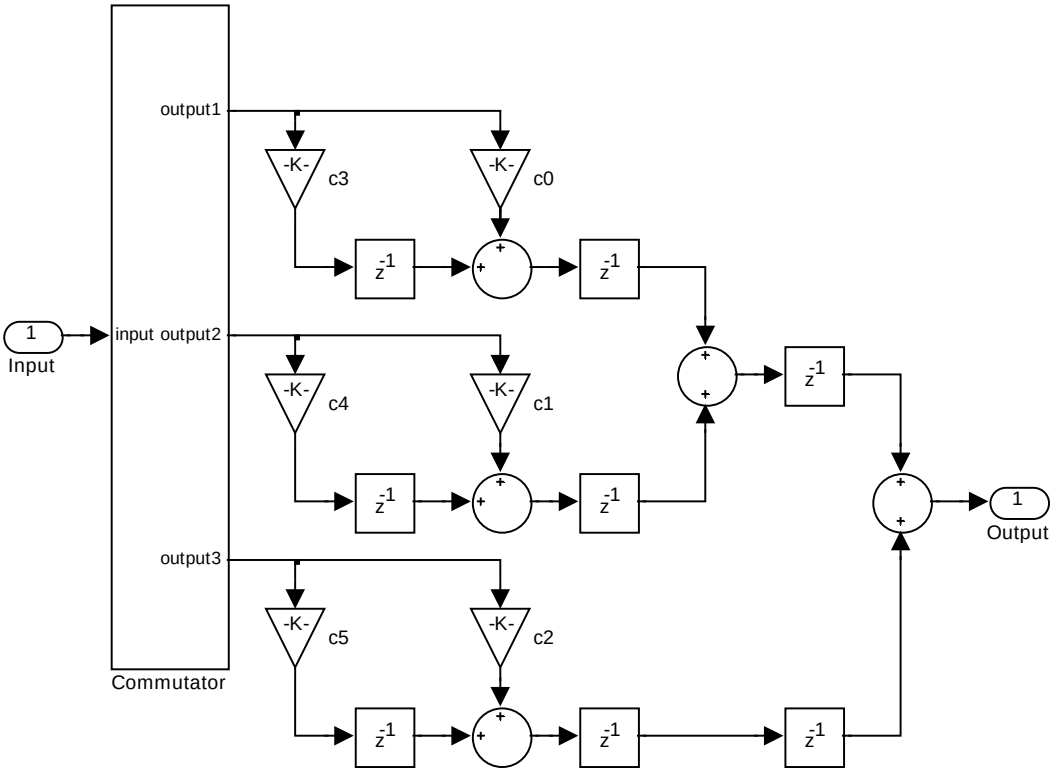


FIGURE 5.4: Simulink diagram of an FIR filter implementation for decimation by 3 with fully pipelined arithmetic

Decimation by 4 x 3 x 2 FIR

The first of decimation combinations to be considered, decimates first by 4, then 3 and finally 2, achieving an overall rate reduction of 24. This is a 3 stage decimator. The filters were first developed in a MATLAB environment and tested in order to assess if they comply with the necessary requirements using floating-point coefficients. Then

the coefficients were quantised to establish the minimum coefficient wordlength that meets the specification so converting the filter to fixed point arithmetic.

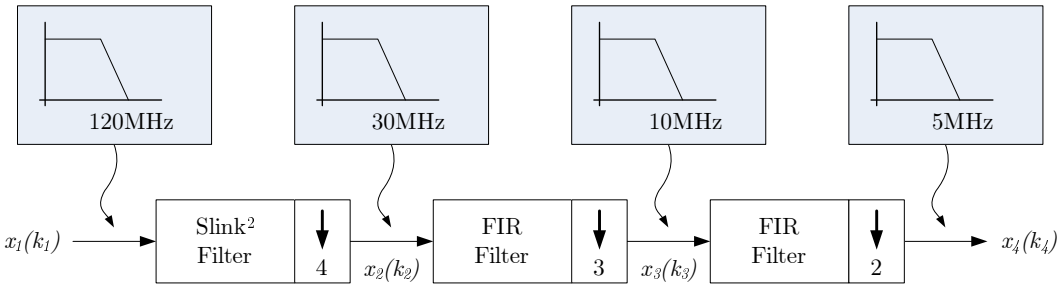


FIGURE 5.5: Decimation 4 x 3 x 2 and corresponding bandwidth by stages

Figure 5.5 shows the decimation by stages and the corresponding bandwidth at each stage. Figure 5.6 shows the responses of the filters for this particular decimation ratio combination in every stage. The properties of the filters are summarised in Table 5.3. As mentioned before, the first stage at the decimation process chain uses a slink filter of degree 2 which does not require any multipliers. Other subsequent stages uses linear-phase FIR filters. It can be seen from Table 5.3 that, although the passband ripple and stopband attenuation for the 2nd and 3rd stage FIR filters, 2nd stage filter order is lower than that of the 3rd stage. This is because the transition band at the second stage is much more relaxed than the transition band at the 3rd stage. Also the filter orders have been chosen carefully so that the number of coefficients is divisible by the decimation ratio at that particular stage. For example, the 2nd stage FIR filter is 5th order which means it has 6 coefficients and 2 filter coefficients are used per filter path.

TABLE 5.3: FIR Filter Properties for decimation 4 x 3 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	4	3	2
Filter type	Slink	FIR	FIR
Filter order	2	5	21
Passband ripple	N/A	0.8 dB	1 dB
Stopband attenuation	N/A	25 dB	25 dB
Coefficient wordlength	N/A	9 bits	9 bits
Area utilisation	82350 gates		
Power dissipation	31.7 mW		

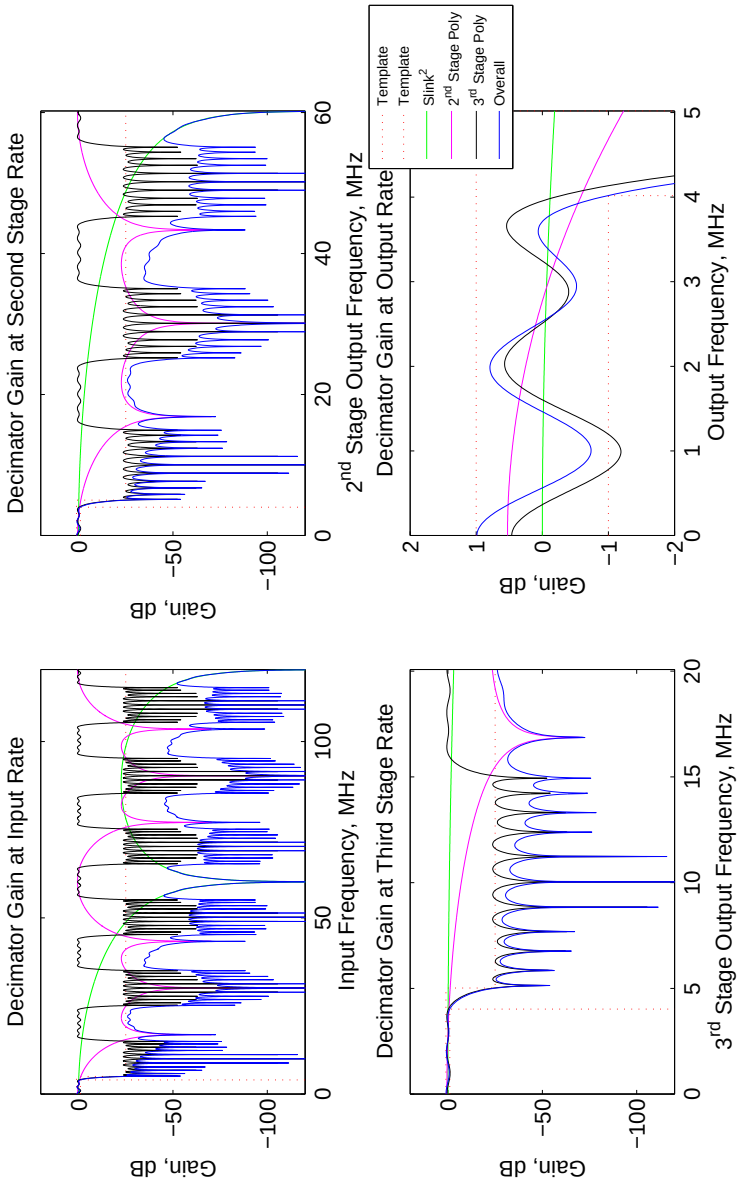


FIGURE 5.6: Overall Filter Response for decimation ratio 4 x 3 x 2 using FIR filters

Decimation by 6 x 2 x 2 FIR

Second on this list is also a 3 stage decimator which first decimates by a factor of 6 followed by 2 and 2. This time the 1st stage has a higher decimation ratio which means that the subsequent stages will operate at a lower sample rate compared with the previous case. The decimation ratios and the bandwidth at each stage is shown in Figure 5.7.

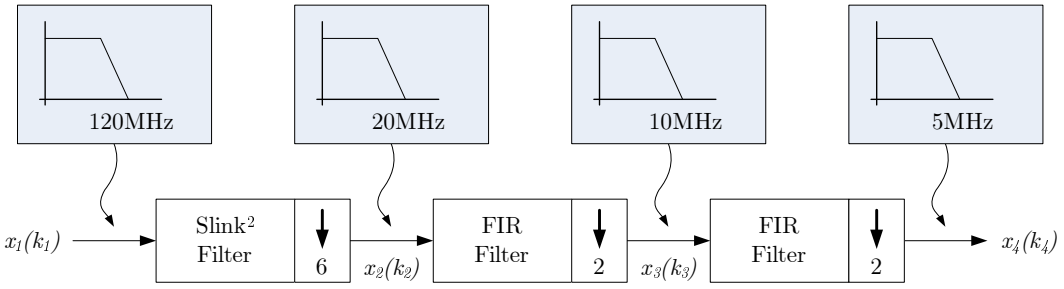


FIGURE 5.7: Decimation 6 x 2 x 2 and corresponding bandwidth by stages

The final filter response is shown in Figure 5.8. As can be seen from the figure, the overall filter fits into the template in every decimation stage. The properties of the filters used in this stage is summarised in Table 5.4.

TABLE 5.4: FIR Filter Properties for decimation 6 x 2 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	6	2	2
Filter type	Slink	FIR	FIR
Filter order	2	3	21
Passband ripple	N/A	0.8 dB	1 dB
Stopband attenuation	N/A	26 dB	25 dB
Coefficient wordlength	N/A	9 bits	9 bits
Area utilisation	82828 gates		
Power dissipation	31.3 mW		

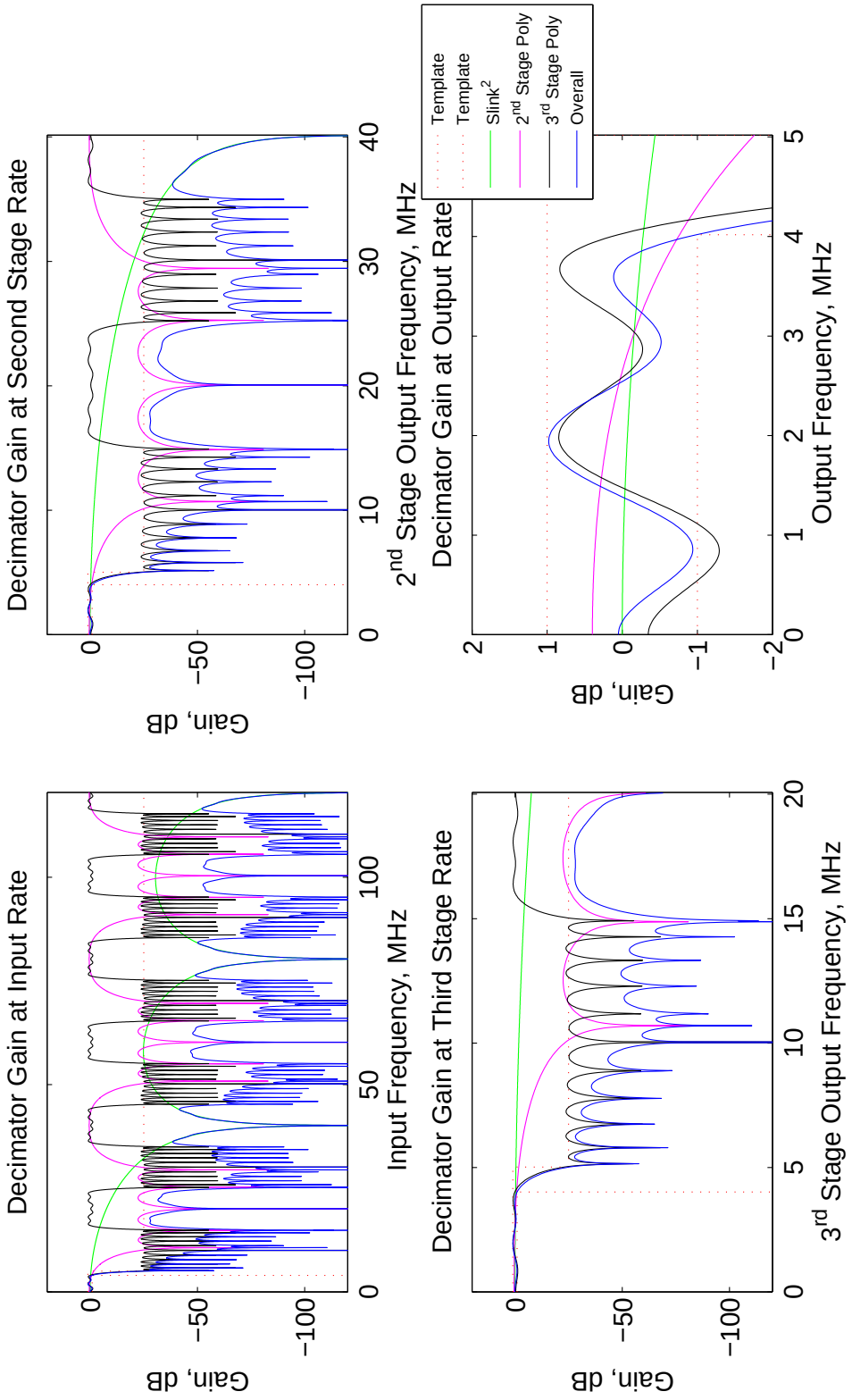


FIGURE 5.8: Overall Filter Response for decimation ratio 6 x 2 x 2 using FIR filters

Decimation by 12 x 2 FIR

Decimation by a factor of 12 followed by 2 requires only 2 stages. This time the 1st stage has the highest decimation ratio of 12 which means that the 2nd stage will operate at its lowest sampling rate compared with other combinations. The decimation ratios and the bandwidth at each stage is shown in Figure 5.9.

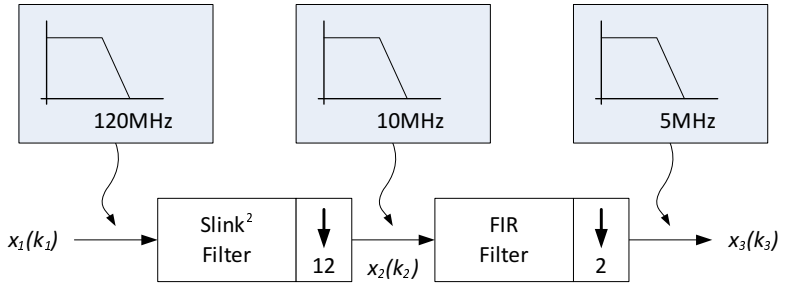


FIGURE 5.9: Decimation 12 x 2 and corresponding bandwidth by stages

The final filter response is shown in Figure 5.10. As can be seen from the figure, the overall filter fits into the template in every decimation stage. The properties of the filters used in this stage is summarised in Table 5.5. It should be noted from Figure 5.10 that the second stage filter response is plotted up to twice the Nyquist frequency. This is done in order to ensure that the frequencies beyond Nyquist are still within the template otherwise once decimated, aliasing will take place. Not surprisingly this decimation combination has the lowest power dissipation for FIR filters as can be seen from the Table 5.5.

TABLE 5.5: FIR Filter Properties for decimation 12 x 2

	1st Stage	**2nd Stage**
Decimation ratio	12	2
Filter type	Slink	FIR
Filter order	2	21
Passband ripple	N/A	1.8 dB
Stopband attenuation	N/A	20 dB
Coefficient wordlength	N/A	9 bits
Area utilisation	51175 gates	
Power dissipation	19.3 mW	

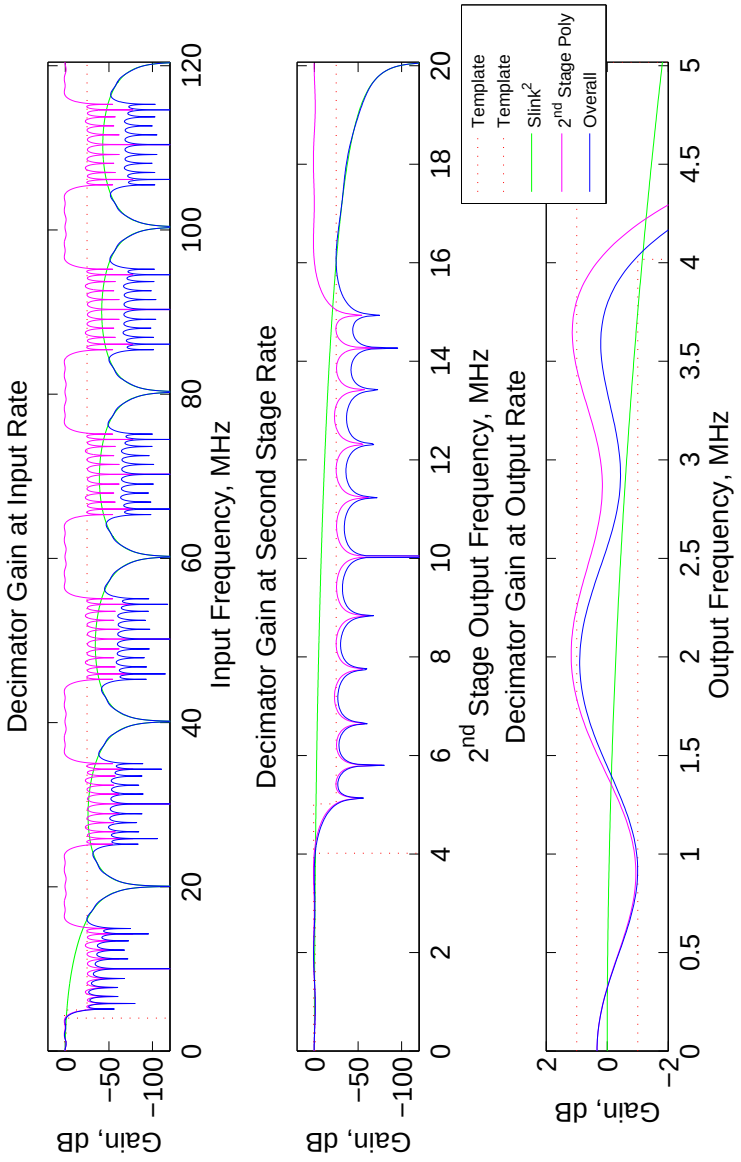


FIGURE 5.10: Overall Filter Response for decimation ratio 12 x 2 using FIR filters

Decimation by 8 x 3 FIR

An alternative 2-stage decimator uses the decimation ratios of 8 followed by 3. This time the 1st stage has a decimation ratio of 8 which means that the 2nd stage filter will also operate at its lowest sampling rate compared with other combinations. The decimation ratios and the bandwidth at each stage is shown in Figure 5.11.

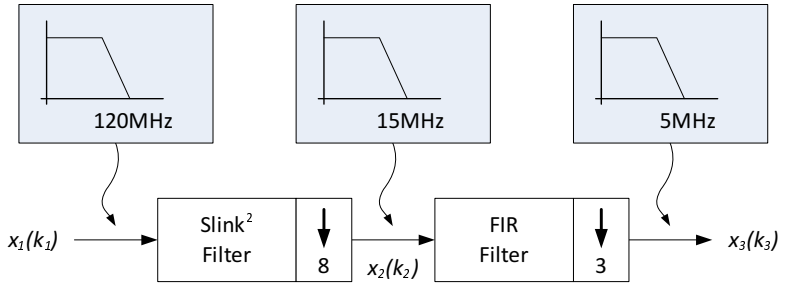


FIGURE 5.11: Decimation 8 x 3 and corresponding bandwidth by stages

The final filter response is shown in Figure 5.12. As can be seen from the figure, the overall filter fits into the template at every decimation stage. The properties of the filters used in this stage is summarised in Table 5.6. It should be noted from the Figure 5.12 that the second stage filter response is plotted up to twice Nyquist. This is done in order to make sure that the frequencies beyond Nyquist are still within the template otherwise once decimated aliasing will take place.

TABLE 5.6: FIR Filter Properties for decimation 8 x 3

	1st Stage	**2nd Stage**
Decimation ratio	8	3
Filter type	Slink	FIR
Filter order	2	29
Passband ripple	N/A	1.27 dB
Stopband attenuation	N/A	26.5 dB
Coefficient wordlength	N/A	9 bits
Area utilisation	52382 gates	
Power dissipation	22.6 mW	

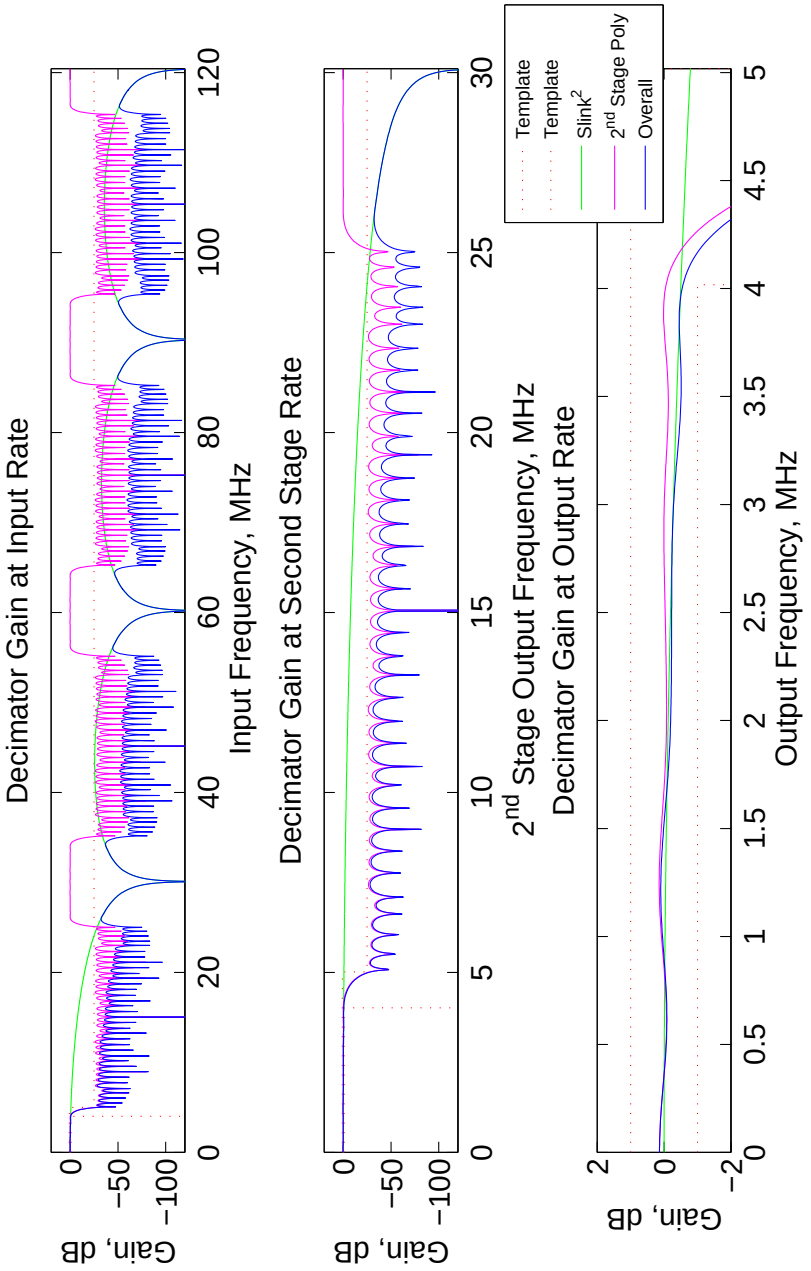


FIGURE 5.12: Overall Filter Response for decimation ratio 8 x 3 using FIR filters

Decimation by 6 x 4 FIR

The third candidate for 2-stage decimator is to decimate by 6 followed by a decimation ratio of 4. This time the 1st stage has a decimation ratio of 6 which means that the 2nd stage filter will also operate at the output rate compared with other combinations by using the polyphase decomposition property. The decimation ratios and the bandwidth at each stage is shown in Figure 5.13.

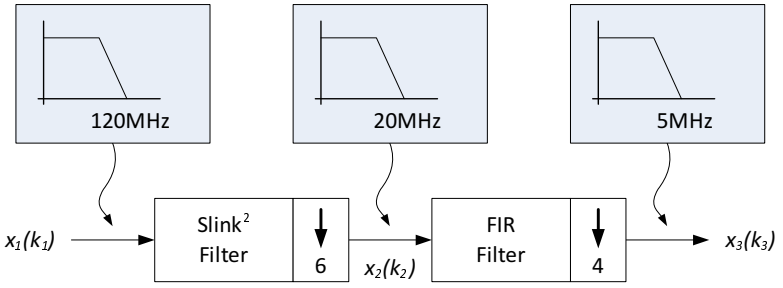


FIGURE 5.13: Decimation 6 x 4 and corresponding bandwidth by stages

The overall filter response is shown in Figure 5.14. As can be seen from the figure, the overall response fits into the template in every decimation stage. The properties of the filters used in this stage is summarised in Table 5.7. It should be noted from the Figure 5.14 that the second stage filter response is plotted up to twice the Nyquist. This is done in order to make sure that the frequencies beyond Nyquist are still within the template otherwise once decimated aliasing will take place. It should also be noted that this decimation combination for FIR filters has the lowest power dissipation as can be seen from Table 5.7.

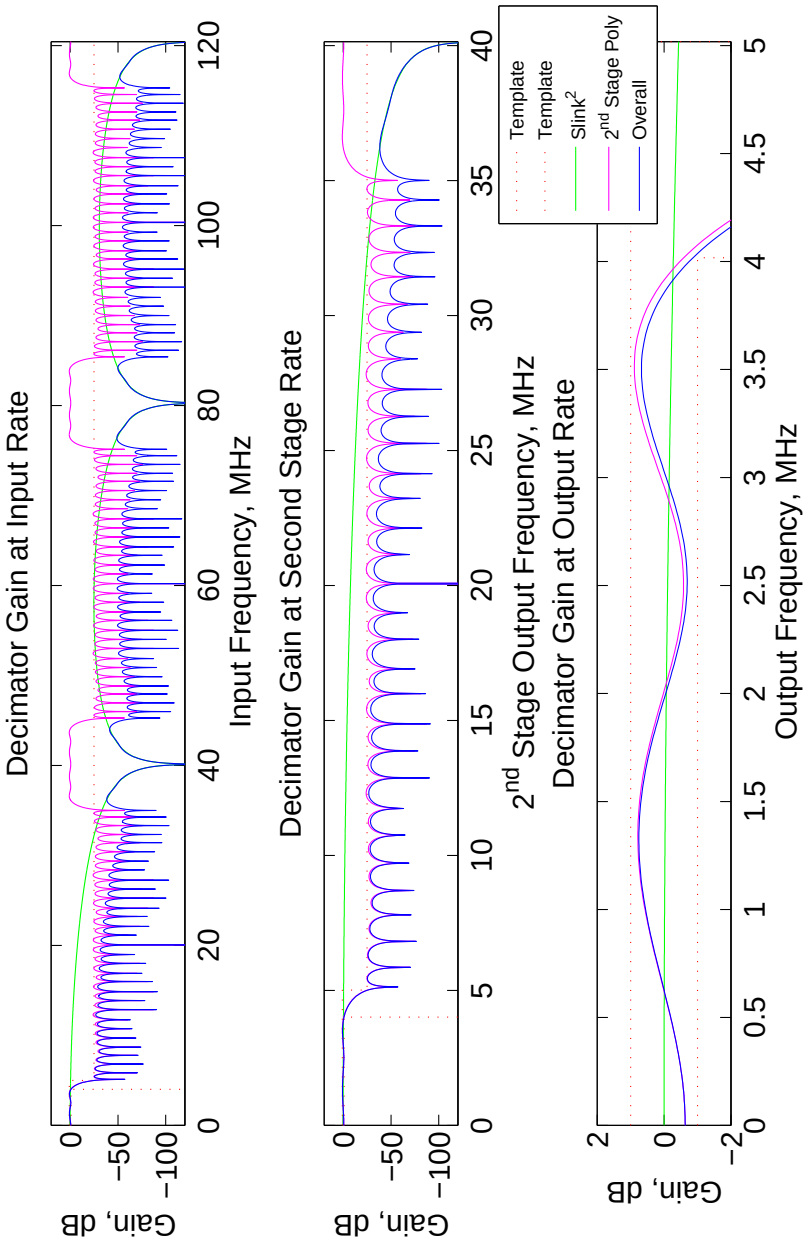


FIGURE 5.14: Overall Filter Response for decimation ratio 6 x 4 using FIR filters

TABLE 5.7: FIR Filter Properties for decimation 6 x 4

	1st Stage	**2nd Stage**
Decimation ratio	6	4
Filter type	Slink	FIR
Filter order	2	39
Passband ripple	N/A	1.27 dB
Stopband attenuation	N/A	26.5 dB
Coefficient wordlength	N/A	9 bits
Area utilisation	82208 gates	
Power dissipation	28.7 mW	

Decimation by 24 FIR

Perhaps the most obvious decimation is to perform it in a single stage by a factor of 24. In this case, there is no slink filter before the FIR filters but the input signal is filtered with an FIR filter straight away. The decimation ratios and the bandwidth at each stage is shown in Figure 5.15.

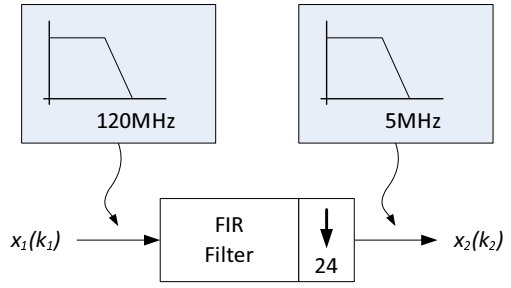


FIGURE 5.15: Decimation 24 and corresponding bandwidth by stages

As can be seen from the Figure 5.8, the filter order for this decimation is much higher than it is for the other FIR filters reported previously. This is because the filter's transition bandwidth is very narrow relative to the sampling frequency. This results in a much higher filter order than the other approaches which increases the computational complexity and subsequently the power dissipation. The power dissipation and the area

utilisation estimation reported in Table 5.8 confirms the expected very high hardware utilisation and high power consumption.

TABLE 5.8: FIR Filter Properties for decimation 24

	1st Stage
Decimation ratio	24
Filter type	FIR
Filter order	215
Passband ripple	2 dB
Stopband attenuation	25 dB
Coefficient wordlength	18 bits
Area utilisation	466453 gates
Power dissipation	144.4 mW

5.2.2 Decimation with IIR filters

The second investigation was to use a minimum-phase IIR filter in the decimation process. IIR filters have a non-linear phase response but in return they can filter a signal with much reduced filter order for the same performance compared with FIR filters. This means that implementing an FIR equivalent IIR filter requires much less computational complexity and reduced power consumption.

The same 2-stage and 3-stage decimation ratios that have been reported in the previous section with the FIR filters have been repeated here with an IIR equivalent filter. Similar to decimation with the FIR filters, a slink lowpass filter was used as the first stage decimation filter for the reasons mentioned in the previous section.

The IIR filters designed for this application were based on a Allpass based Polyphase structures. This is because the feedback inherent in conventional IIR filters do not allow the computational savings inherent in the feedback process. This is also because

they offer very effective filter implementation using minimum number of coefficients and they are less prone to coefficient quantisation. Also they have very small passband ripples [62], [63], [64]. Furthermore, Numerator-Denominator (ND) Tapped Delay Line (TDL) based Allpass structure is used since it offers the minimum dynamic growth [65]. Because of the output in the IIR filter the datapath should be quantised in order to limit the infinite data growth. But quantisation introduces noise therefore the amount of noise that will be introduced to the system needs to be calculated. For this research the noise floor for all the IIR filters was chosen to be around -80dB which would be sufficient. The number of guard bits are calculated for each filter in order to make sure that the internal arithmetic does not overflow. This is estimated using L1-norm which is defined as given in Equation 5.4 [66].

$$L_{1,n} = \sum_{k=0}^{\infty} |h_n(k)| \tag{5.4}$$

where $h_n(k)$ is the impulse response between the input and the nth node of the filter.

Decimation by 4 x 3 x 2 IIR

Again the first stage is a slink decimator. A second order slink filter was sufficient for the first stage decimation. Then it followed by an IIR lowpass filter with a decimation ratio of 3. For the second stage IIR filter a non-halfband filter structure had to be used since the decimation ratio is not 2. This means the filter structure cannot take the advantage of the polyphase decomposition. Therefore the filter has to operate at the

input rate rather than the output rate. The Figure 5.16 shows the IIR filter structure used. The structure shares the feedforward delay registers for the polyphase upper and lower branch in order to minimize the hardware usage. Also the filter has to operate at the input sample rate and it is at the output that the sample rate is reduced. This disadvantage causes the filter to dissipate more power. Also the "convert" blocks are the rounders used in order to limit the data path bit growth due to the feedback. The rounding method used all throughout was convergent rounding which gives the best performance in terms of d.c. offset and quantisation noise.

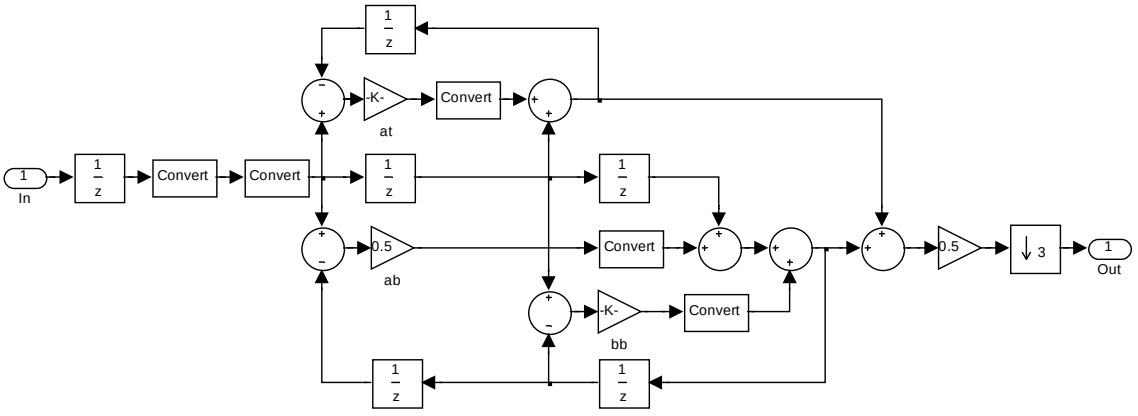


FIGURE 5.16: Simulink model of IIR filter for 2nd stage decimation

However, since the 3rd stage decimation ratio is 2 the filter cut-off is at half-Nyquist (ν_c=0.5, f_c=f_s/4). Because the halfband filters' cut-off frequency is at half-Nyquist, they are used wherever decimation ratio is 2. Also the lowpass filter can work at the output rate. The simulink block diagram is shown in Figure 5.17.

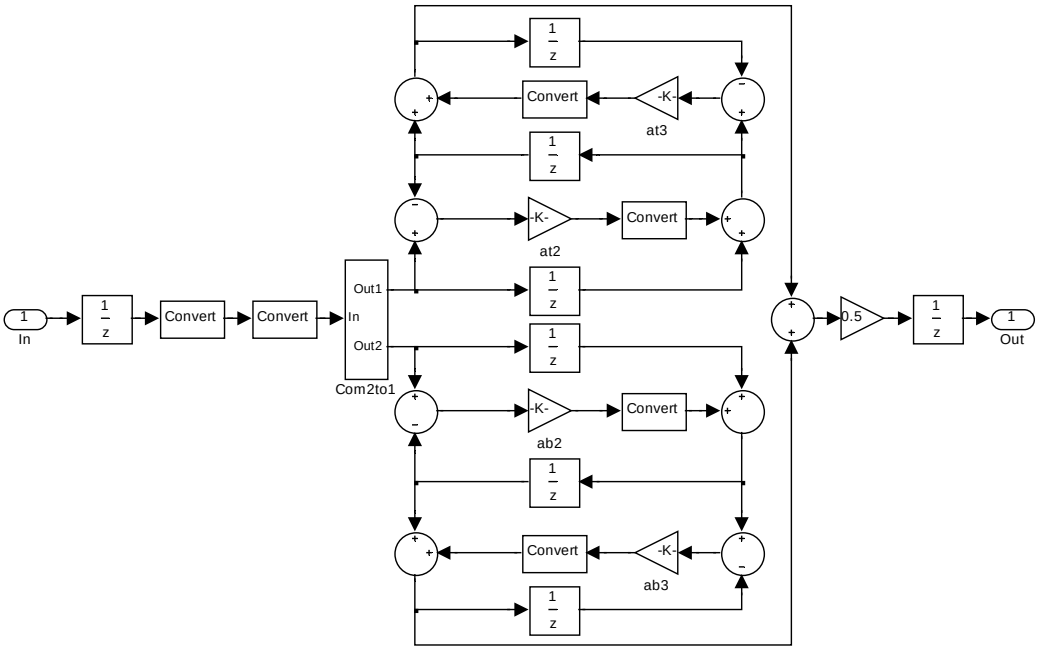


FIGURE 5.17: Simulink model of IIR filter for 3rd stage decimation

As can be seen from Figure 5.17, the data at the input is distributed by using a 2-way commutator and the filter's sampling rate is halved. The overall decimation filter response for this particular case is given in Figure 5.18.

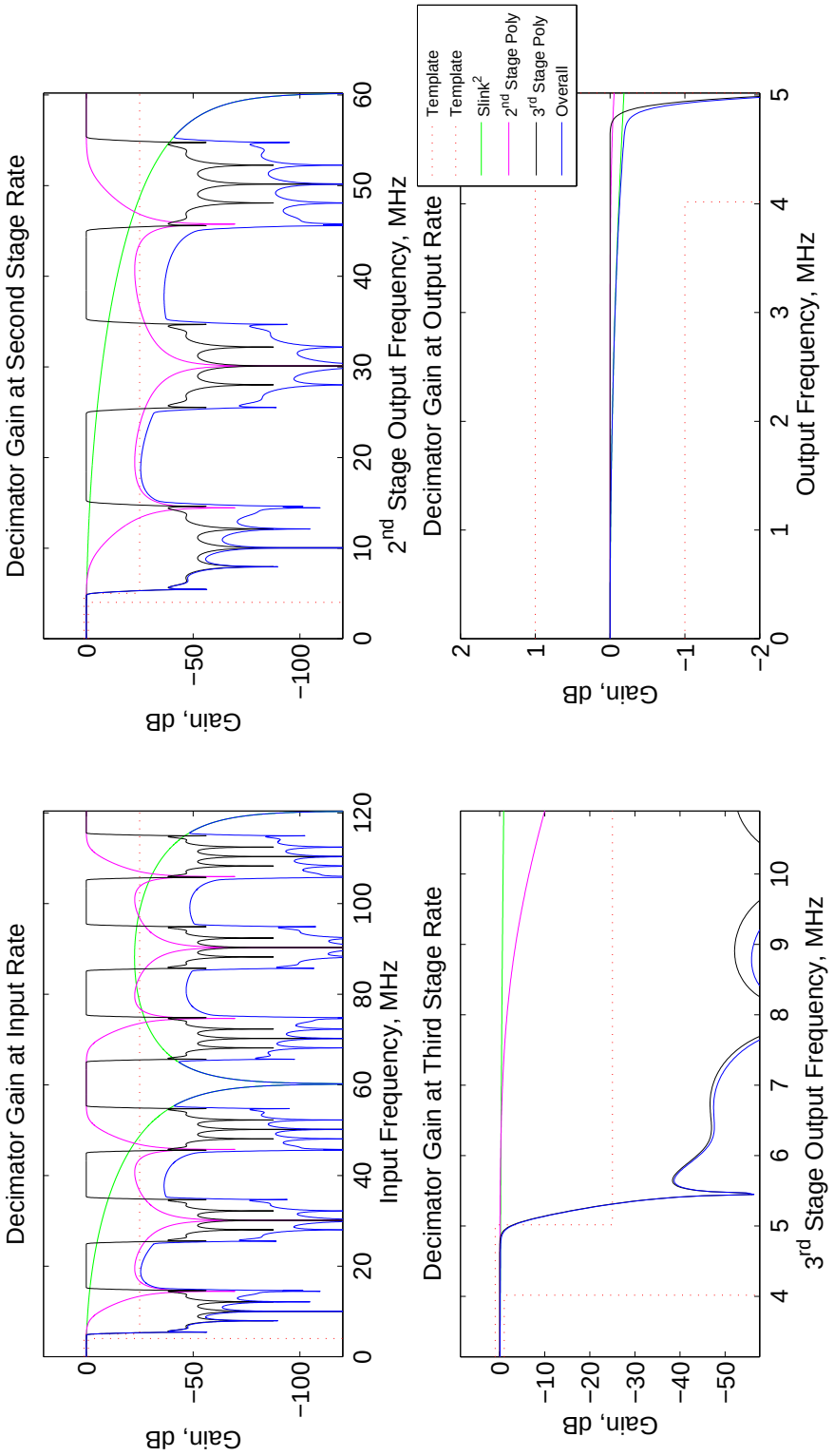


FIGURE 5.18: Overall Filter Response for decimation ratio 4 x 3 x 2 using IIR filters

Generally the Slink filter distorts the passband response because of their roll-off response at their passband and this is usually compensated at the final decimation stage. However, since the Polyphase IIR filters have very small passband ripples, the final output does not need to be compensated, it is still within the required template. But as can be seen from the left bottom subplot of Figure 5.18, the overall stopband goes beyond the required cut-off frequency. This is a limitation due to the fact that halfband polyphase filters have a fixed cut-off at half Nyquist. When decimated, any frequencies beyond half Nyquist will fold back into the passband causing aliasing. However the filter violates the requirement by only 300 kHz which means only the frequencies beyond 4.7 MHz will be contaminated with the alias signal. Since the band of interest is up to 4 MHz this aliasing does not cause any performance degradation to the filtered data. The filter properties are shown in Table 5.9. As can be seen from the table, the power dissipation for this decimation combination using IIR filter is the lowest so far.

TABLE 5.9: IIR Filter Properties for decimation 4 x 3 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	4	3	2
Filter type	Slink	IIR	IIR
Filter order	2	4	5
Passband ripple	N/A	0.007 dB	0.007 dB
Stopband attenuation	N/A	25 dB	26 dB
Coefficient wordlength	N/A	4 bits	7 bits
Area utilisation	11374 gates		
Power dissipation	12.4 mW		

Decimation by 6 x 2 x 2 IIR

The second decimator considers decimation by 6 then 2 and 2 again. It starts with slink decimator. Here a second order Slink filter was sufficient as well for the first

stage decimation. Then it followed by an IIR lowpass filter with a decimation ratio of 2. Unlike the previous case, since the decimation ratio for the 2nd and 3rd stage decimation ratios are 2, a halfband allpass based structure is deployed in order to take the advantage of operating the filters at the output rate which is twice as slow as the input rate. Figures 5.19 and 5.20 show the IIR filter structure used for the 2nd stage and 3rd stage decimation filtering respectively. As can be seen from both the figures, the 2nd stage filter complexity is less than the 3rd stage filter's complexity. This is due to the fact that 2nd stage filtering requirements are more relaxed in the transition band compared with the final stage.

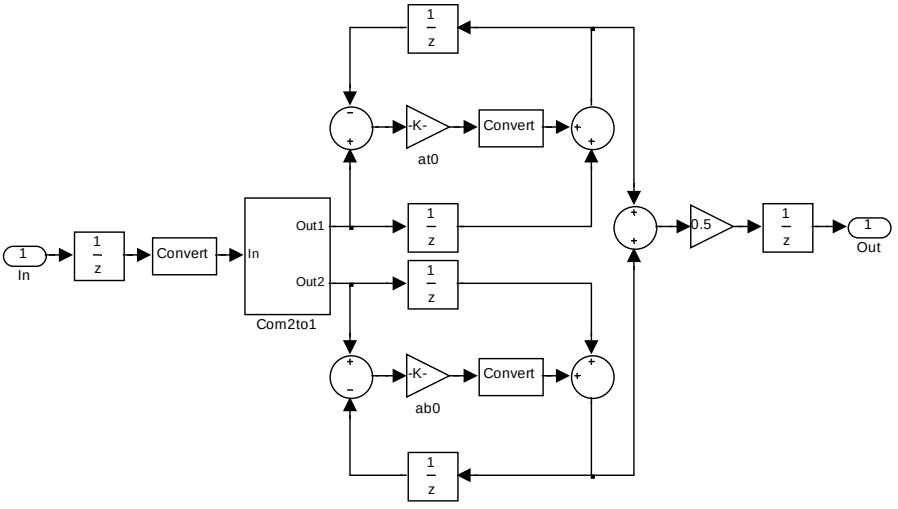


FIGURE 5.19: Simulink model of IIR filter for 2nd stage decimation

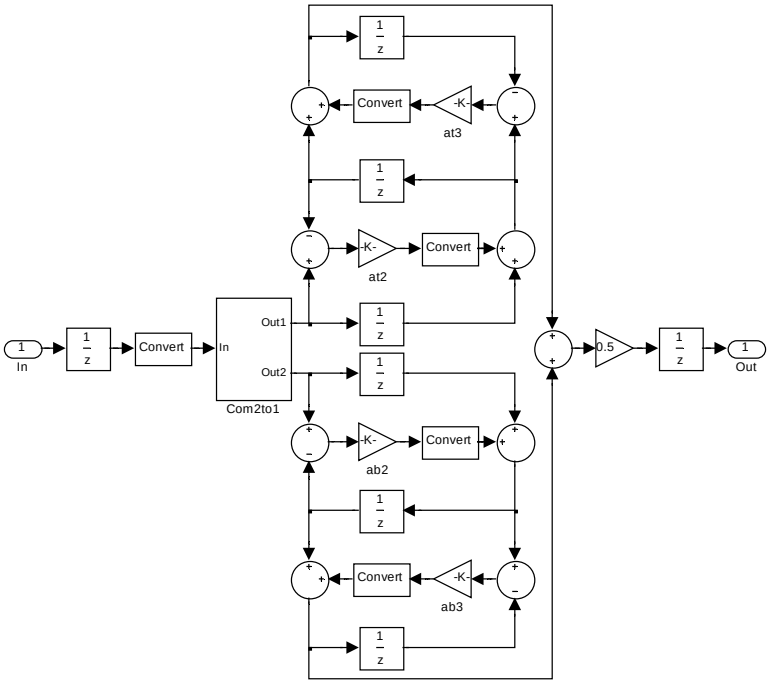


FIGURE 5.20: Simulink model of IIR filter for 3rd stage decimation

Finally the overall filter response in each decimation stages has been given in Figure 5.21. As explained in the previous case the aliasing is present here as well. However, since it is in the transition band there is no need for an extra filtering at the output. Also slink filter roll-off compensation is not required because the overall passband is within the given specification. The filter properties are summarised in Table 5.10.

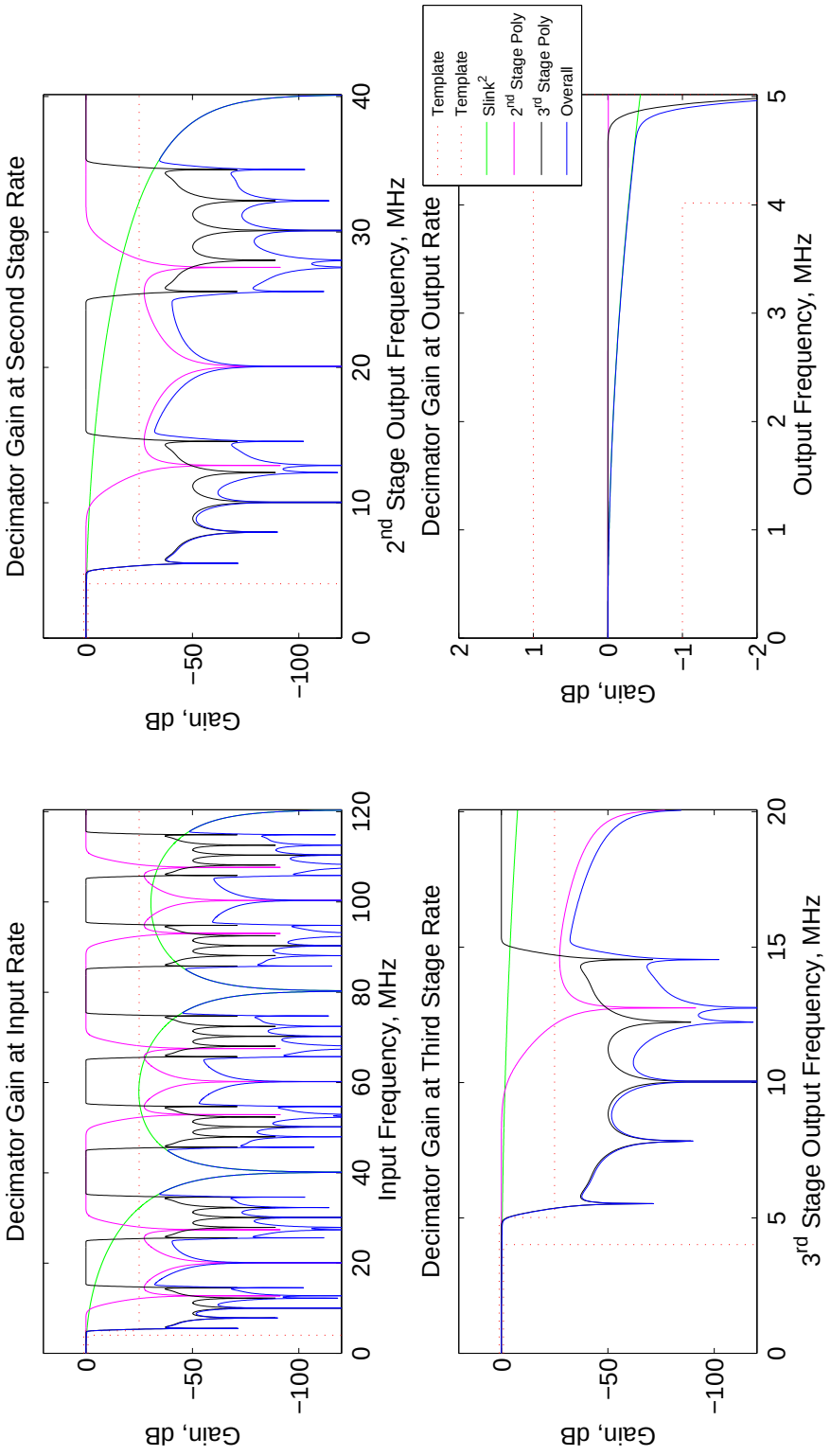


FIGURE 5.21: Overall Filter Response for decimation ratio 6 x 2 x 2 using IIR filters

TABLE 5.10: IIR Filter Properties for decimation 6 x 2 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	6	2	2
Filter type	Slink	IIR	IIR
Filter order	2	5	9
Passband ripple	N/A	<0.1 dB	<0.1 dB
Stopband attenuation	N/A	25 dB	26 dB
Coefficient wordlength	N/A	4 bits	4 bits
Area utilisation	12169 gates		
Power dissipation	7.9 mW		

Decimation by 12 x 2 IIR

The third option considered was a 2-stage decimator. It starts with slink decimation reducing the rate by 12 followed by a reduction by 2. This time a second order Slink filter was not sufficient to filter out the out-of-band signals before the downsampling process therefore the a 3rd order Slink filter had to be deployed. Then it followed by an IIR lowpass filter with a decimation ratio of 2. Here, a halfband allpass based structure is also deployed in order to take the advantage of operating the filters at the output rate which is half the input rate. Figure 5.22 shows the IIR filter structure used for the 2nd stage decimation filtering.

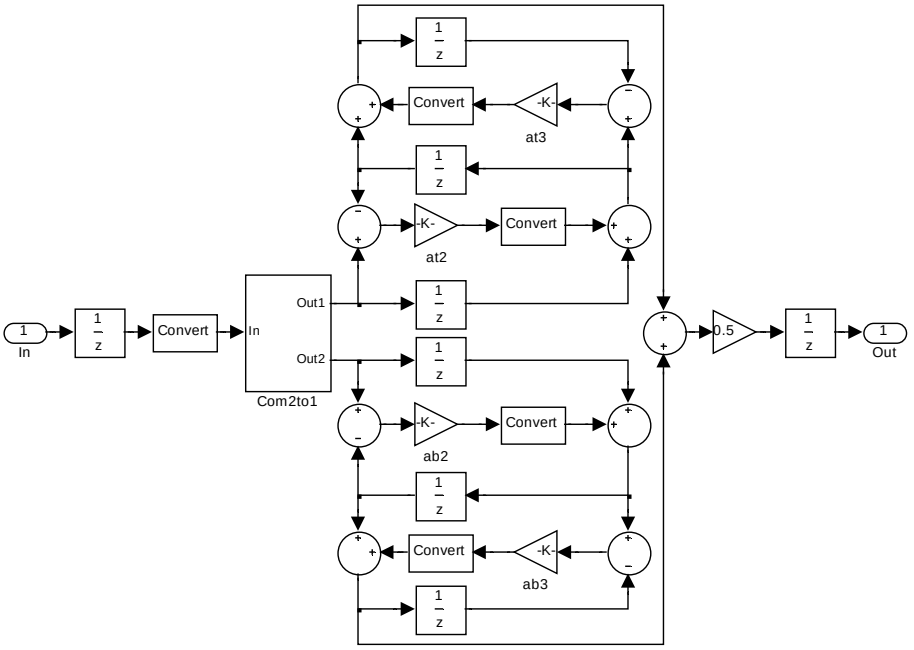


FIGURE 5.22: Simulink model of IIR filter for 2nd stage decimator

The overall filter response in each decimation stages is given in Figure 5.23. As explained in the previous case, the aliasing is present here as well. However, since it is in the transition band there is no need for an extra filtering at the output. However, a Slink filter roll-off compensation is required because the overall passband ripples goes higher than the required specification. This is because, since the slink filter order is higher, the passband roll-off is sharper as well. Figure 5.24 shows the structure used in order to compensate the slink filter roll-off [67]. The slink roll-off compensator's frequency response is also given in 5.25. Slink filter roll-off is compensated at the output of the final stage where the sampling rate is lower than the other stages in order to reduce the power consumption. The filter properties are summarised in Table 5.11.

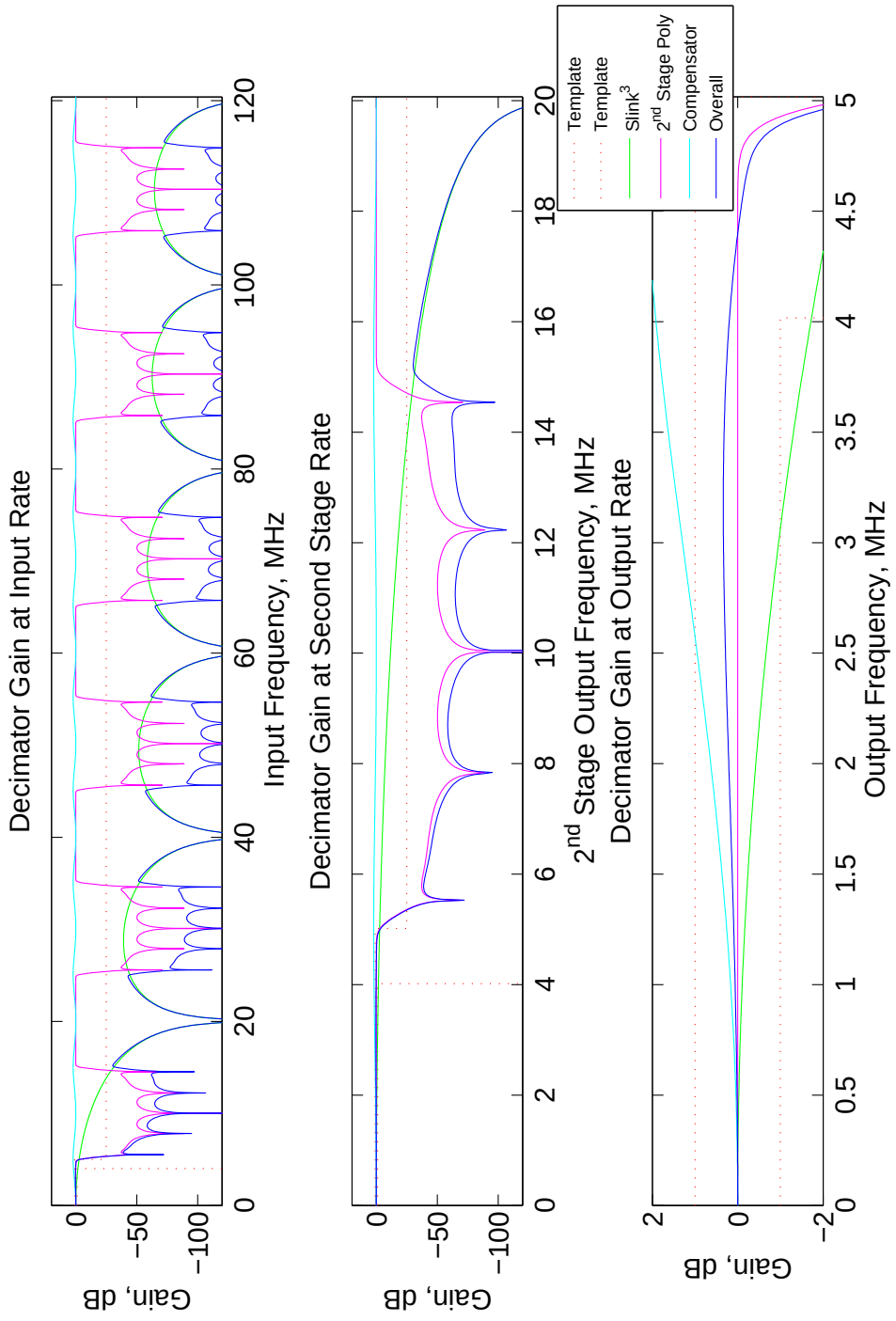


FIGURE 5.23: Overall Filter Response for decimation ratio 12 x 2 using IIR filters

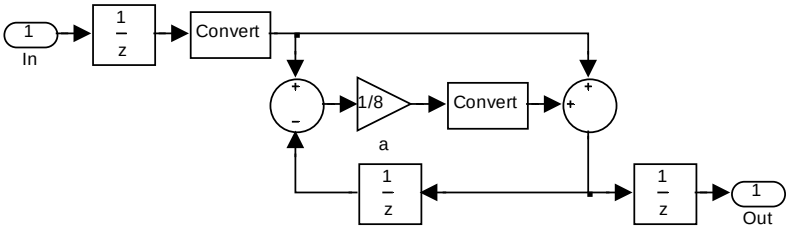


FIGURE 5.24: Simulink model of the structure used to compensate the Slink roll-off

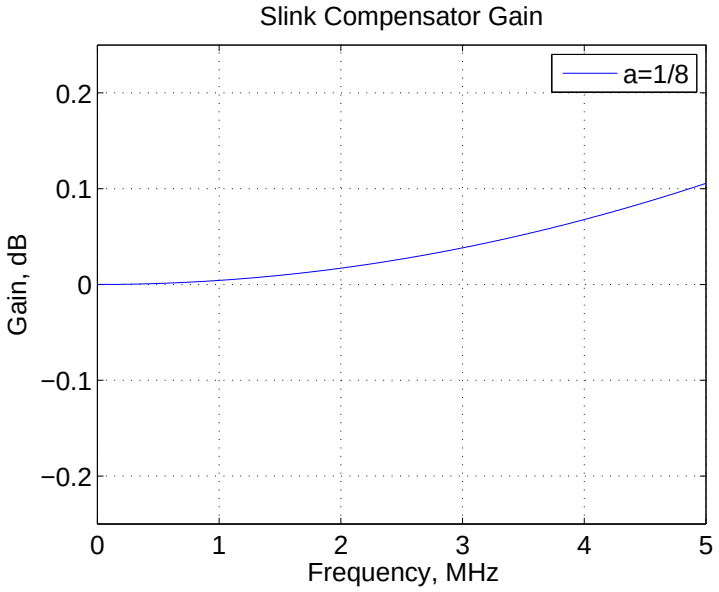


FIGURE 5.25: The frequency response of the Slink roll-off compensator

TABLE 5.11: IIR Filter Properties for decimation 12 x 2

	1st Stage	**2nd Stage**
Decimation ratio	12	2
Filter type	Slink	IIR
Filter order	3	9
Passband ripple	N/A	<0.5 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	4 bits
Area utilisation	9828 gates	
Power dissipation	9.3 mW	

Decimation by 8 x 3 IIR

The fourth option was another 2-stage decimation combination with a first stage slink decimator reducing the rate by 8 followed by a second stage reducing the rate by 3. A second-order slink filter was sufficient to filter out the out-of-band signals before the downsampling process. Then it followed by an IIR lowpass filter with a decimation ratio of 3. Here, as mentioned previously, since the decimation ratio 3, a non-halfband allpass based structure had to be used. Consequently the second stage filter had to operate at the input rate rather than the output rate which increases the power consumption. But it still dissipated less power than the most power efficient FIR filter counterpart due to the efficient filter structures deployed. Figure 5.26 shows the IIR filter structure used for the 2nd stage decimation filtering.

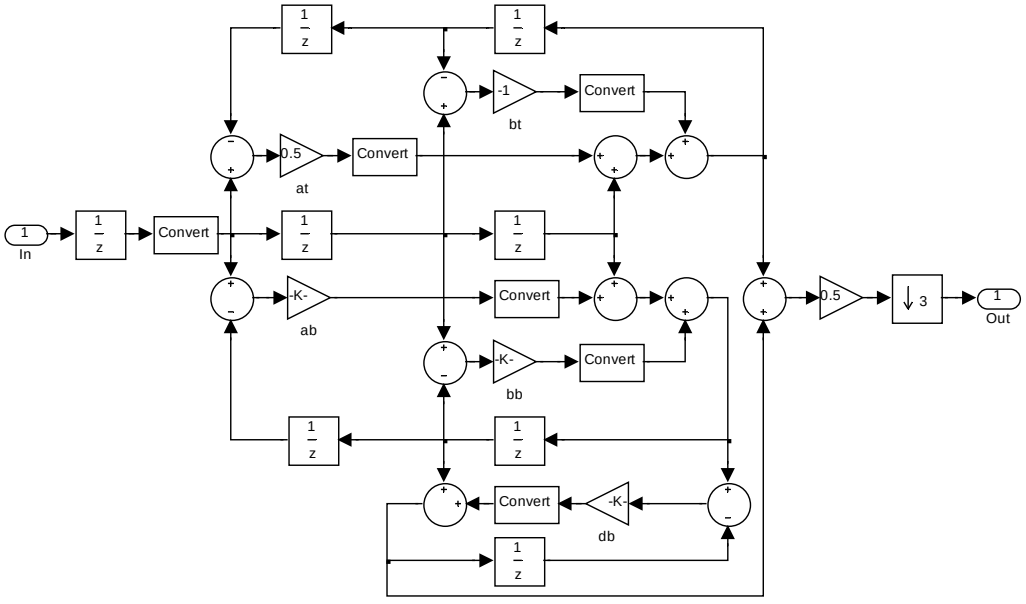


FIGURE 5.26: Simulink model of IIR filter for 2nd stage decimation

The overall filter response in each decimation stages is given in Figure 5.27. Here since a non-halfband structure is used, the filter's cut-off frequency can be adjusted to the

required frequency therefore aliasing does not occur. A slink filter roll-off compensator is not required either. The filter properties are summarised in table 5.12.

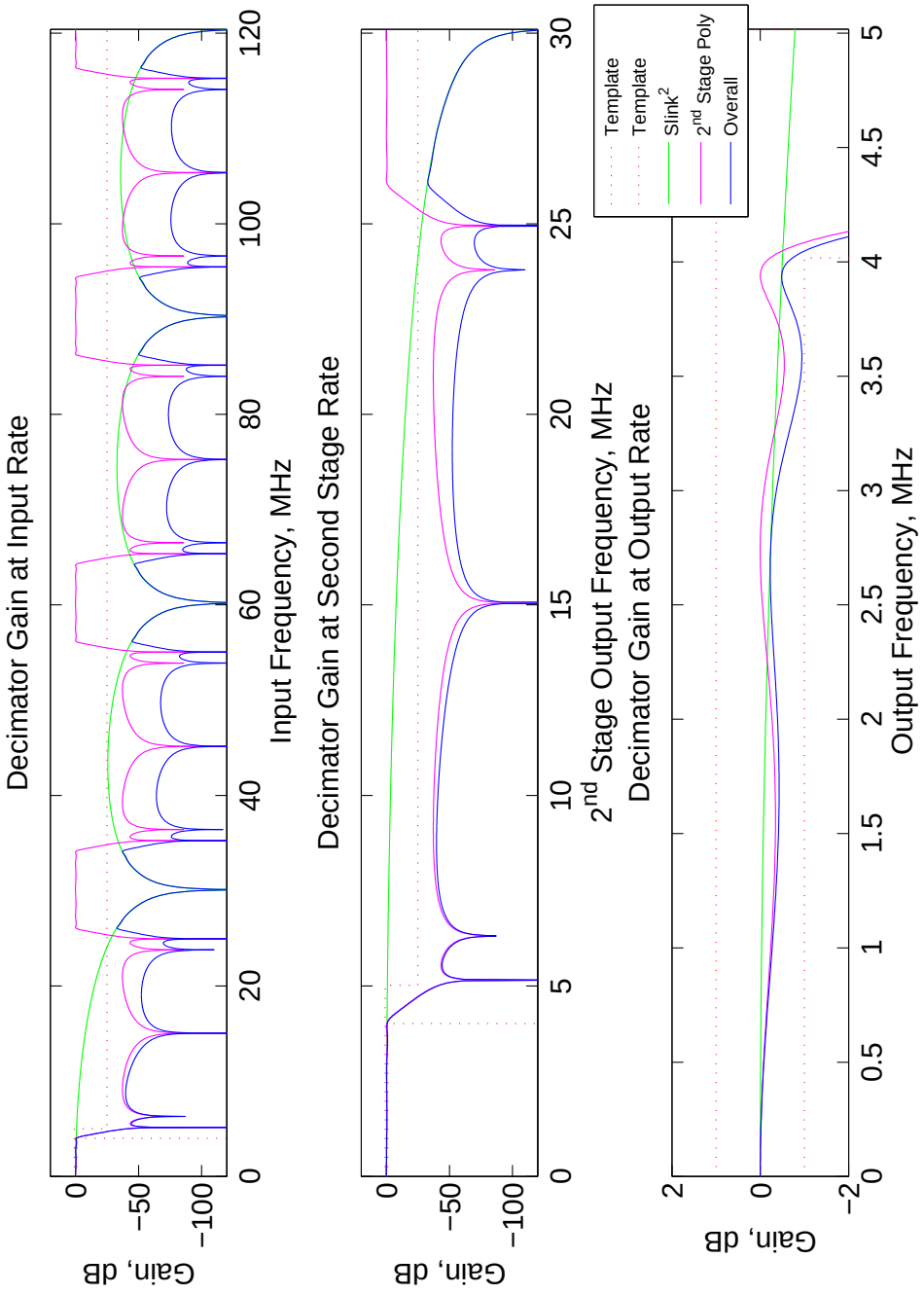


FIGURE 5.27: Overall Filter Response for decimation ratio 8 x 3 using IIR filters

TABLE 5.12: IIR Filter Properties for decimation 8 x 3

	1st Stage	**2nd Stage**
Decimation ratio	8	3
Filter type	Slink	IIR
Filter order	2	10
Passband ripple	N/A	1 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	6 bits
Area utilisation	9585 gates	
Power dissipation	11.3 mW	

Decimation by 6 x 4 IIR

The fifth option was another 2-stage decimation combination of 6 followed by 4 starting with slink decimator. A second-order Slink filter was sufficient to filter out the out-of-band signals before the downsampling process. Then it is followed by an IIR lowpass filter with a decimation ratio of 4. Here, as mentioned previously, since the decimation ratio 4, a non-halfband allpass based structure had to be used. Since a non-halfband allpass based structure is used the 2nd stage filter had to operate at the input rate rather than the output rate which increases the power consumption. Figure 5.28 shows the IIR filter structure used for the 2nd stage decimation filtering.

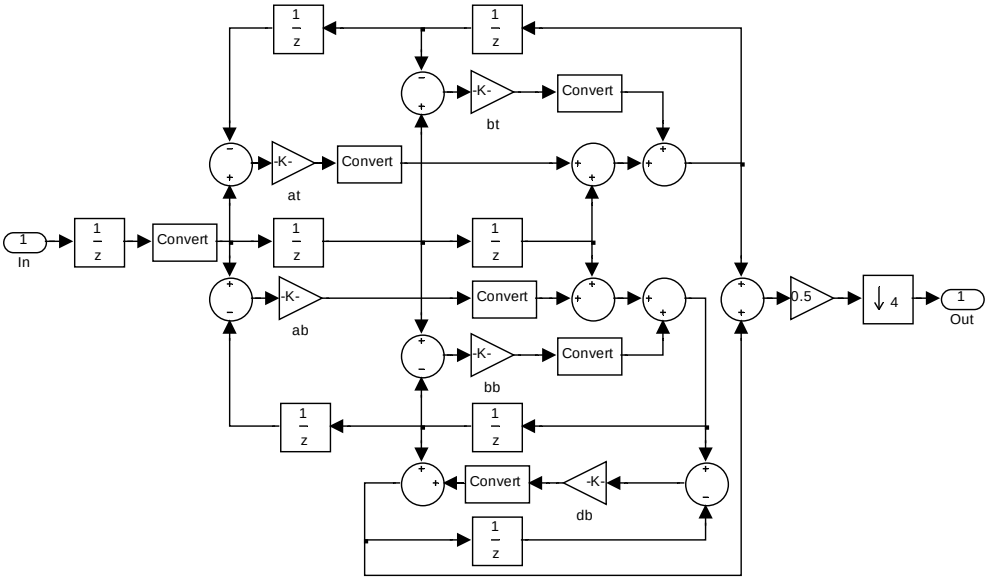


FIGURE 5.28: Simulink model of IIR filter for 2nd stage decimation

Finally the overall filter response in each decimation stages is given in Figure 5.29. Here since a non-halfband structure is used, the filter's cut-off frequency can be adjusted to the required frequency therefore aliasing does not occur. A slink filter roll-off compensator is not required either. The filter properties are summarised in Table 5.13.

TABLE 5.13: IIR Filter Properties for decimation 6 x 4

	1st Stage	**2nd Stage**
Decimation ratio	6	4
Filter type	Slink	IIR
Filter order	2	10
Passband ripple	N/A	<0.1 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	7 bits
Area utilisation	11161 gates	
Power dissipation	16.2 mW	

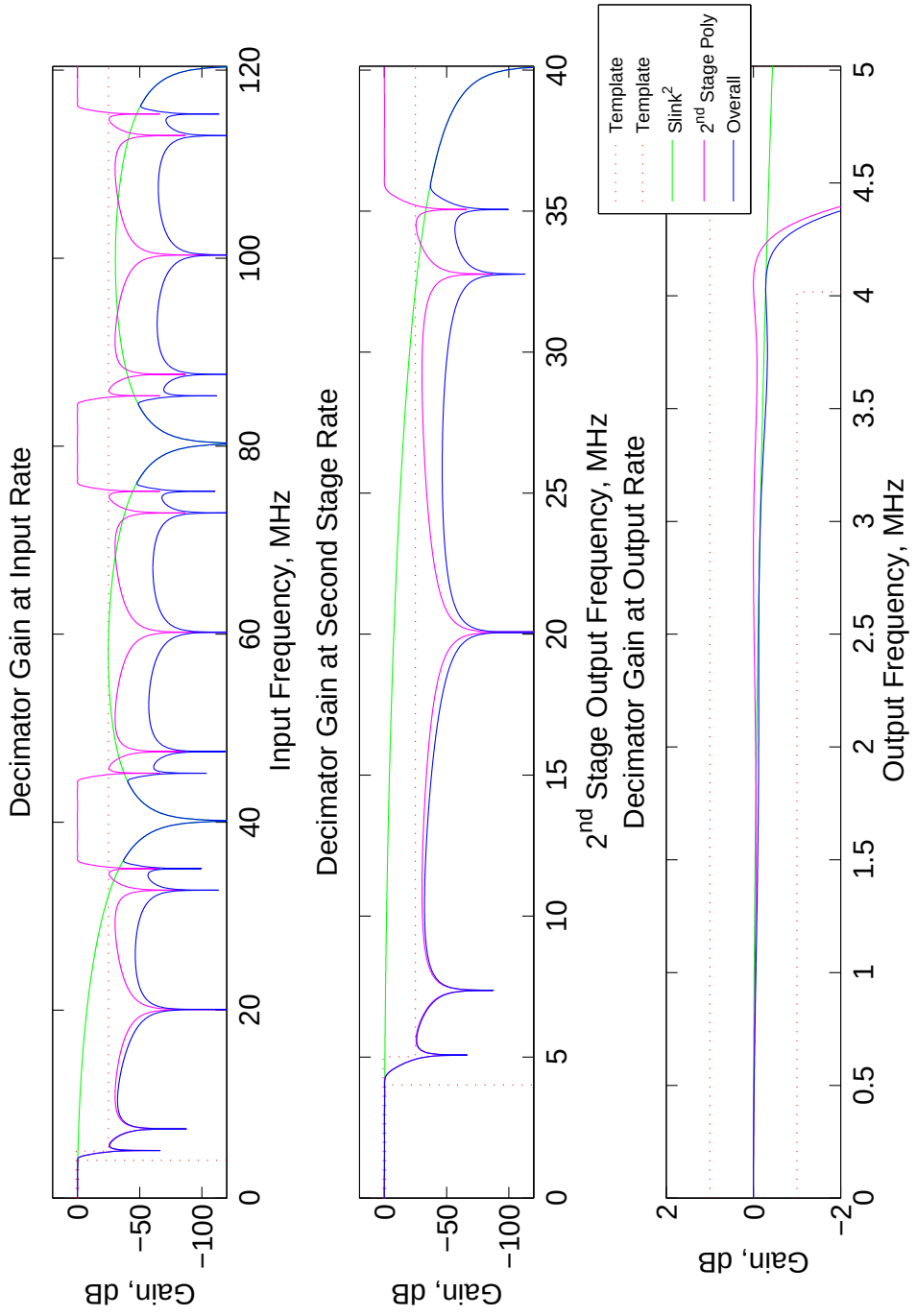


FIGURE 5.29: Overall Filter Response for decimation ratio 6 x 4 using IIR filters

5.2.3 Decimation with almost linear-phase IIR Filters

The third option was to use an Almost Linear Phase (ALP) IIR filter for the decimation process. ALP IIR filters have linear phase response in the passband frequencies and non-linear phase in the transition and the stopband frequencies. Although they are not as power and area efficient as minimum-phase IIR filters, compared to linear-phase FIR filters, they are more efficient.

The ALP IIR filter coefficients have been calculated using a the same 2-stage and 3-stage decimation ratios that have been reported in the previous sections with the FIR and IIR filters. Similarly, Slink lowpass filter is used as the first stage decimation filter for the reasons mentioned in the previous sections.

ALP IIR Filters uses allpass based structures with polyphase decomposition for efficient computing. Depending on the filter requirements, structures shown in Figure 5.30 and 5.31 were used. Also, sample delay z^{-D} depends on the decimation ratio D. However, using Noble identity the downsampler is moved from output to the input and z^{-D} becomes z^{-1}.

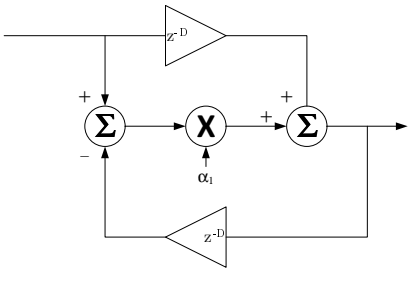


FIGURE 5.30: Allpass based IIR Filter Structure 1

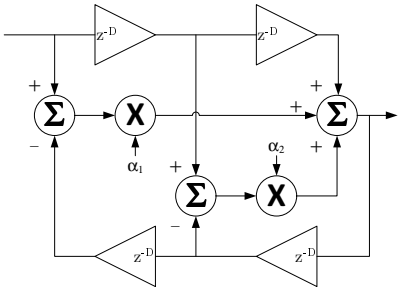


FIGURE 5.31: Allpass based IIR Filter Structure 2

Similar to minimum-phase IIR filter, the datapath needed to be quantized in order to restrict the bit growth because of the output feedback in the filter structure. But, as mentioned earlier, this introduces noise to the system. The amount of noise injected to the system is determined by the number of bits the datapath is quantized and for this research the noise floor for all the ALP IIR filters is chosen to be around -80dB which would be sufficient. The number of guardbits also needs to be calculated for each filter in order to make sure that the internal arithmetic does not overflow. This is estimated using the L1-norm which is defined Equation 5.4. The following sections report on the filters designed to be used in the decimation process.

Decimation by 4 x 3 x 2 ALP IIR

Decimation starts with Slink lowpass filter. A second order slink filter was sufficient for the first stage decimation. Then it followed by an ALP IIR lowpass filter with a decimation ratio of 3. When a minimum-phase IIR filter was deployed with a decimation ratio of 3 or higher a non-halfband allpass filter had to be used. However, with ALP IIR filters regardless of the decimation ratio, halfband allpass filter are used. This gave an advantage such that the decimation filters can work at the output sample rate rather than the input rate which minimized the power dissipation. The polyphase filter for an ALP IIR filter differs from the minimum-phase IIR filters which are:

- The number of polyphase path is determined by the decimation ratio
- The first branch of the filter contains only number of delays which the amount of delay depends on the filter complexity

- Depending on the filter requirements, a polyphase branch can be composed of either Structure 1 or Structure 2 or both structures shown in Figures 5.30 and 5.31 cascaded

For the second stage ALP IIR filter, the structure shown in Figure 5.32 is used. The final scale at the output is always the reciprocal of the decimation ratio therefore for this case it is 1/3. Usually in a 2 path polyphase IIR filter this scale is 1/2 and when implemented it does not require a dedicated multiplier, it is implemented simply by shifting the data towards the least significant bit by 1 bit. However, for scale 1/3 this is not the case. Therefore a dedicated multiplier had to be used. Also the filter is working at the output rate which is 3 times slower than the input rate which reduces the power dissipation. For the 3rd stage decimation ratio of 2, the structure given in Figure 5.33 is used. Since the decimation ration is 2 the output scale is 1/2 which is implemented as shifting the input to the scale to the towards LSB by 1 bit. The subsystems that are shown in Figures 5.32 and 5.33 are the allpass structures that are given in Figures 5.30 and 5.31. The naming conventions are as follows: Each component in any given path has labels started with the branch number (i.e. B0, B1, etc...). Then the subsystems have two types; either T1 or T2 which refer to the Figures 5.30 and 5.31 respectively. For example the subsystem named B1T1_1 implies that the subsystem in Branch 1 uses allpass structure 1.

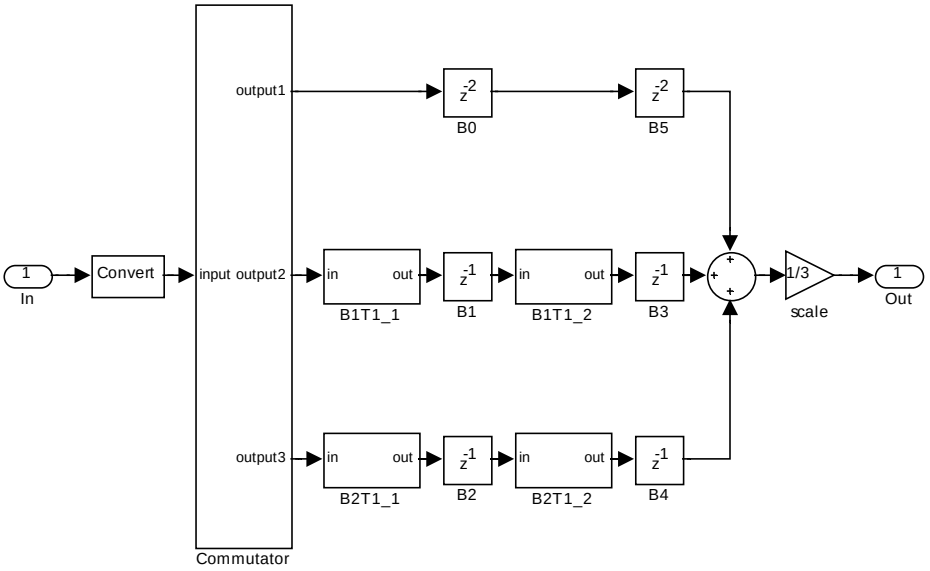


FIGURE 5.32: Simulink model of ALP IIR filter for the 2nd stage decimation

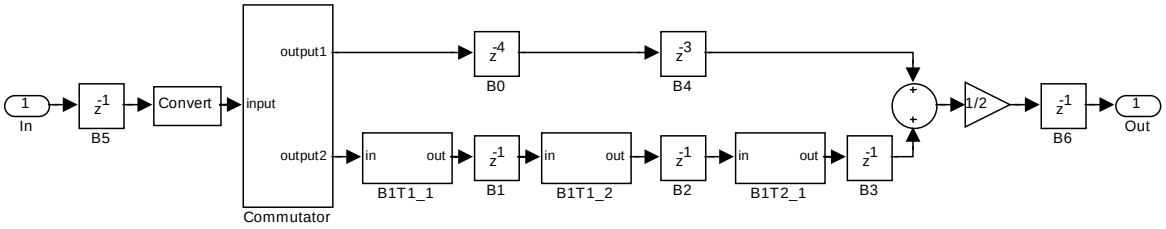


FIGURE 5.33: Simulink model of ALP IIR filter for the 3rd stage decimation

The overall decimation filter response for this particular case is given in Figure 5.34. As can be seen from the figure, the final stage filter transition band goes outside the template here also. However, as explained previously, this does not cause any problem. Also it can be seen that, in the middle of the stopband region of the 2nd-stage filter a small peak occurs. This is a well known artefact of using m-path polyphase filters where the path is greater than 2. More details on this problem can be found in [68]. Finally, the table 5.14 summarises the parameters used in this decimation combination. Compared to the equivalent minimum-phase IIR filter, it can be seen that ALP IIR filters require a higher filter order therefore consume more power. This is due to the

fact that it requires a higher order filter in order to linearise the phase response of the filter in the passband.

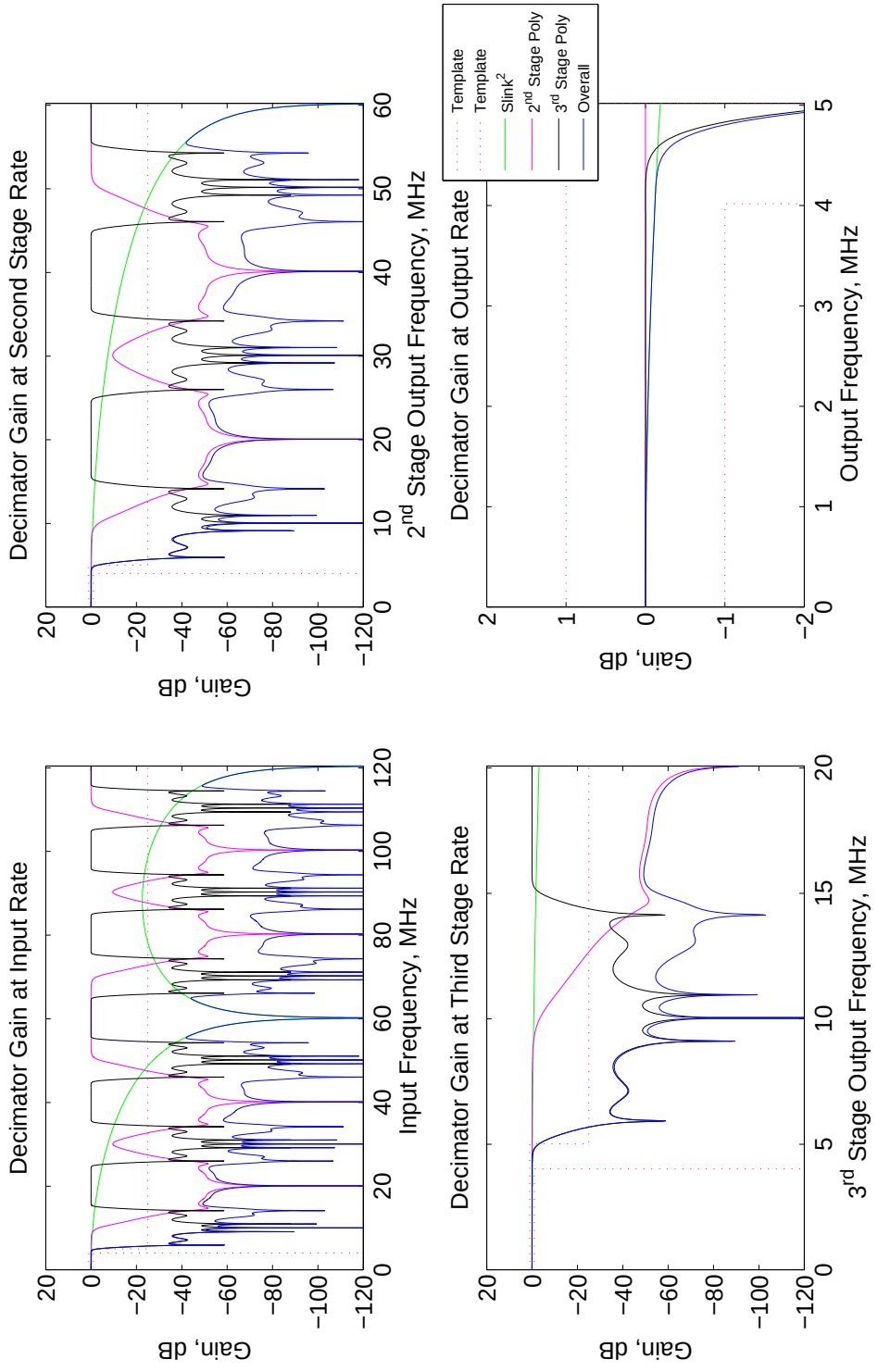


FIGURE 5.34: Overall Filter Response for decimation ratio 4 x 3 x 2 using ALP IIR filters

TABLE 5.14: ALP IIR Filter Properties for decimation 4 x 3 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	4	3	2
Filter type	Slink	ALP IIR	ALP IIR
Filter order	2	13	13
Passband ripple	N/A	<0.1 dB	<0.1 dB
Stopband attenuation	N/A	25 dB	25 dB
Coefficient wordlength	N/A	7 bits	6 bits
Area utilisation	19916 gates		
Power dissipation	11.3 mW		

Decimation by 6 x 2 x 2 ALP IIR

The second decimation combination to be considered starts with slink decimation reducing the sample rate by 6 followed by two stages each decimating by 2. Here, a second order slink filter was sufficient as well for the first stage decimation. It is followed by an ALP IIR decimators with a decimation ratio of 2. As explained previously the ALP IIR filters operate at the output rate. The Figure 5.35 and 5.36 show the ALP IIR filter structures used for the 2nd stage and 3rd stage decimation filtering respectively.

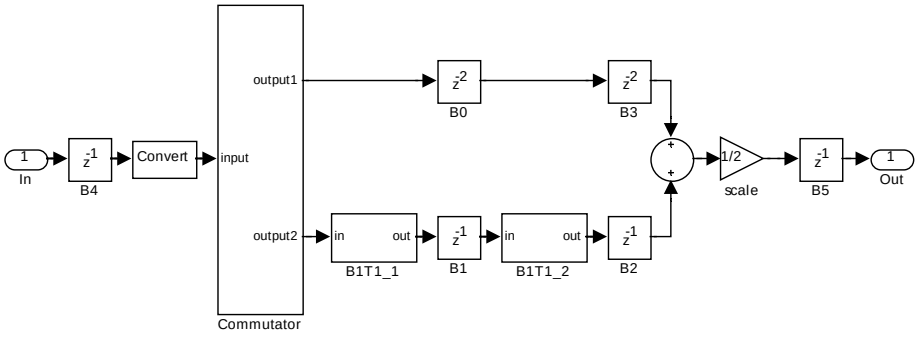


FIGURE 5.35: Simulink model of ALP IIR filter for 2nd stage decimation

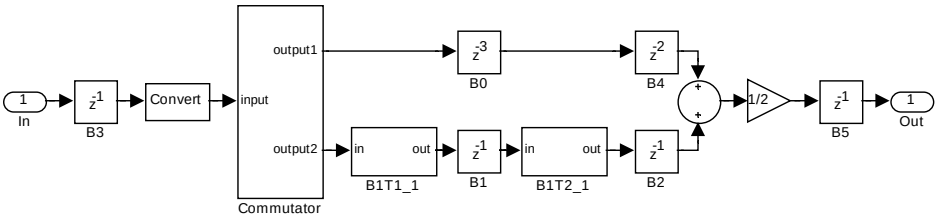


FIGURE 5.36: Simulink model of ALP IIR filter for 3rd stage decimation

The overall filter response in each decimation stage is been given in Figure 5.37. As explained in the previous case aliasing is present here as well. However, since it is in the transition band there is no need for an extra filtering at the output. Also slink filter roll-off compensation is not required because the overall passband is within the given specification. The filter properties are summarised in Table 5.15.

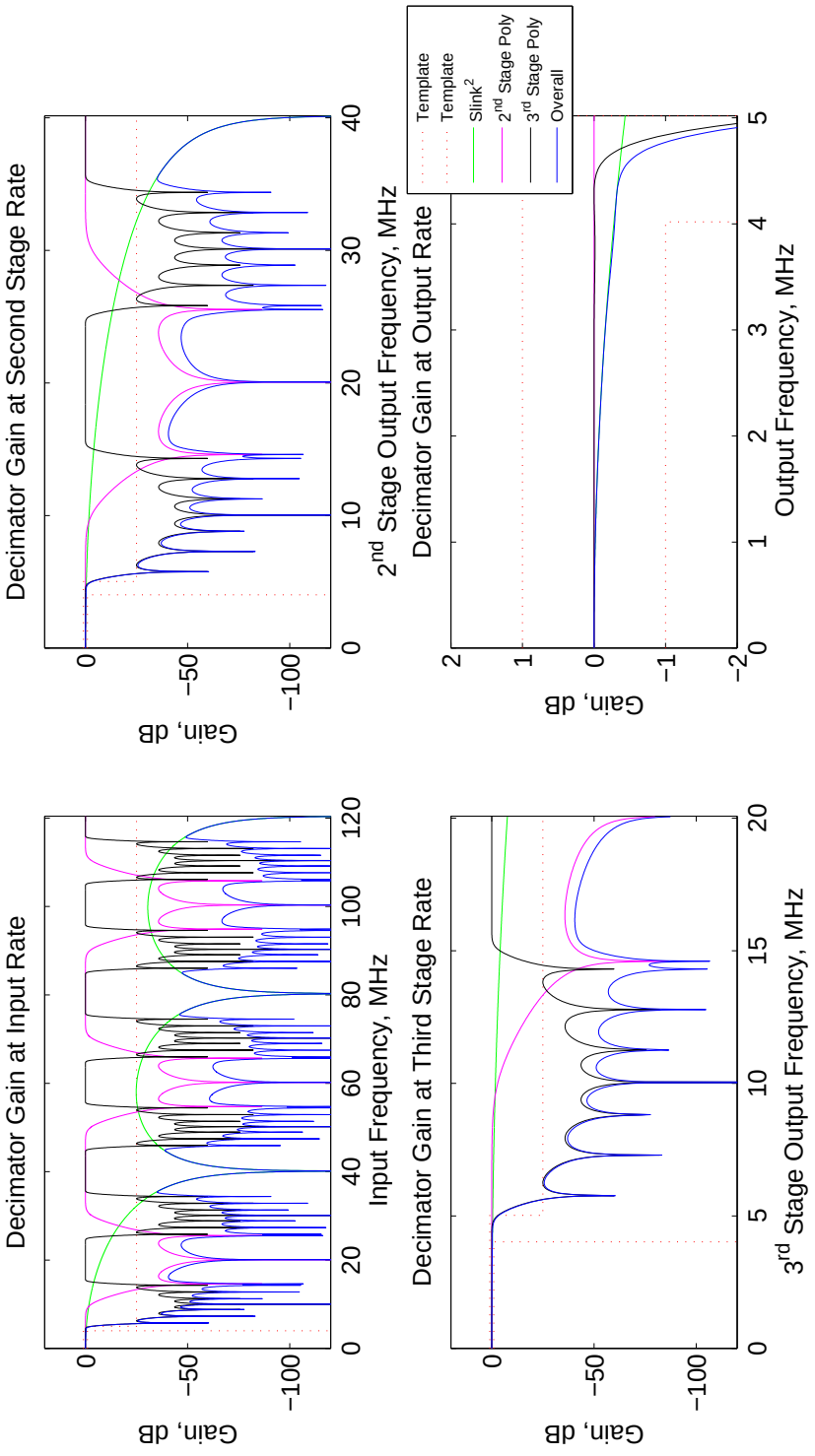


FIGURE 5.37: Overall Filter Response for decimation ratio 6 x 2 x 2 using ALP IIR filters

TABLE 5.15: ALP IIR Filter Properties for decimation 6 x 2 x 2

	1st Stage	**2nd Stage**	**3rd Stage**
Decimation ratio	6	2	2
Filter type	Slink	ALP IIR	ALP IIR
Filter order	2	7	7
Passband ripple	N/A	<0.1 dB	<0.1 dB
Stopband attenuation	N/A	25 dB	25 dB
Coefficient wordlength	N/A	5 bits	5 bits
Area utilisation	14570 gates		
Power dissipation	8.7 mW		

Decimation by 12 x 2 ALP IIR

The third option is a 2-stage decimator with a first stage reduction by 12 followed by 2 starting with slink decimator. This time, a second-order slink filter was not sufficient to filter out the out-of-band signals before the downsampling process so a third-order slink filter had to be deployed. The second stage is an ALP IIR lowpass filter with a decimation ratio of 2. Figure 5.38 shows the ALP IIR filter structure used for the 2nd stage decimation filtering.

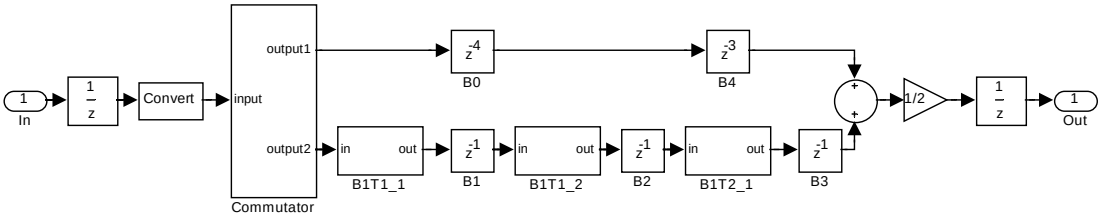


FIGURE 5.38: Simulink model of ALP IIR filter for 2nd stage decimation

The overall filter response in each decimation stage is given in Figure 5.39. As explained in the previous case, aliasing is present here as well. However, since it is in the transition band there is no need for an extra filtering at the output. However, a slink filter roll-off compensation is required because the overall passband ripples goes higher than the required specification. This is because, since the Slink Filter order is higher, the

passband roll-off is sharper as well. The Slink filter compensation structure that is used here is the same as shown previously in Figure 5.24 shows the structure used in order to compensate the Slink filter roll-off. Slink filter roll-off is compensated at output of the final stage where the sampling rate is lower than the other stages in order to reduce the power consumption. The filter properties are summarised in Table 5.16.

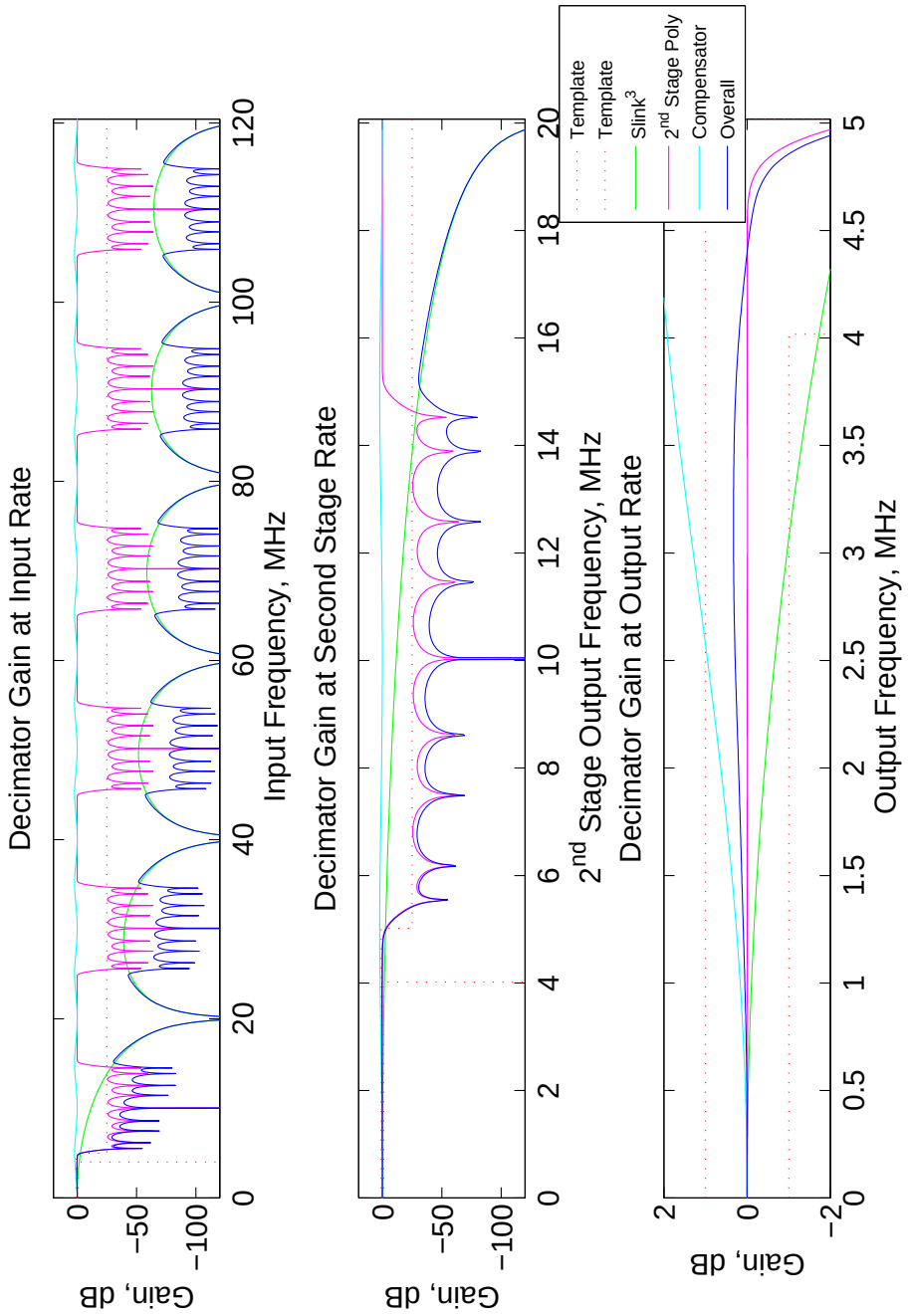


FIGURE 5.39: Overall Filter Response for decimation ratio 12 x 2 using ALP IIR filters

TABLE 5.16: ALP IIR Filter Properties for decimation 12 x 2

	1st Stage	**2nd Stage**
Decimation ratio	12	2
Filter type	Slink	IIR
Filter order	3	17
Passband ripple	N/A	<0.1 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	7 bits
Area utilisation	14938 gates	
Power dissipation	10.4 mW	

Decimation by 8 x 3 ALP IIR

The fourth option is another 2-stage decimation combination of 8 followed by 3 starting with a slink lowpass filter. A second-order Slink filter was sufficient to filter out the out-of-band signals before the downsampling process in this case. Then it followed by an ALP IIR lowpass filter with a decimation ratio of 3. Here, a scale of 1/3 is required at the filter output so a dedicated multiplier has to be used.

The overall filter response in each decimation stage is given in Figure 5.41. A Slink filter roll-off compensator is not required either. The filter properties are summarised in Table 5.17.

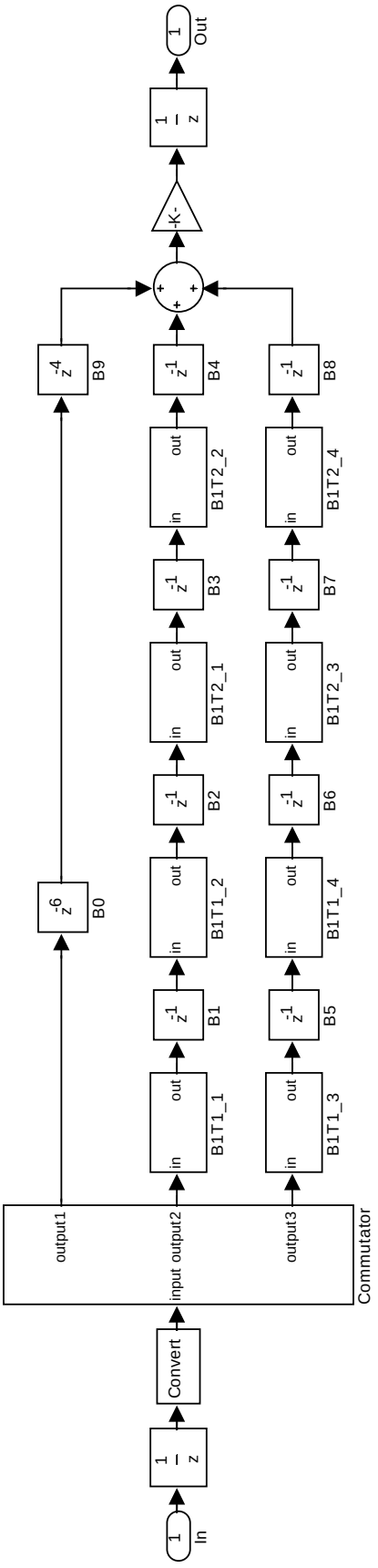


FIGURE 5.40: Simulink model of ALP IIR filter for 2nd stage decimation

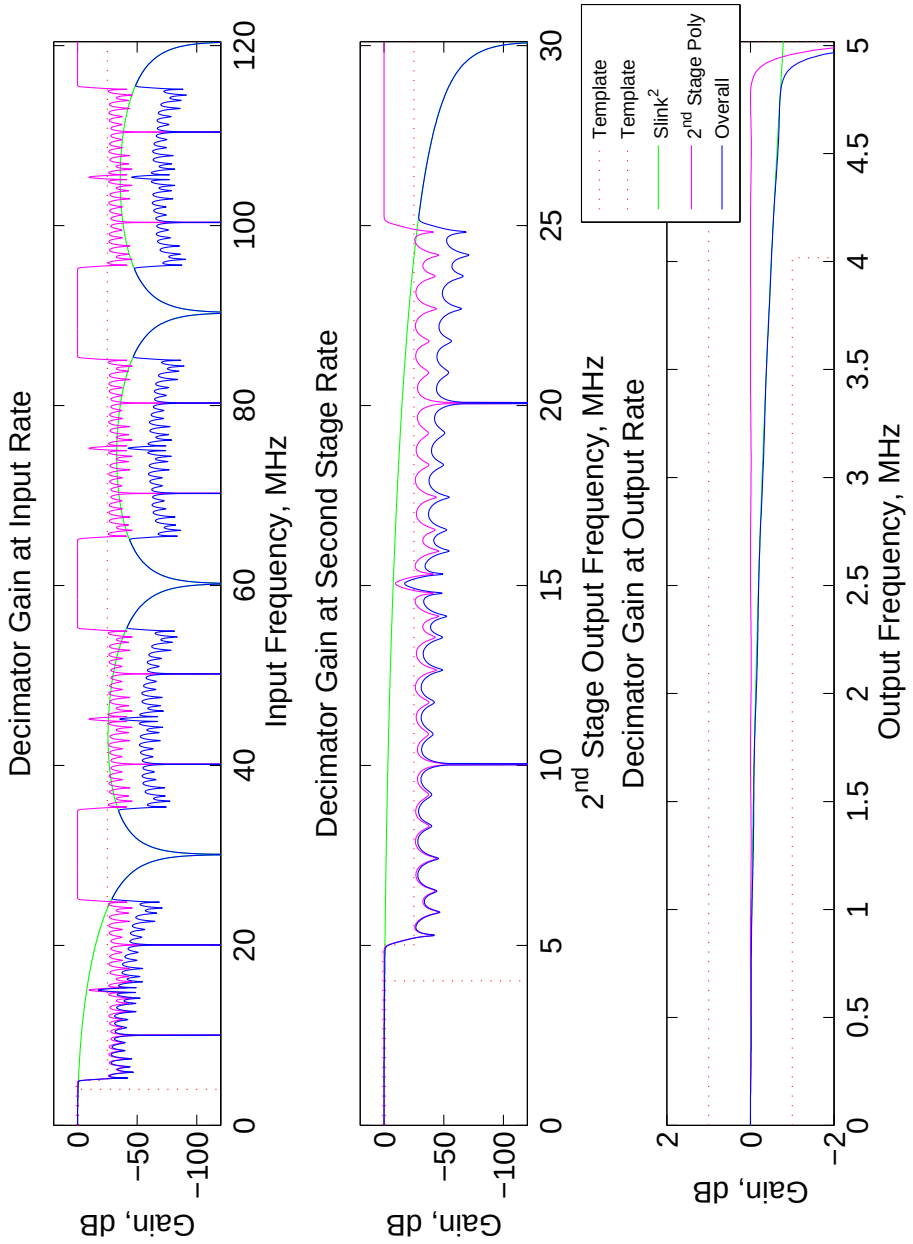


FIGURE 5.41: Overall Filter Response for decimation ratio 8 x 3 using ALP IIR filters

TABLE 5.17: ALP IIR Filter Properties for decimation 8 x 3

	1st Stage	**2nd Stage**
Decimation ratio	8	3
Filter type	Slink	IIR
Filter order	2	37
Passband ripple	N/A	<0.1 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	6 bits
Area utilisation	19126 gates	
Power dissipation	9.7 mW	

Decimation by 6 x 4 ALP IIR

The fifth option is another 2-stage decimation combination of 6 followed by 4 starting with slink decimator. A second-order slink filter was sufficient to filter out the out-of-band signals in the first stage. This followed an ALP IIR lowpass filter with a decimation ratio of 4. Figure 5.42 shows the ALP IIR filter structure used for the 2nd stage decimator.

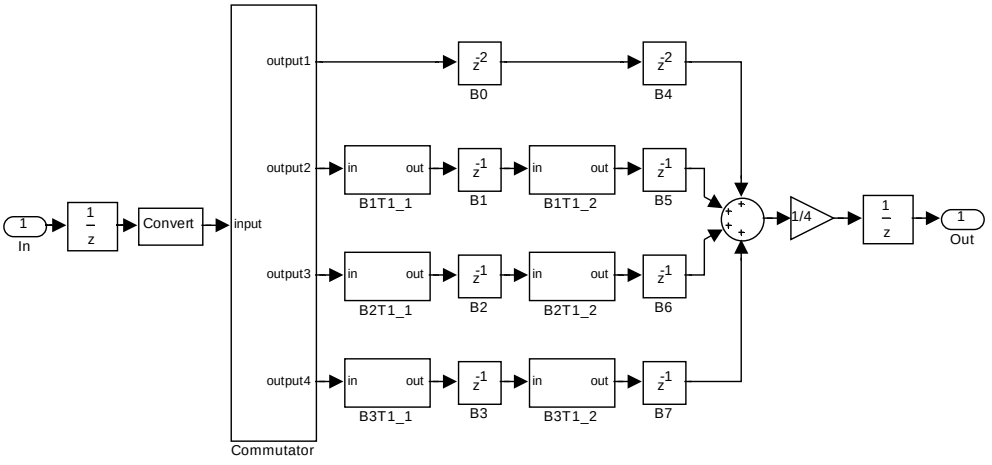


FIGURE 5.42: Simulink model of ALP IIR filter for 2nd stage decimation

The overall filter response in each decimation stage is given in Figure 5.43. A slink filter roll-off compensator is not required either. The filter properties are summarised in Table 5.18. It should also be noted that this decimation combination has the lowest

power consumption amongst all the decimation with ALP IIR filters. Compared to the lowest power dissipated by the FIR filter decimation, using ALP IIR filter for decimation filtering save power consumption by 2 times.

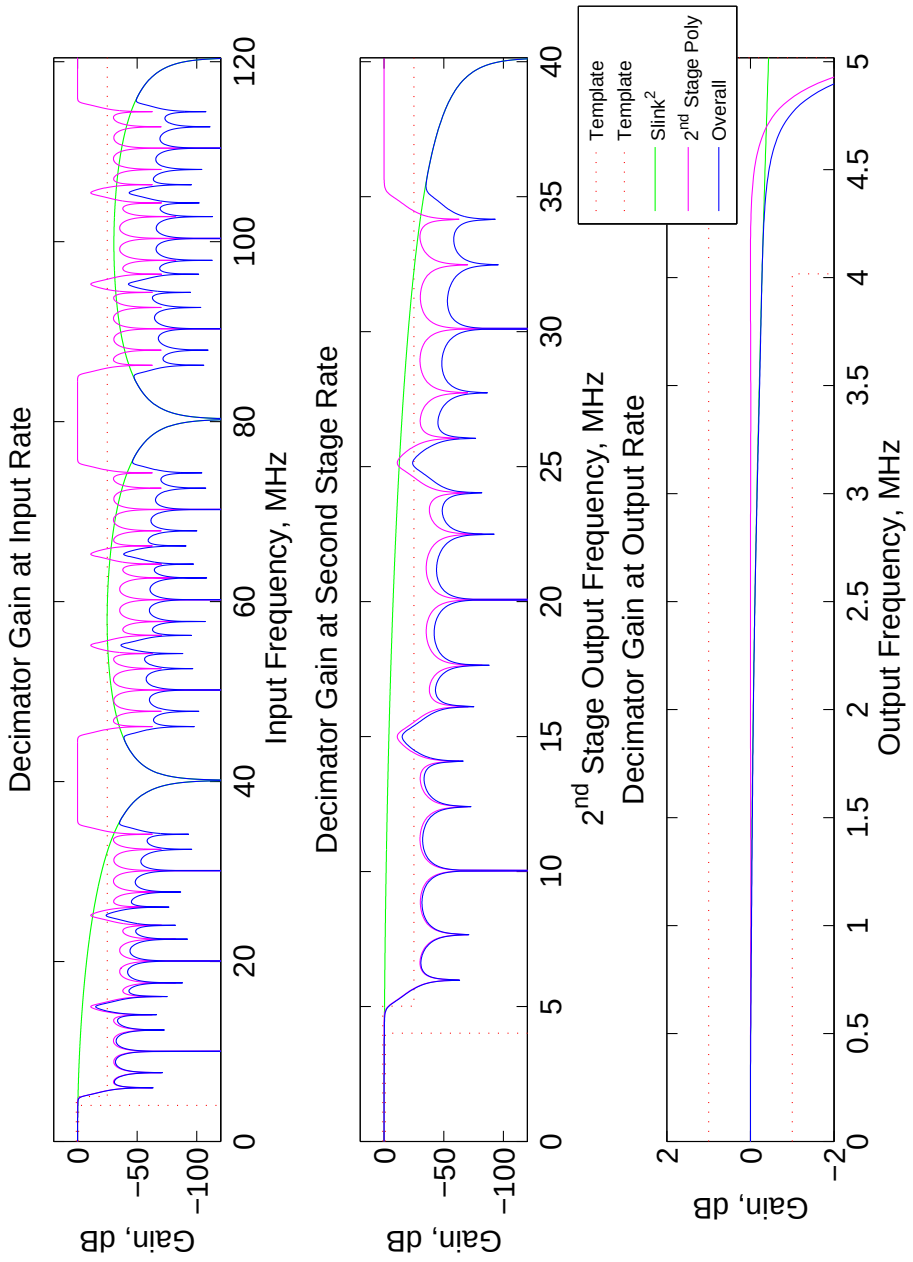


FIGURE 5.43: Overall Filter Response for decimation ratio 6 x 4 using ALP IIR filters

TABLE 5.18: ALP IIR Filter Properties for decimation 6 x 4

	1st Stage	**2nd Stage**
Decimation ratio	6	4
Filter type	Slink	IIR
Filter order	2	25
Passband ripple	N/A	<0.1 dB
Stopband attenuation	N/A	25 dB
Coefficient wordlength	N/A	7 bits
Area utilisation	16296 gates	
Power dissipation	8.0 mW	

5.3 Chapter Conclusion

This chapter presented the various filters that have been designed in order to understand how different filter types and different decimation ratio configurations affect the power dissipation and hardware resource utilisation. Linear-phase FIR, minimum-phase IIR and almost linear phase IIR type of filters have been considered. The filters implemented using polyphase decomposition in order to reduce the filter operating speed which saves power where possible. Also for minimum-phase IIR filters, halfband allpass based structures were used, where possible, since they use minimum number of multiplication. A summary of all the filter type and decimation ratios with their power dissipation and hardware utilisation are given in Table 5.19. It is demonstrated that by using an IIR filter the power dissipation and computational complexity reduces greatly. It should also be noted that decimators with minimum-phase IIR filters has the lowest power consumption amongst all the decimation cases considered. Compared to the lowest power dissipated by the FIR filter decimation, it is also shown that using IIR filter for decimation filtering save power consumption by 2.5 times. When ALP IIR decimators were deployed, compared to the equivalent FIR filter it can be seen that they still

use less hardware resources and dissipate less power. On top of that, by dividing the decimation ratio into multi stages saves extra power and computation cost.

TABLE 5.19: Various Decimation Stages Studied

Combination		**Filter Type**					
		Linear-phase FIR Filter		**Minimum-phase IIR Filter**		**Almost-linear phase IIR Filter**	
		Number of gates	Power [mW]	Number of gates	Power [mW]	Number of gates	Power [mW]
3-stage	4 x 3 x 2	82350	31.7	11374	12.4	19916	11.3
	6 x 2 x 2	82828	31.3	12169	7.9	14570	8.7
2-stage	12 x 2	51175	19.3	9828	9.3	14938	10.4
	8 x 3	62382	22.6	9585	11.3	19126	9.7
	6 x 4	82208	28.7	11161	16.2	16296	8.0
1-stage	24	466453	144.4				

Chapter 6

Filtering Effects on Positioning

After the digital filters were designed and tested, the next task was to deploy them on a test platform in order to evaluate the performance of the decimators with real GPS signals by measuring the effects of phase non-linearity on the position estimate. This chapter begins by explaining the integration of the designed filters into the test system where the filters were implemented on an FPGA and operated in real time. The overall performance using the different decimation filters is then evaluated and compared. The impact of non-linear phase of the IIR filters on the pseudorange is then described for both GLONASS and GPS signals. The concept of pseudorange compensation is then introduced and the effectiveness of various compensation methods are evaluated.

6.1 Test Platform

The hardware realisation of the filters that have been described in Chapter 5 were designed using VHDL and then integrated into the ADVRG GNSS FPGA based test platform in order to undertake real-time testing with real-world signals.

Since the rest of the GNSS receiver design uses most of the FPGA hardware resources, each filter had to be integrated sequentially otherwise the FPGA resources would not be sufficient. Consequently, for each filter, the position measurement had to be taken sequentially. The measurements were taken as quickly as possible so that the satellites did not move very much between measurements. For each decimation combination, 3 types of filters were used to capture positioning data. These were linear-phase FIR filters, minimum-phase IIR filters and almost-linear-phase IIR filters. There was time to acquire positioning data for these 3 different filters for only one decimation combination in any one day. Consequently, the next set of measurements with a different set of decimation ratios was taken exactly 23 hours 56 minutes later when the given constellation at the measurement point appears again [69]. This ensures that positioning data is captured with the same set of satellites with the same constellation for all the decimation ratios and filters being tested. It, therefore required 7 days to acquire a full set of results.

Figure 6.1 shows the GPS constellation used to compare the decimator's position performance. All the data were recorded using this constellation as described above. Figure 6.2 shows a different GPS constellation which was also used in order to measure the repeatability of the experiments as explained in the following section.

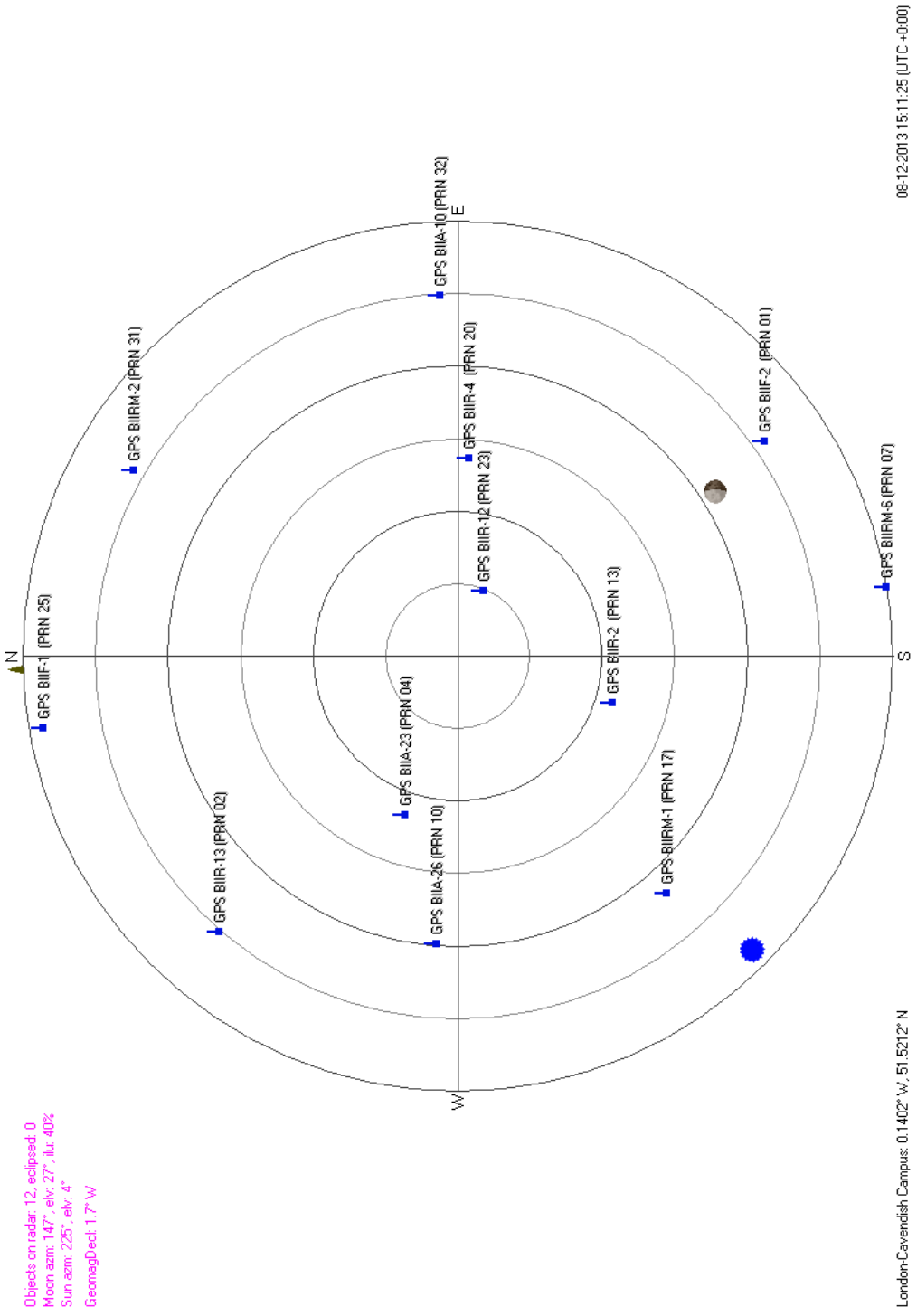


FIGURE 6.1: GPS Constellation used for measuring decimator performance

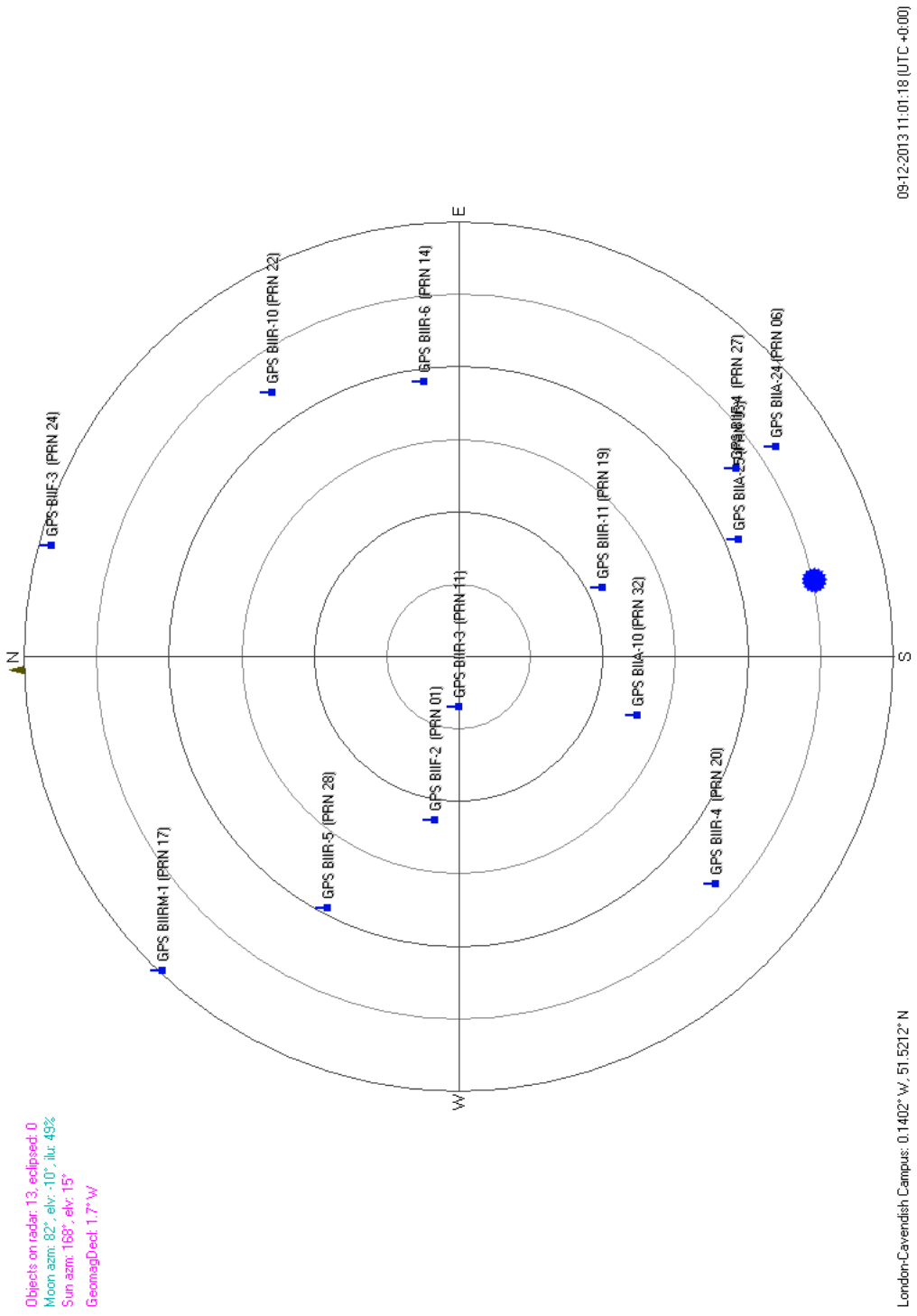


FIGURE 6.2: GPS Constellation used for repeatability test

The variation in group delay over the range of Doppler frequency offsets is relatively small. Therefore it was possible to model the change in group delay as a function of the Doppler shift using a second-order polynomial.

$$t_d = c_d . {f_d}^2 + t_0 \tag{6.1}$$

The coefficient c_d was determined by experiment for the possible Doppler range between ±10 kHz and the match is shown in Figure 6.3 for the decimation combination of 8 by 3 with $c_d = 3.25 \times 10^{-21}$. Since the Doppler frequency of the carrier wave was very small compared with the overall decimation filter's bandwidth, the group delay variation was also very small, around 0.3 picoseconds. Different satellites produce different pseudorange measurements but since the same filter that is being used is same therefore the observation is not position dependent.

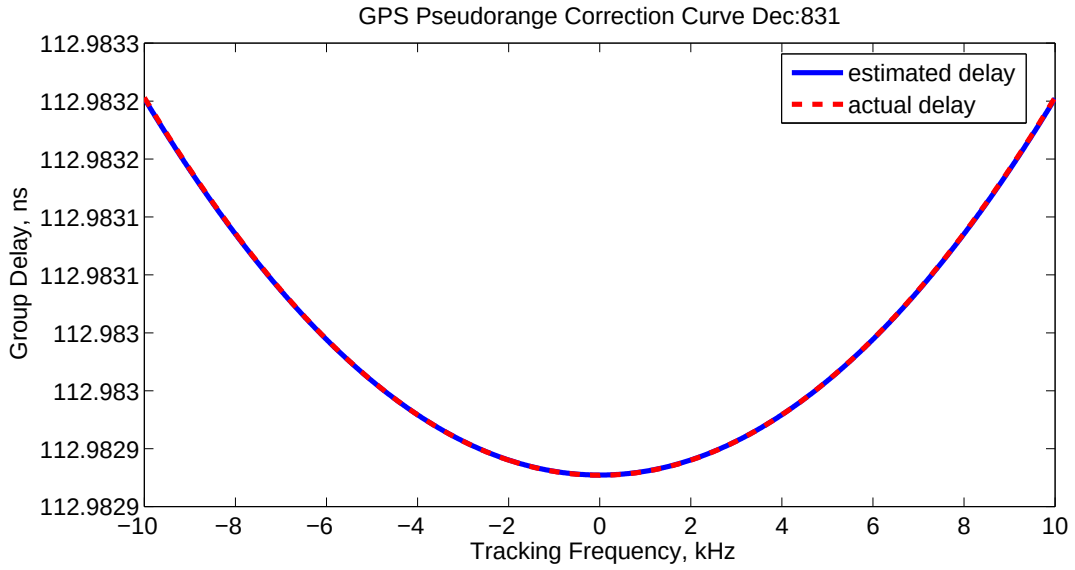


FIGURE 6.3: Group delay estimation for decimation combination 8x3

Later for position calculation with an IIR filter, the non-linear phase was compensated using this 2nd order curve fitting which minimized the positioning error.

6.2 Position Variation vs Decimation Structure

In the following experiments, approximately 80 position measurements (each taking 500 ms) were made. The figures show the individual measurements (+) and their mean (□) while the accompanying table provides a key.

6.2.1 Measurement Repeatability

A set of measurements were taken with different constellations in order to check if the measurement would differ with different constellations. The difference was measured by the average distance from the reference antenna position as well as the standard deviation of each individual measurement points. For this decimation combination, two different experiments were performed. Firstly, a set of measurements were taken the satellite constellation shown in Figure 6.1 and the following day a second measurement were taken with the same satellite constellation in order to establish the repeatability of the measurements. A third measurement was taken with a completely different satellite constellation, shown in Figure 6.2 in order to investigate the influence of the satellite positions on these comparisons. The results are shown and explained in Figure 6.4 and Table 6.1.

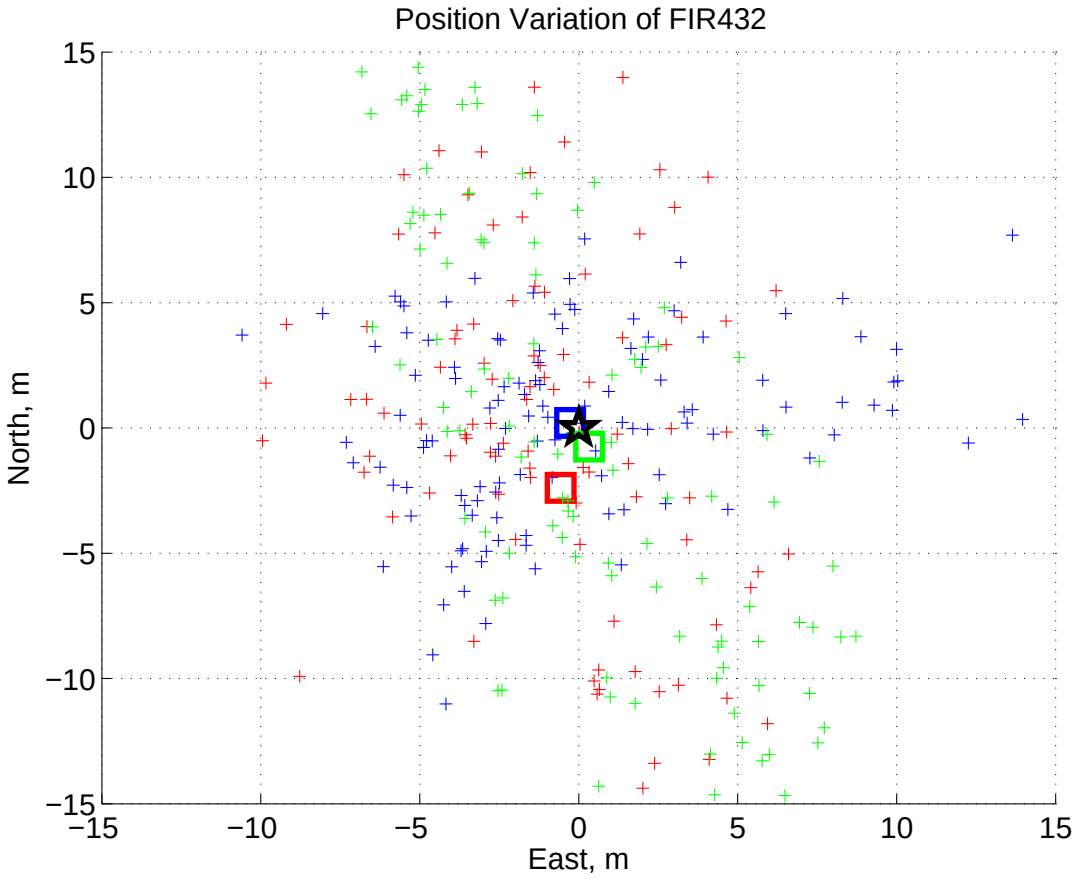


FIGURE 6.4: Position variation of FIR filter with decimation 4-3-2

TABLE 6.1: Legend of position variation for FIR432

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 432	9.98m	2.46m	
+/□	FIR 432	10.12m	0.81m	
+/□	FIR 432	6.11m	0.33m	Different constellation
☆	REF			

It can be seen that the measurements with same and different constellations have a similar spread of results both with the error in the mean position being only a few metres.

The second experiment repeated the same measurements using IIR filters with the same decimation combination of 4 by 3 by 2. As in the previous experiment, the first

2 measurements were taken with the satellite constellation shown in Figure 6.1 and a third measurement with a different satellite constellation, Figure 6.2, was recorded. The results are presented in Figure 6.5 and Table 6.2.

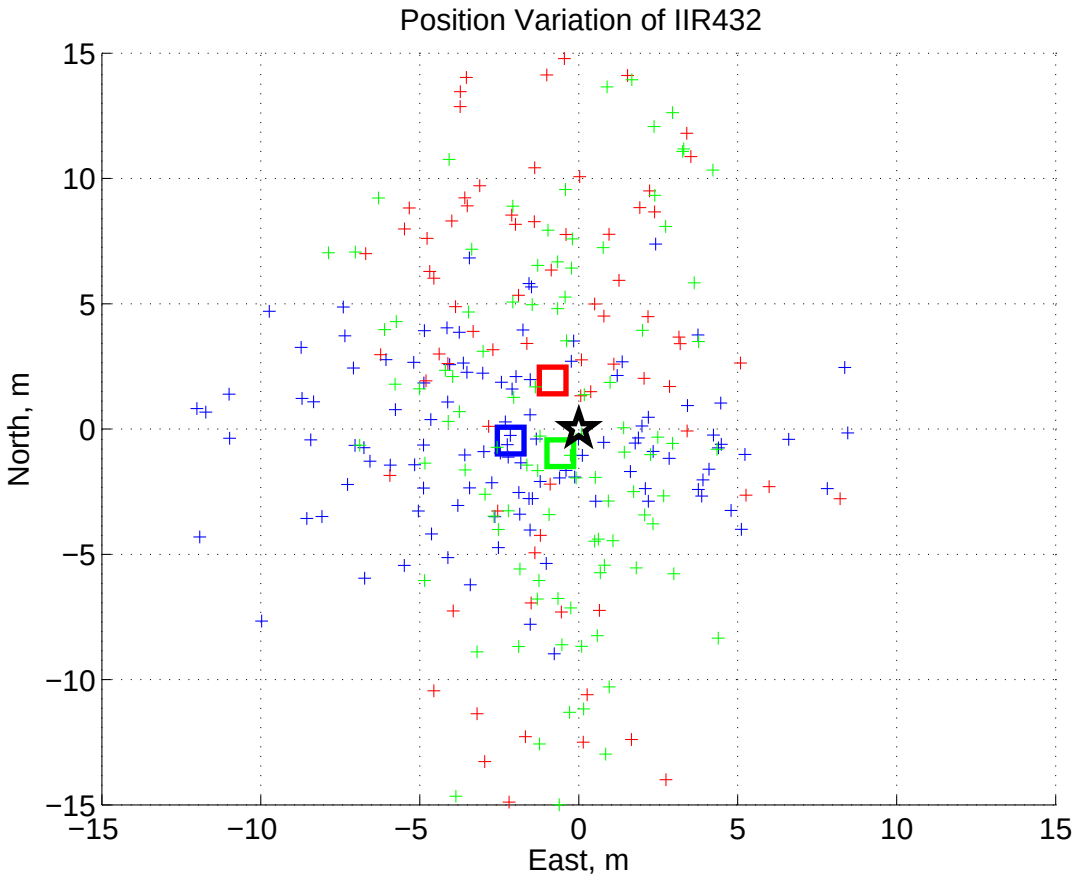


FIGURE 6.5: Position variation of IIR filter with decimation 4-3-2

TABLE 6.2: Legend of position variation for IIR432

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	IIR 432	14.36m	2.11m	
+/□	IIR 432	9.11m	1.13m	
+/□	IIR 432	5.51m	2.19m	Different constellation
☆	REF			

The third experiment was to repeat the same measurements using ALP IIR filters with the same decimation combination of 4 by 3 by 2. Once again, this was necessary in

order to establish the effects of using the ALP IIR filter in positioning performance. As in the previous experiment, the first 2 measurements were taken with the same satellite constellation and a third measurement with different satellite constellation was recorded. The results are presented Figure 6.6 and Table 6.3.

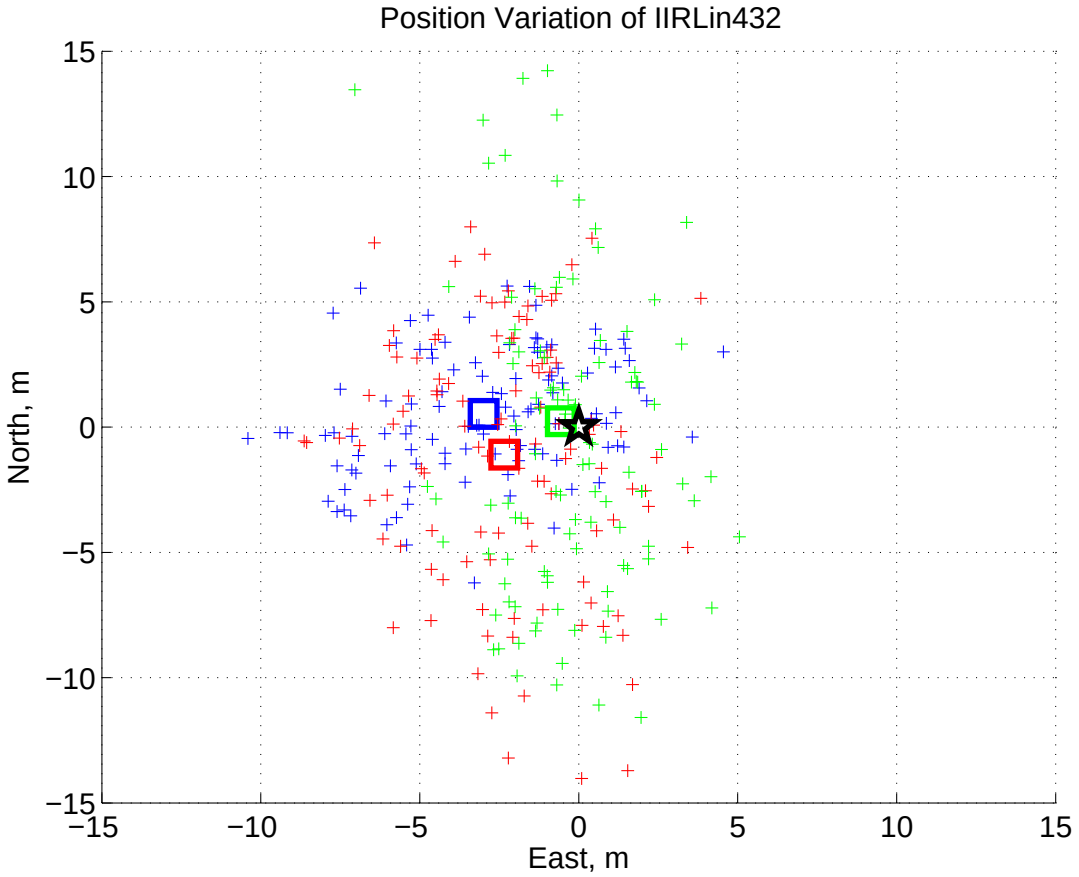


FIGURE 6.6: Position variation of ALP IIR filter with decimation 4-3-2

TABLE 6.3: Legend of position variation for IIRLin432

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	IIRLin 432	5.68m	2.59m	Same const.
+/□	IIRLin 432	7.57m	0.61m	Same const.
+/□	IIRLin 432	3.94m	3.04m	Different const.
☆	REF			

Comparing Figures 6.4, 6.5 and 6.6 shows any differences in the position estimate following FIR and IIR decimators are smaller than the random variations due to noise.

6.2.2 Filters with Decimation 4-3-2

The next set of measurements were taken with the constellation shown in Figure 6.1. The 3 decimation types for the decimation combination of 4 by 3 by 2 are compared in Figure 6.7 and Table 6.4. In addition, the effect of adding a correction term as described in Equation 6.1. with $C_d = 300 \times 10^{-24}$ is shown as filter type "IIR432-C".

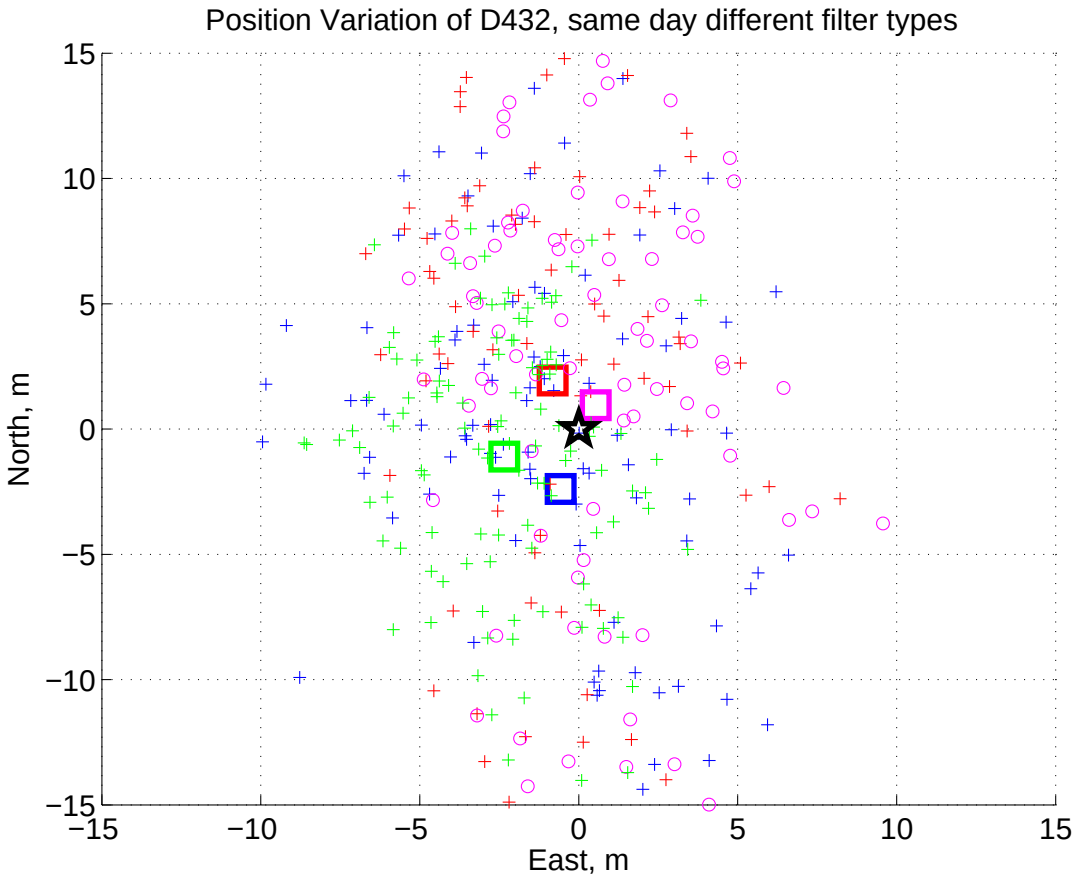


FIGURE 6.7: Position variation of filters with decimation 4-3-2

TABLE 6.4: Legend of position variation for D432

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 432	9.98m	2.46m	
+/□	IIR 432	14.36m	2.11m	
○/□	IIR 432-C	14.36m	1.09m	phase compensation
+/□	IIRLin 432	5.68m	2.59m	
☆	REF			

6.2.3 Filters with Decimation 6-2-2

The next set of measurements were taken with the constellation shown in Figure 6.1. The 3 decimation types for the decimation combination of 6 by 2 by 2 are compared in Figure 6.8 and Table 6.5. In addition, the effect of adding a correction term as described in Equation 6.1 with $C_d = 350 \times 10^{-24}$ is shown as filter type "IIR622-C".

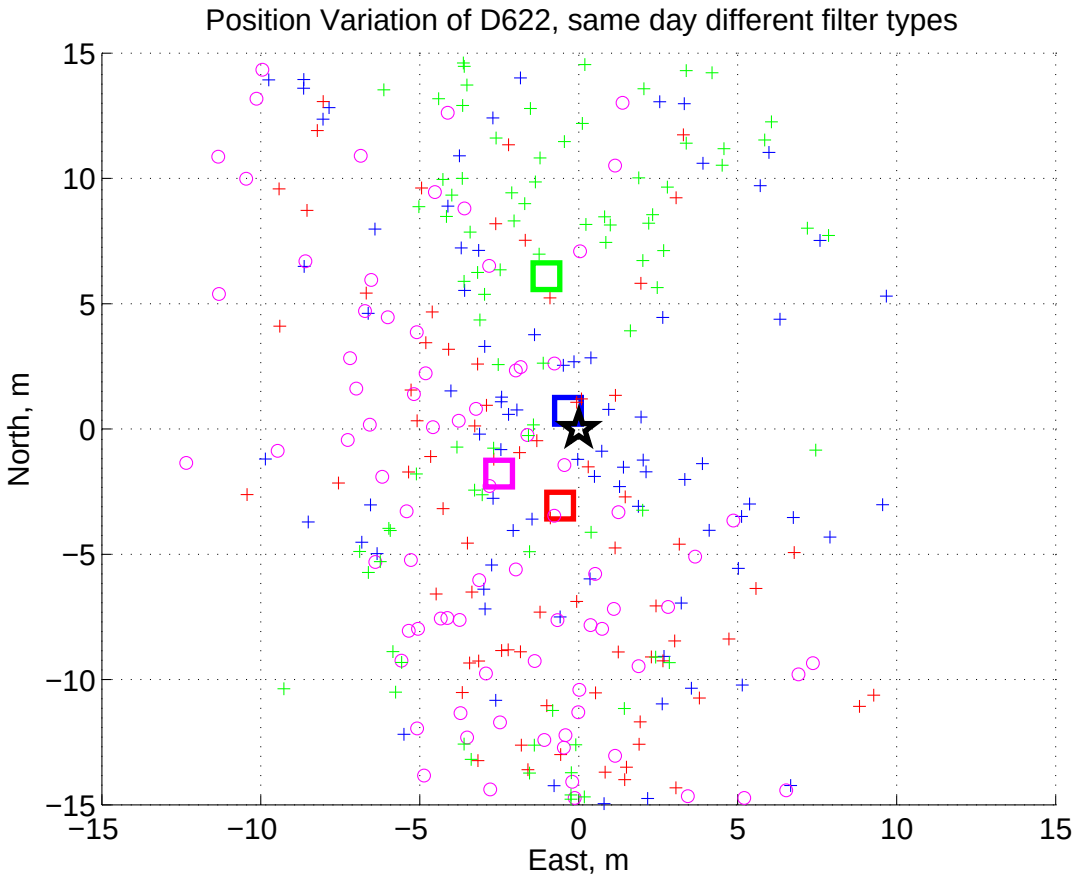


FIGURE 6.8: Position variation of filters with decimation 6-2-2

TABLE 6.5: Legend of position variation for D622

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 622	14.00m	0.8m	
+/□	IIR 622	13.73m	3.12m	
○/□	IIR 622-C	13.73m	3.07m	phase compensation
+/□	IIRLin 622	11.80m	6.18m	
☆	REF			

6.2.4 Filters with Decimation 6-4

The next set of measurements were taken with the constellation shown in Figure 6.1. The 3 decimation types for the decimation combination of 6 by 4 are compared in Figure 6.9 and Table 6.6. In addition, the effect of adding a correction term as described in Equation 6.1 with $C_d = 1.9 \times 10^{-21}$ is shown as filter type "IIR641-C".

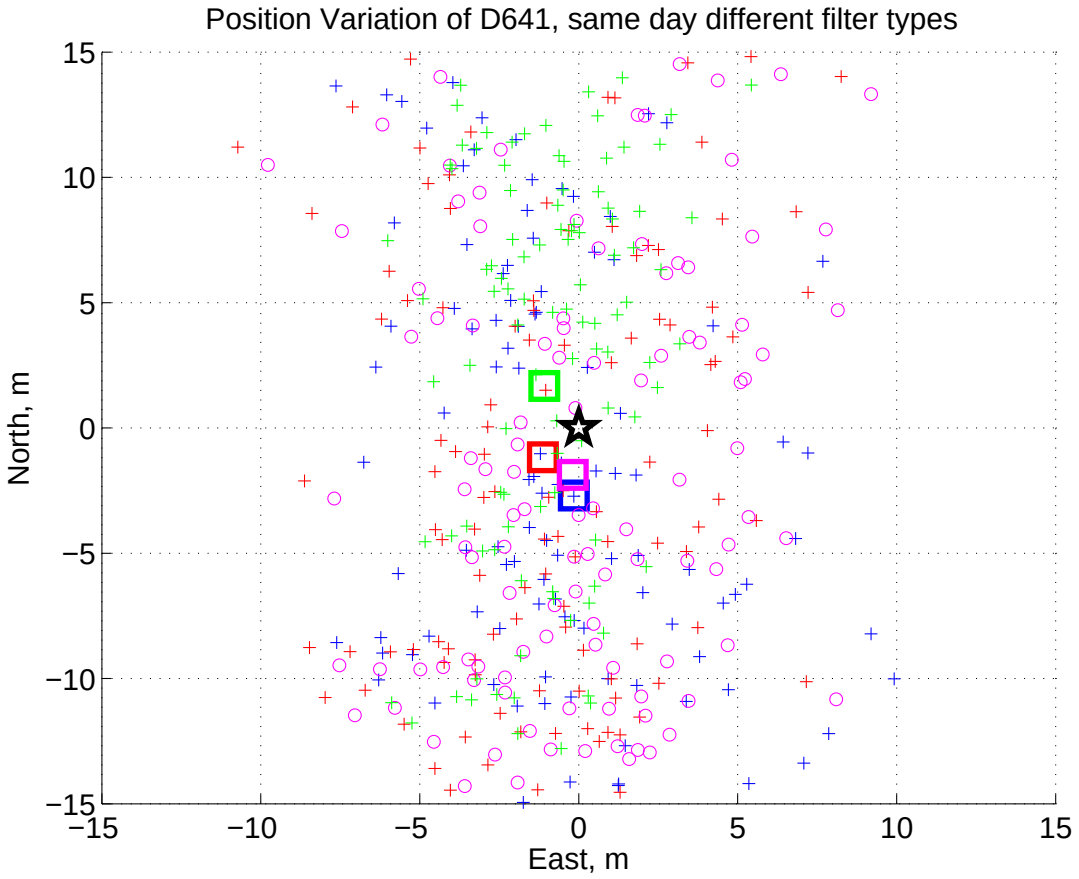


FIGURE 6.9: Position variation of filters with decimation 6-4

TABLE 6.6: Legend of position variation for D641

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 641	9.78m	2.70m	
+/□	IIR 641	9.93m	1.63m	
○/□	IIR 641-C	9.93m	1.89m	phase compensation
+/□	IIRLin 641	10.60m	1.99m	
☆	REF			

6.2.5 Filters with Decimation 8-3

The next set of measurements were taken a decimation ratio of 8 by 3. The results are presented below. The satellite constellation was also same as the one as it is for

the previous decimation ratios explained earlier in order to be able to compare the analysis results across all the measurements. The results are compared in Figure 6.10 and Table 6.7. The effect of adding a correction term as described in Equation 6.1 with $C_d = 3.25 \times 10^{-21}$ is shown as filter type "IIR831-C".

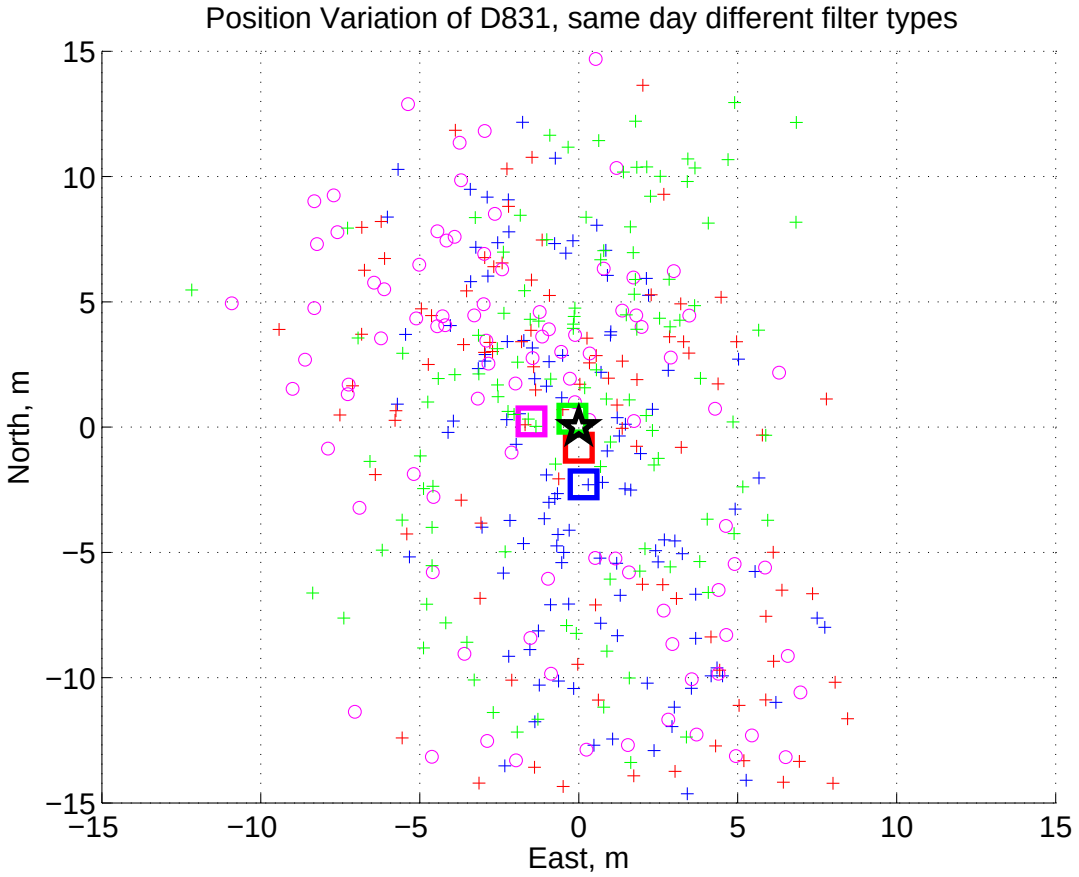


FIGURE 6.10: Position variation of filters with decimation 8-3

TABLE 6.7: Legend of position variation for D831

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 831	7.46m	2.29m	
+/□	IIR 831	11.40m	0.82m	
○/□	IIR 831-C	11.40m	1.50m	phase compensation
+/□	IIRLin 831	8.44m	0.39m	
☆	REF			

6.2.6 Filters with Decimation 12-2

The last set of measurements were taken a decimation ratio of 12 by 2. The results are presented below in Figure 6.11 and Table 6.8. The satellite constellation was also same as the one as it was for the previous decimation ratio combinations explained earlier. The coefficient value used for this measurement to correct the pseudorange estimation was $c_d = 50 \times 10^{-15}$.

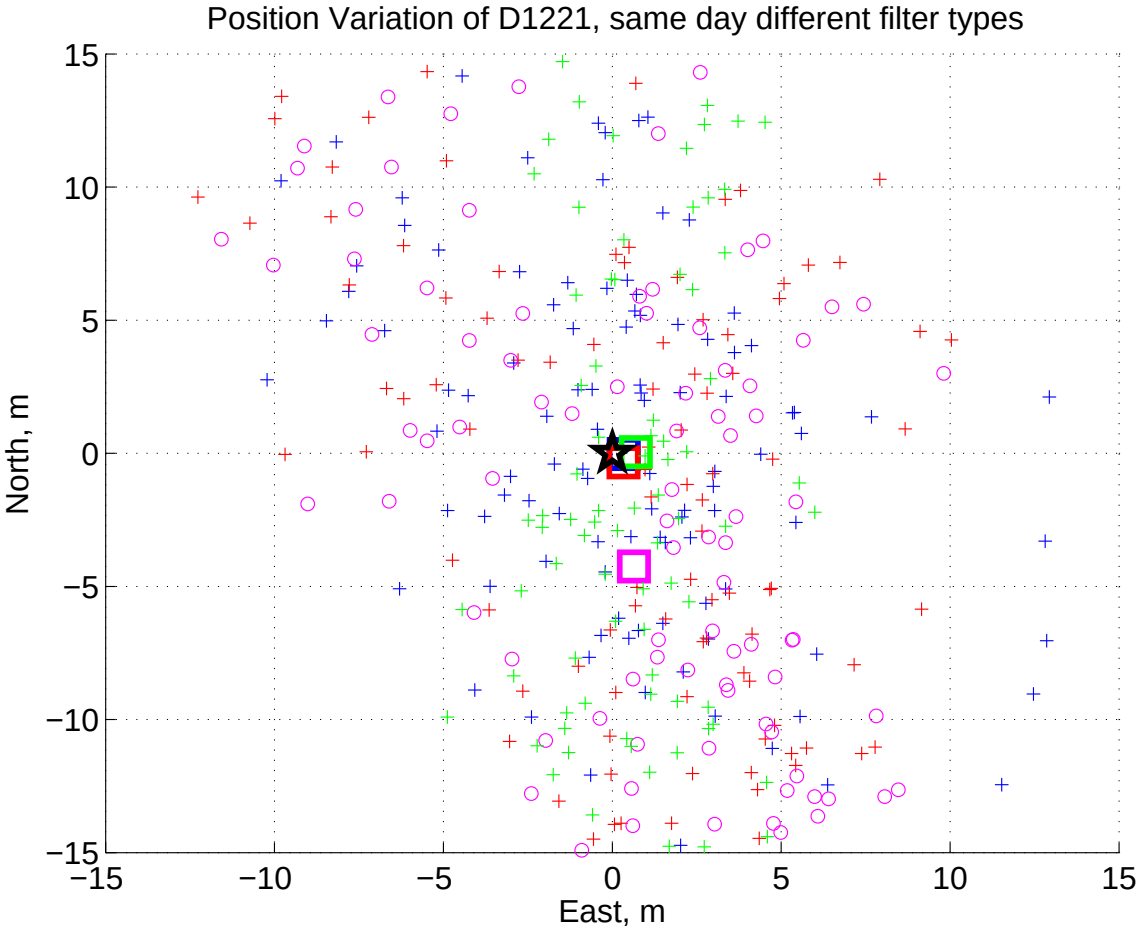


FIGURE 6.11: Position variation of filters with decimation 12-2

TABLE 6.8: Legend of position variation for D1221

Legend	Filter Type	Std Dev	Distance of mean from the Reference	Comments
+/□	FIR 1221	9.70m	0.34m	
+/□	IIR 1221	11.65m	0.48m	
○/□	IIR 1221-C	14.17m	4.30m	phase compensation
+/□	IIRLin 1221	11.92m	0.70m	
☆	REF			

The results of the measurements are presented. As can be seen from all the figures above in every decimation combination, the position variation between different filter types are within the noise. This showed that using a non-linear phase filter does not have negative effect on the positioning performance using GPS signals.

6.3 Performance Analysis with Pseudorange

6.3.1 GPS Pseudorange Measurement

The real-time testing of the filters given above has shown that, for the GPS L1 C/A signal, the use of more efficient non-linear-phase filter does not deteriorate the positioning performance. In order to further investigate the effects of the filter's phase non-linearity a set of artificial GPS L1 C/A data was produced with real navigation data that was extracted from the real-time testing of the filters. In order to perform the experiment, a range of different Doppler frequencies were introduced to the generated GPS signal. The Doppler offset ranges from 0 Hz up to 10 kHz, which is the maximum possible Doppler shift possible for a GPS [41], in steps of 500 Hz, resulting in 21 GPS signals being synthesised each with different Doppler frequency. These were stored

to provide a set of experimental input signals. The generated GPS data were then decimated using a linear-phase FIR filter and a minimum-phase IIR filter separately. For filtering two stage decimation of combination 8 by 3 was used. The reason for choosing this particular combination was because the IIR filter had one of the highest group delay variation between 0 and Nyquist.

After the GPS L1 C/A signals were filtered with linear-phase FIR and minimum-phase IIR filters, the decimator outputs were stored and subsequently need to acquire the satellites. Then the acquired satellites were tracked for 36 seconds, which is the minimum required tracking time in order to extract navigation bits from the GPS signal that could provide a position. After the navigation bits were extracted, the pseudoranges were calculated individually for each filter and for each Doppler frequency. The difference between FIR filtered and IIR filtered pseudoranges for each Doppler frequency group were compared in order to establish the effects of the phase non-linearity. Figure 6.12 shows the results of the measurements taken. It is seen that, as the Doppler frequency increases the pseudorange difference also increases. However the pseudorange reduction is in the order of millimetre which is well below the noise floor.

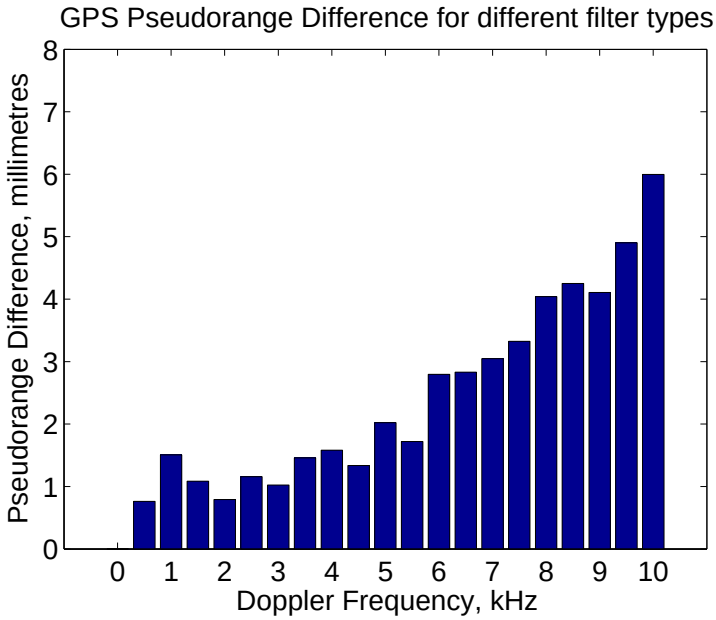


FIGURE 6.12: GPS Pseudorange difference between linear-phase FIR & minimum-phase IIR filters

6.3.2 GLONASS Pseudorange Measurement

Subsection 6.3.1 presented measurements using GPS signals. GPS uses a CDMA channel access technique. The performance in terms of final user position was relatively unaffected by the Doppler frequency shifts with a non-linear phase IIR filter. However, in a GNSS signal such as GLONASS, where an FDMA type of channel access is used, the phase non-linearity was expected to have great impact on the pseudorange measurements.

In order to establish the filter's phase non-linearity effect on a GLONASS signal, the same experiment setup was repeated but this time set of GLONASS data were generated with different Doppler frequencies that ranges from 0 Hz up to 10 kHz. Then the generated GLONASS data were filtered with both linear-phase FIR filter as

well as the minimum-phase IIR filter. Figure 6.13 shows the results obtained from the experiment. In order to have a better understanding of the effect, the IIR filter's frequency response (green) as well as the Group Delay difference between the FIR and IIR filters (red) are plotted on top of each other Figure 6.13. As can be seen from Figure 6.13, the pseudorange for the same GLONASS signal differ up to 200 metres when different frequencies are used for transmitting the GLONASS signal. It is shown in the figure that as the frequency in IIR filter gets closer to the cut-off region the group delay response of the filter increases which is the cause of the pseudorange error.

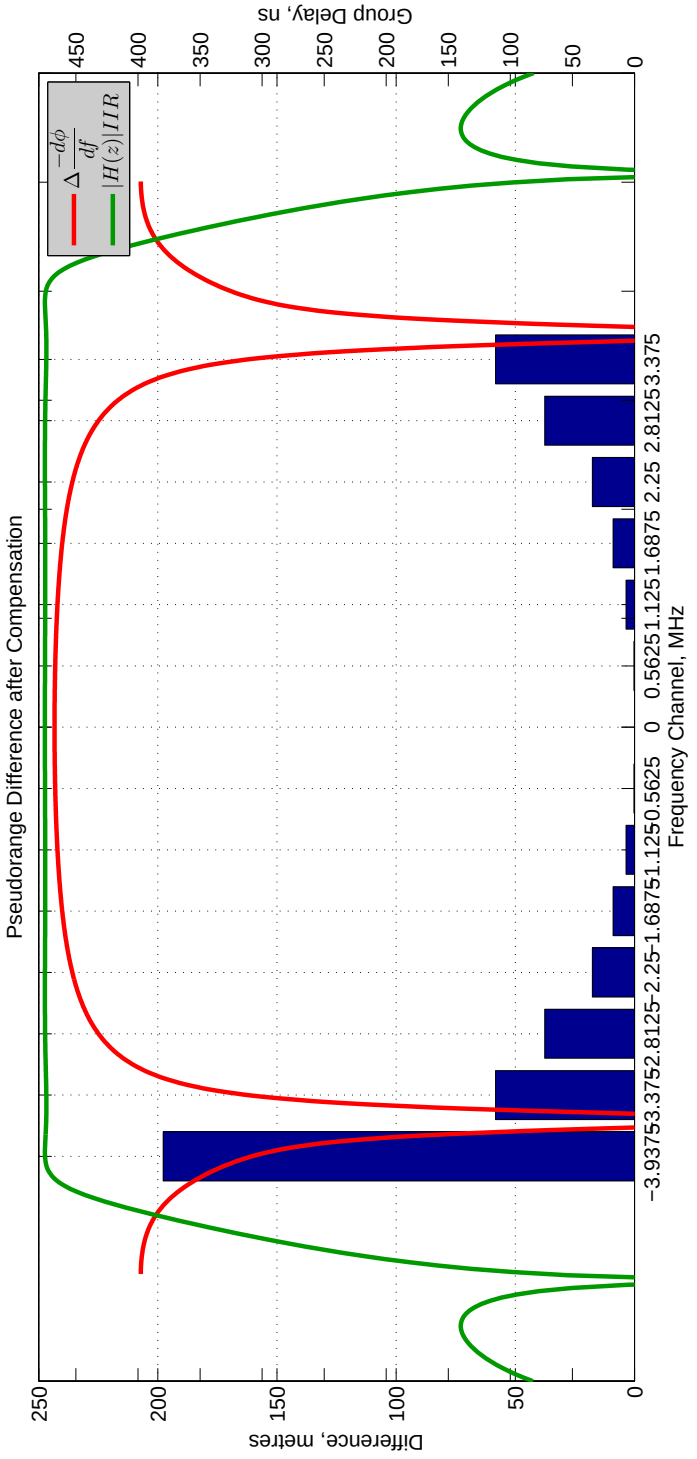


FIGURE 6.13: GLONASS Pseudorange difference between linear-phase FIR & minimum-phase IIR filters

6.4 Pseudorange Measurement Correction

Figure 6.13 shows how the pseudorange measurements varies for different GLONASS satellite transmitting frequencies. Due to big pseudorange differences this needs to be corrected in order to ensure a reliable user position with minimal decimator complexity. There are various techniques that will be reported in this section aiming to correct the variation in pseudorange measurements across the GLONASS band. The proposed methods are listed as follows:

- Group delay compensation of the IIR filter
- Polynomial fit to the pseudorange measurement error
- Combined table look-up & line approximation

6.4.1 Test Setup

All the measurements have been performed using artificially generated data with real navigation message embedded. This was essential in order to ensure the consistency for different transmitting frequencies and different proposed methods. Then the generated data was filtered with FIR and IIR filters for the same decimation combination of 8 by 3. Also in order to measure the effects of Doppler shift, each signal set was synthesized with Doppler shift of -10 kHz, -5 kHz, 0 Hz, 5 kHz, and 10 kHz. This allows the observation of pseudorange variation as a function of Doppler offset. Afterwards, the data was processed by performing an acquisition and tracking for each GLONASS frequency band for FIR and for IIR filtered data. Compensation of the pseudorange

was performed using each of the proposed methods was undertaken. The pseudorange was obtained in the conventional manner. This range was then compensated using each of the 3 proposed methods. These methods are explained in the following sections in more detail.

6.4.2 Group delay compensation

This proposed method saves the IIR filter's group delay in a look-up table. The Doppler shifted centre frequency of the signal is used to determined the position in the table. Then, during pseudorange calculation the group delay can be read from the look-up table and subtracted from the actual pseudorange. The group delay, that is read from the look-up table, from time to distance. This is subtracted from the calculated pseudorange.

In this method, the look-up table should contain sufficient data points in order to be able to correct the pseudoranges. Storing group delay of an IIR filter only at the GLONASS transmitting frequencies is not enough because it should also include the group delay values for the Doppler shift. Then the look-up memory size is proportional to the resolution of the Doppler shift at each frequency band. Using a resolution of 100 Hz Doppler shift requires 201 x 14 address size for the look-up table (there are 201 frequencies between –10 kHz and 10 kHz at 100 Hz intervals and there are 14 different satellites).

Figures 6.14, 6.15 and 6.16 show the results after correcting the pseudorange differences between an FIR and IIR filtered signals using group delay compensation method, each

with different code offset. Using different code offset shows how the correction changes for different pseudorange distance between the receiver and the satellite.

As it can be seen from the figures, using the group delay of the filter to correct the pseudoranges cannot fully compensate the error. Especially compensating for the frequency channel -7, which is close to filter cut-off, had an error around 13 metres.

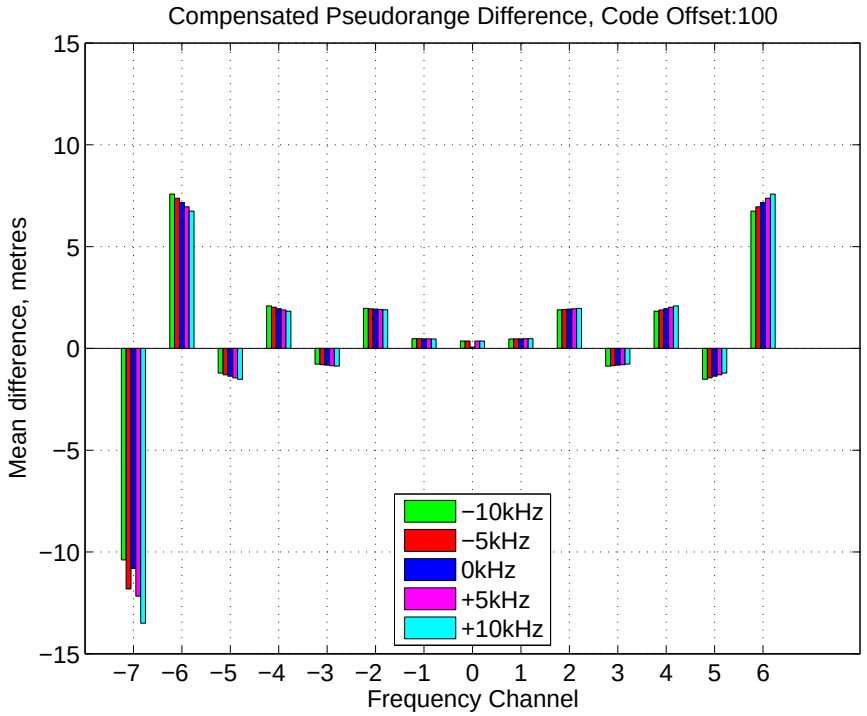


FIGURE 6.14: GLONASS Pseudorange correction using filter's group delay subtraction method for code offset 100

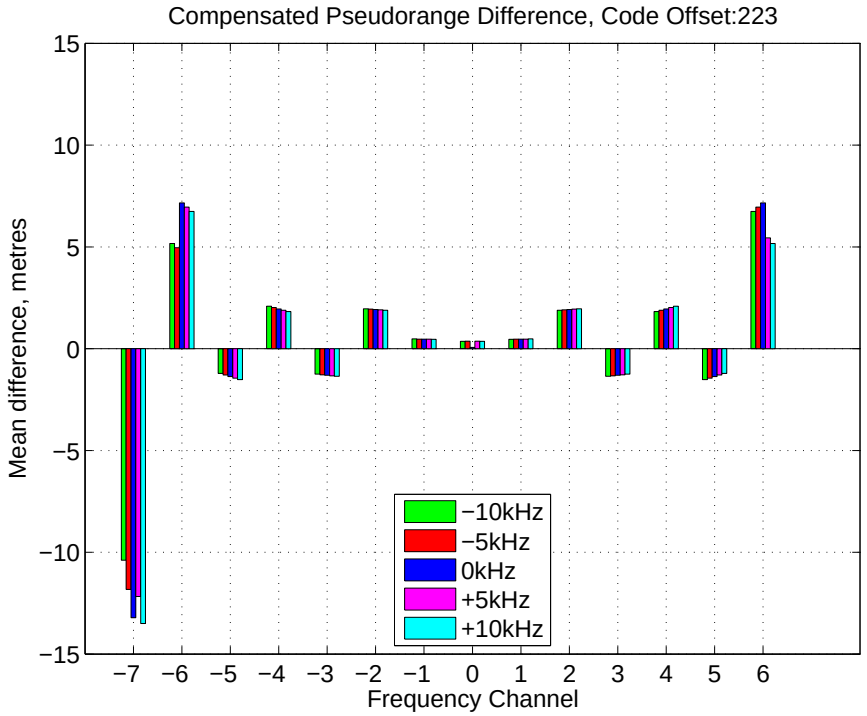


FIGURE 6.15: GLONASS Pseudorange correction using filter's group delay subtraction method for code offset 223

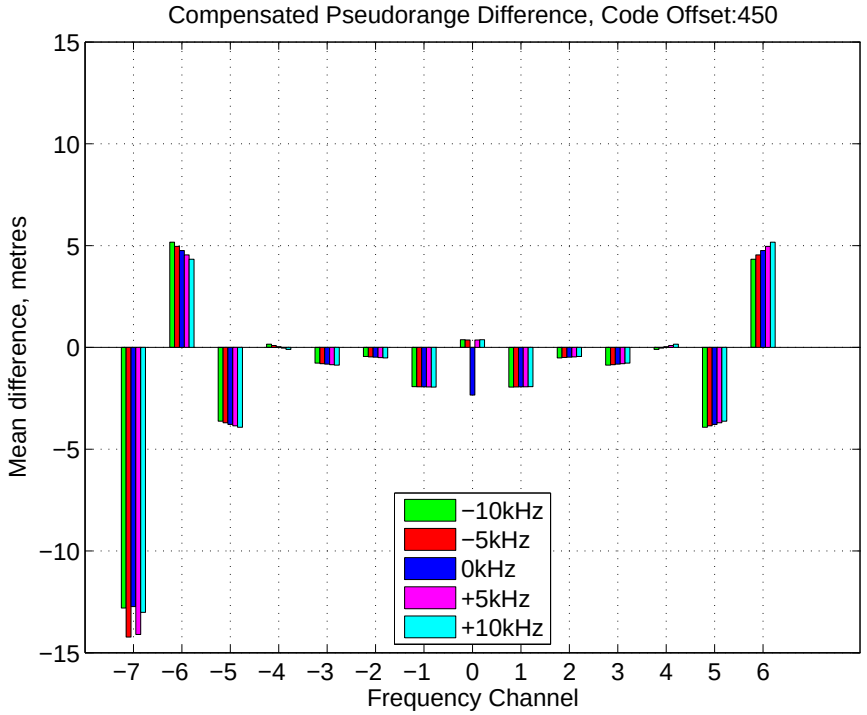


FIGURE 6.16: GLONASS Pseudorange correction using filter's group delay subtraction method for code offset 450

6.4.3 Polynomial fit compensation

The second proposed method was to fit a polynomial curve on the pseudorange difference profile. This method relied on existing pseudorange differences between the FIR and IIR filtered signals. Once the pseudorange error was known, the polynomial curve was fitted to the error profile. The Doppler-shifted centre frequency of the incoming signal was then substituted into the correction polynomial and the resulting correction subtracted from the calculated pseudorange. In this case, the effectiveness of this correction method is dependent on how good the polynomial curve fitted to the pseudorange difference. Also in order to have a good correction, it was essential to experiment with various code offsets. This gave a good range of pseudorange differences. An average was taken and this used for the polynomial curve fit. The performance of the pseudorange correction greatly depended on the order of the polynomial curve. The higher the order, the better the correction.

Figures 6.17, 6.19 and 6.21 show the results of the polynomial curve fitting, each with different code offset for a 3rd order polynomial and Figures 6.18, 6.20 and 6.22 shows the variances of the pseudorange difference at each frequency channel. The 3rd order polynomial equation is given in Equation 6.2. As can be seen from the figures, using third order polynomial did not improve the pseudorange correction compared with the previous method. This is because third order polynomial could not fit the required curve well enough. This is shown in Figure 6.23. From the same figure, it can also be observed that the error performance is a one to one match to the polynomial curve.

$$P_3(f) = 0.3f^3 - 2.25f^2 - 6.1f + 248.5 \tag{6.2}$$

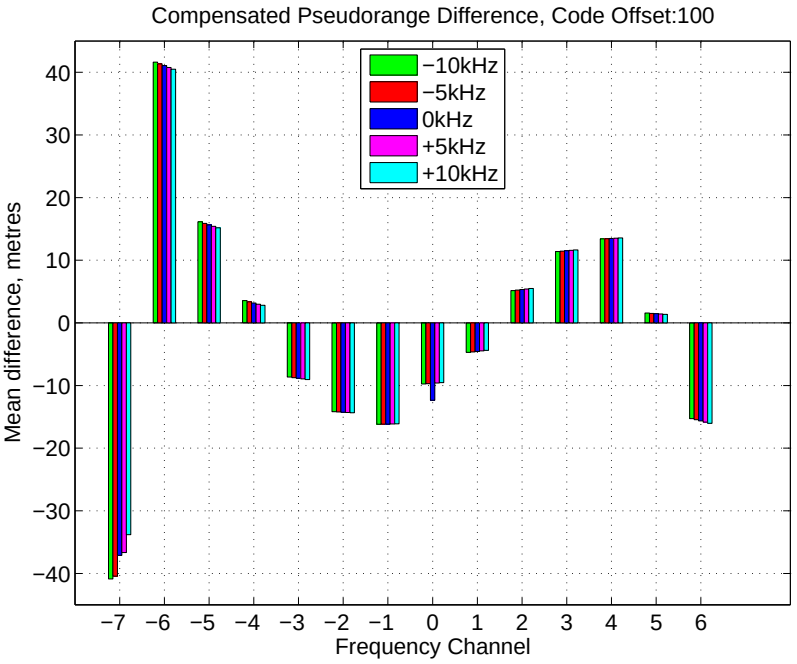


FIGURE 6.17: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 100

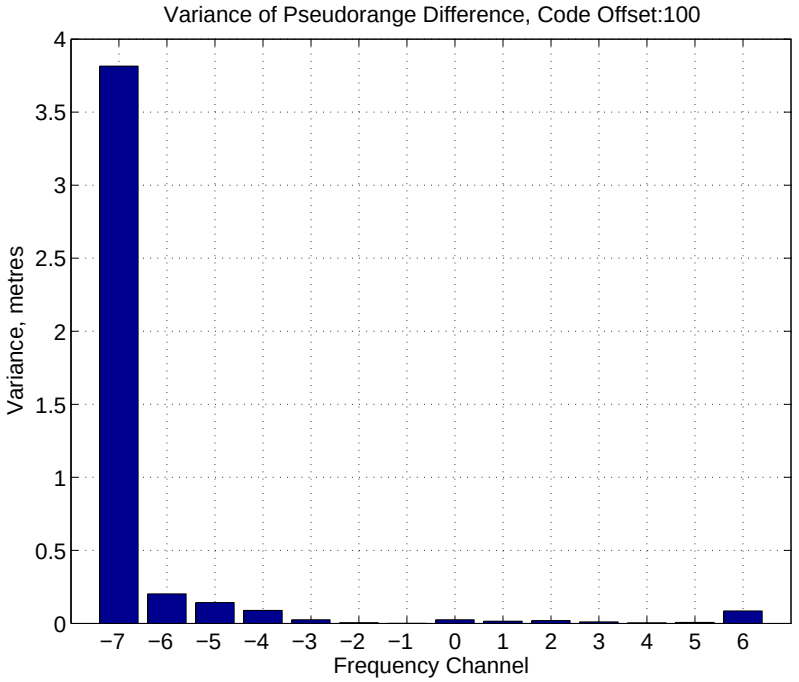


FIGURE 6.18: Variance for code offset 100

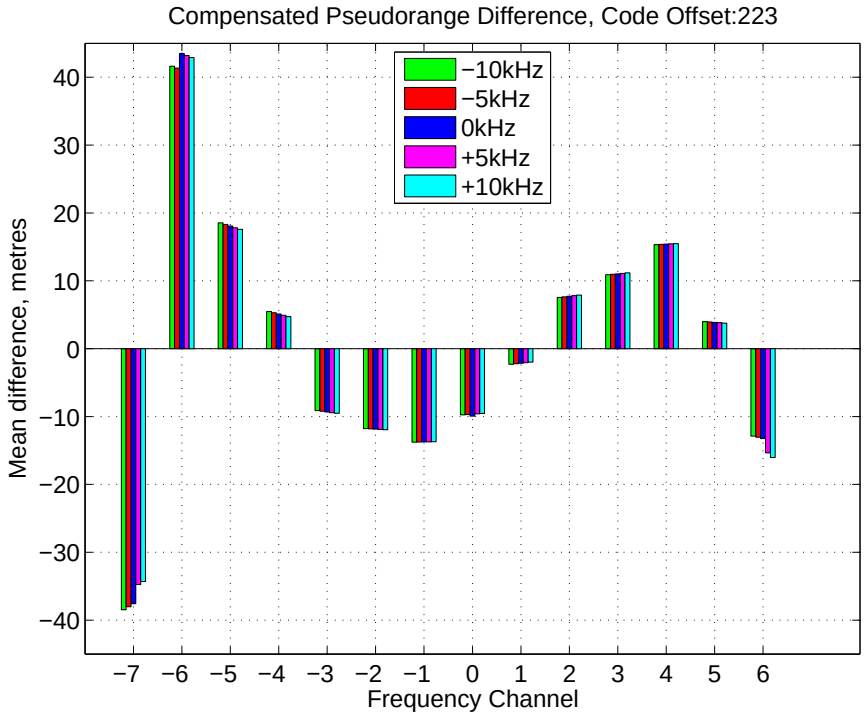


FIGURE 6.19: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 223

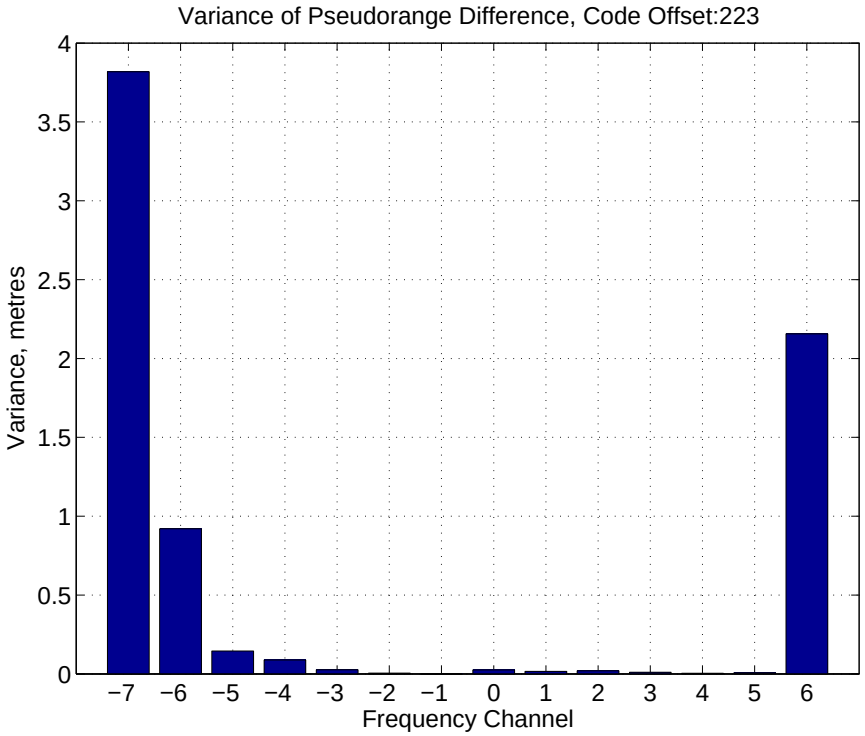


FIGURE 6.20: Variance for code offset 223

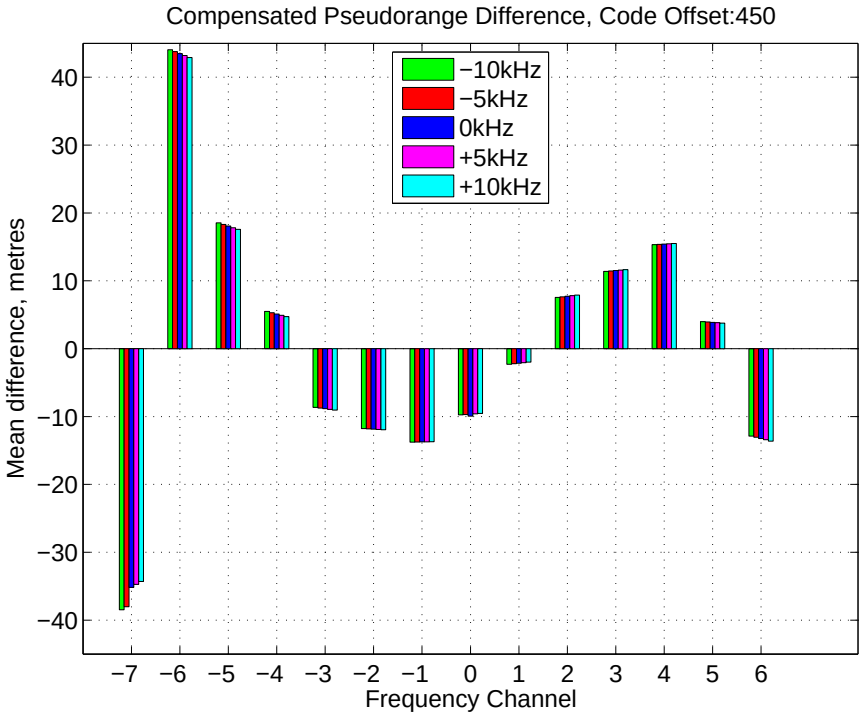


FIGURE 6.21: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 450

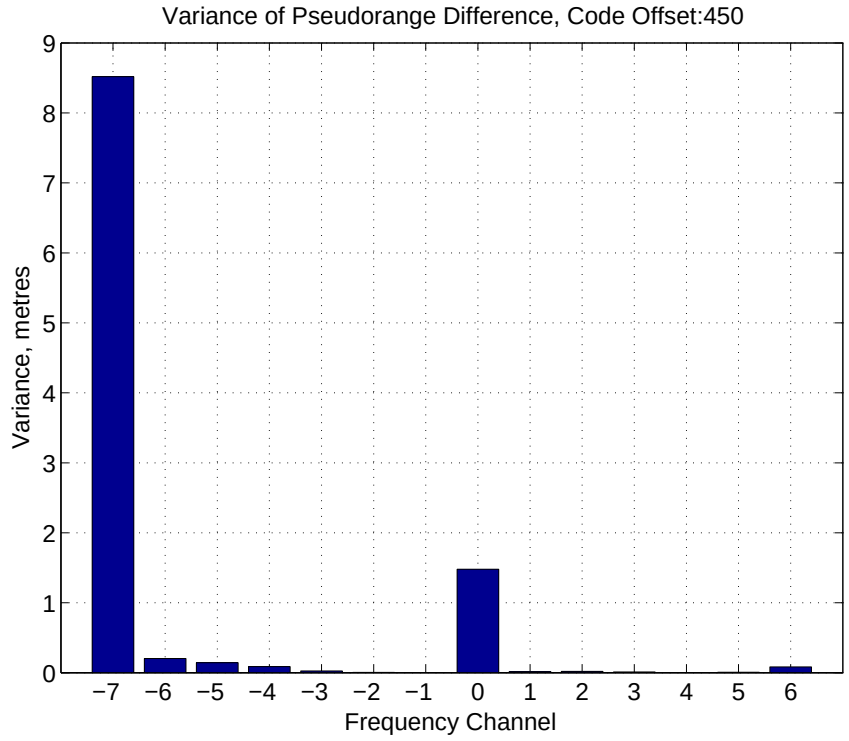


FIGURE 6.22: Variance for code offset 450

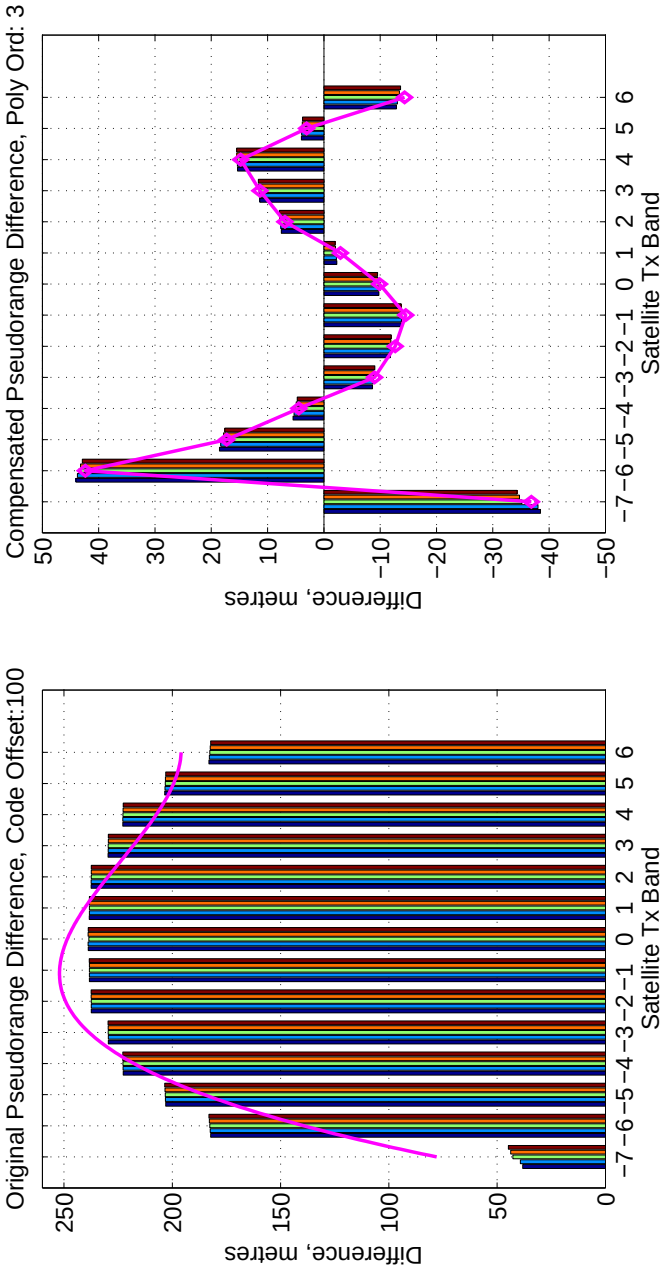


FIGURE 6.23: 3rd order polynomial curve fitting on the Pseudoranges

As can be seen from the figures above, deploying a 3rd order polynomial to correct the pseudorange did not perform well. It resulted in an error as large as 45 metres.

The resulted error was partly because of the error profile's odd symmetry. It can be observed from the Figure 6.23 that the pseudorange difference is symmetrical between channel -6 and channel +6 but not channel -7. Because of this odd symmetry a 3rd order polynomial did not fit well enough to the pseudorange difference. Therefore, in order to find an acceptable performance higher order polynomials have been tested. The next test was to repeat the same experiment with a 5th order polynomial in order to assess how this improved the performance of the pseudorange correction.

Figures 6.24, 6.26 and 6.28 show the results of the polynomial curve fitting and Figures 6.25, 6.27 and 6.29 shows the variances of the pseudorange difference at each frequency channel, each with different code offset for a 5th-order polynomial. The 5th order polynomial equation is given in Equation 6.3. It can be seen that using a 5th-order polynomial improves the pseudorange correction compared with the 3rd order polynomial at the expense of increased complexity. The polynomial is shown in Figure 6.30. From the same figure, it can also be observed that the error performance is a one to one match to the polynomial curve.

$$P_5(f) = 0.015f^5 - 0.049f^4 - 0.615f^3 + 0.006f^2 - 4.656f + 236.4 \tag{6.3}$$

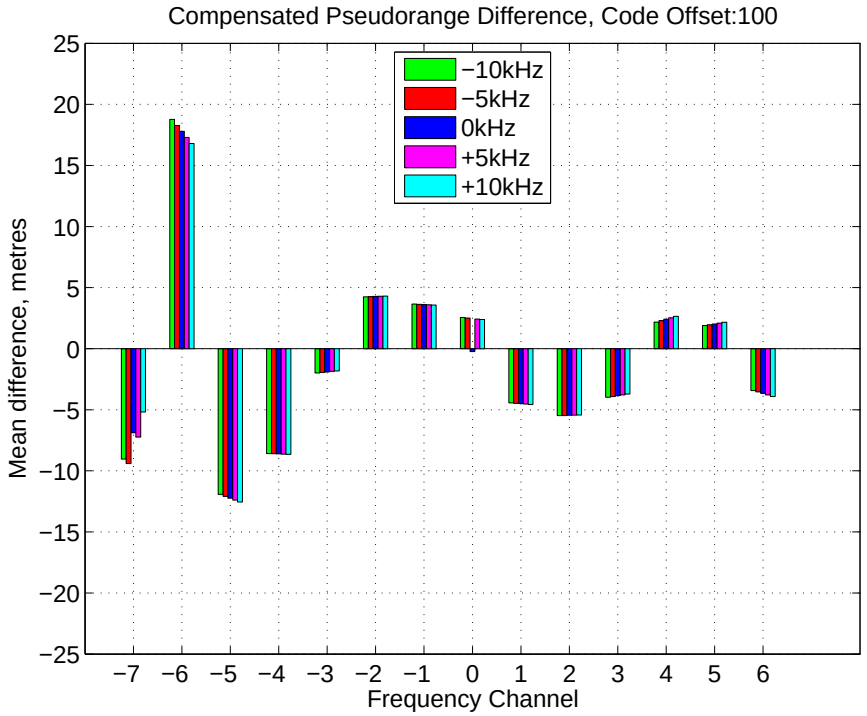


FIGURE 6.24: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 100

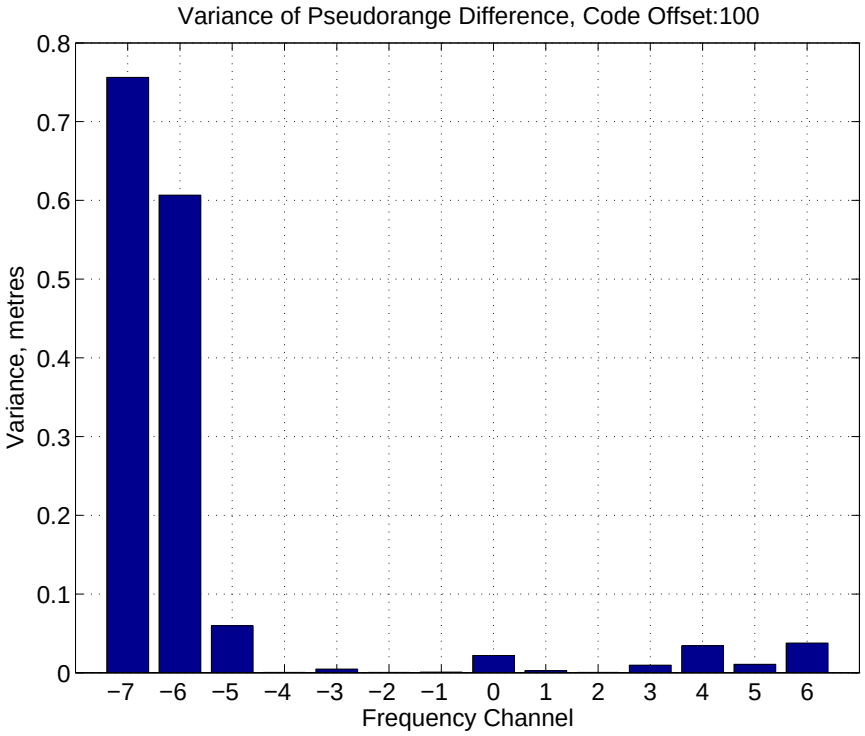


FIGURE 6.25: Variance for code offset 100

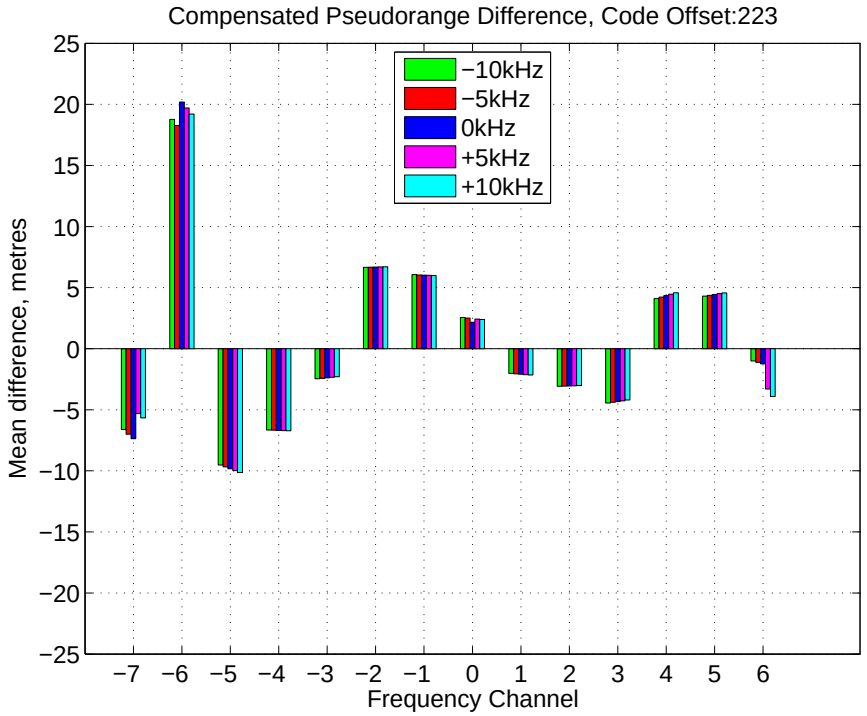


FIGURE 6.26: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 223

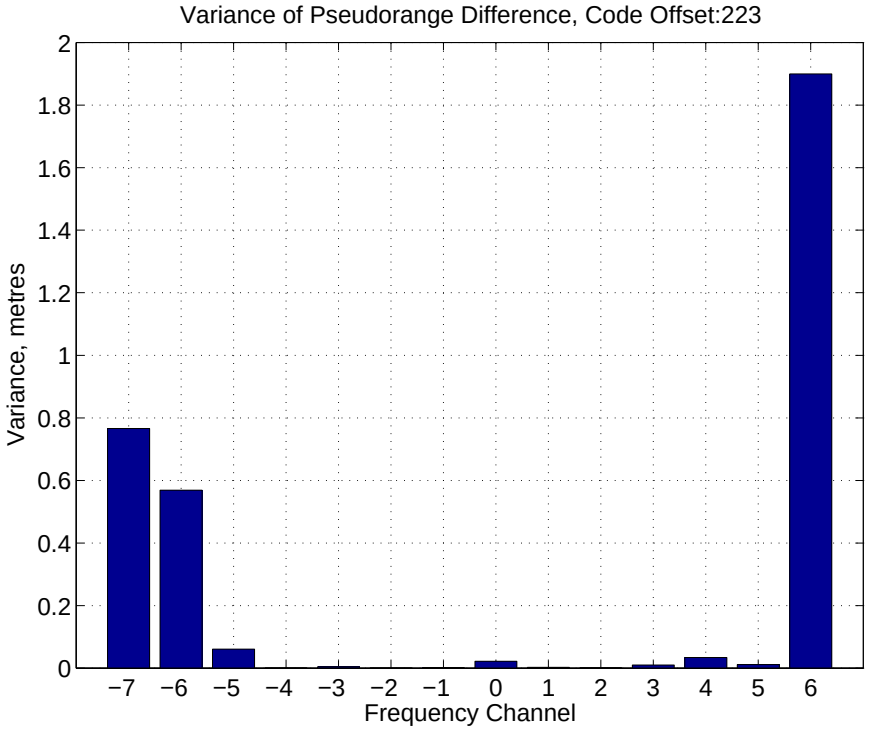


FIGURE 6.27: Variance for code offset 223

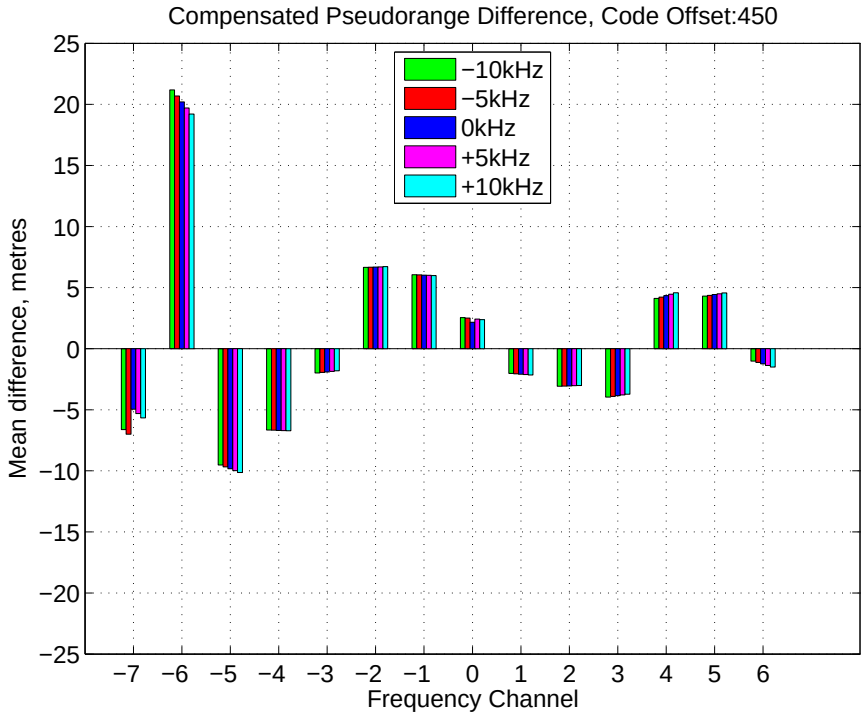


FIGURE 6.28: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 450

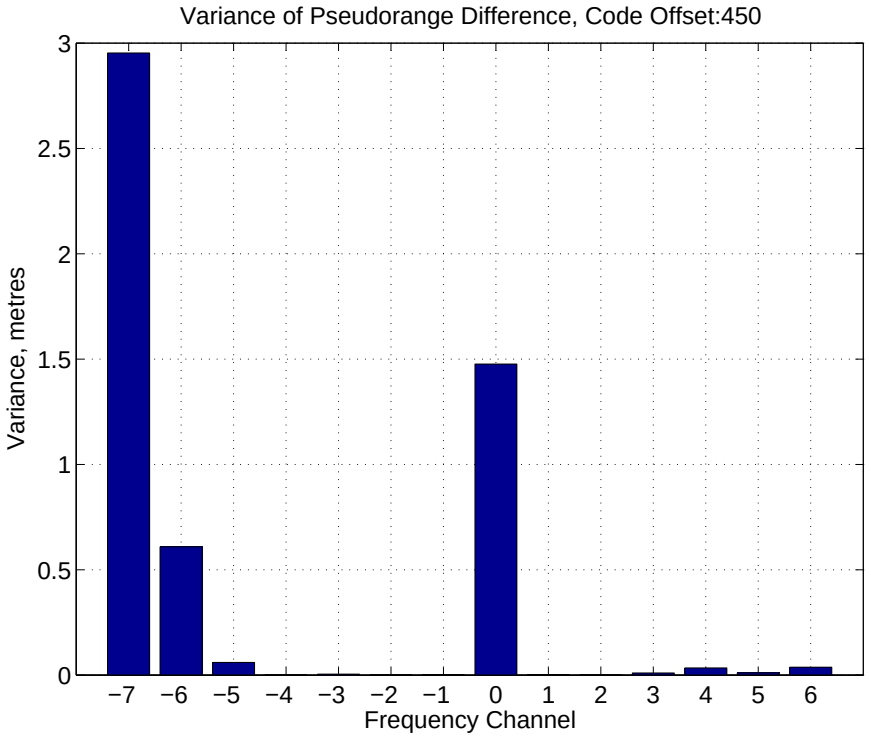


FIGURE 6.29: Variance for code offset 450

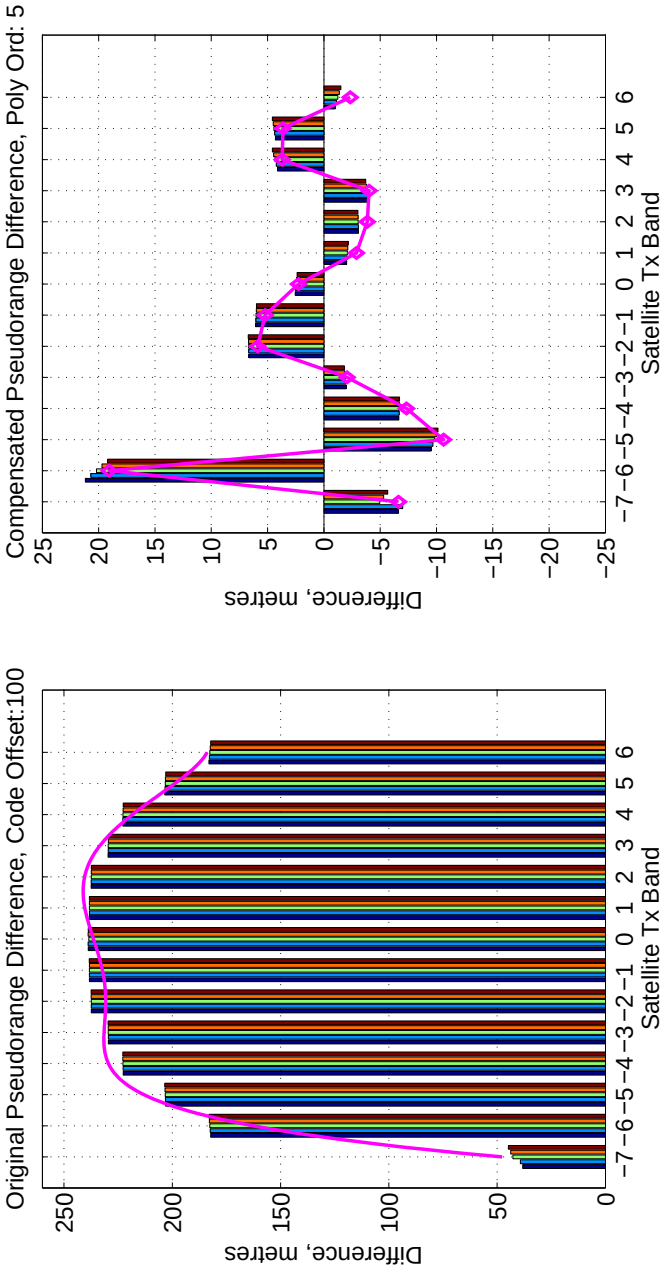


FIGURE 6.30: 5th order polynomial curve fitting on the Pseudoranges

The same test is then repeated for the last time with a 10th order polynomial in order to get a reasonable correction. The results are given in Figures 6.31, 6.33 and 6.35 with

variances of the pseudorange difference in Figures 6.32, 6.34 and 6.36. The 10th order polynomial equation is given in Equation 6.4. As can be seen from the figures, using a 10th order polynomial gives excellent correction with an error of less than 5 metres. However, using a 10th order polynomial is computationally expensive and so is not a low-power solution. The polynomial is shown in Figure 6.37. From the same figure, it can also be observed this time the error performance is not a one to one match to the polynomial curve. This is because the pseudorange correction polynomial is calibrated to work on the average of different code offsets with different error profiles.

$$P_{10}(f) = -4.16 \times 10^{-6} f^{10} + 1.68 \times 10^{-5} f^{9} + 0.0004 f^{8} - 0.001 f^{7} - 0.013 f^{6} + 0.031 f^{5} + 0.13 f^{4} - 0.267 f^{3} - 1.25 f^{2} + 0.596 f + 238.9 \quad (6.4)$$

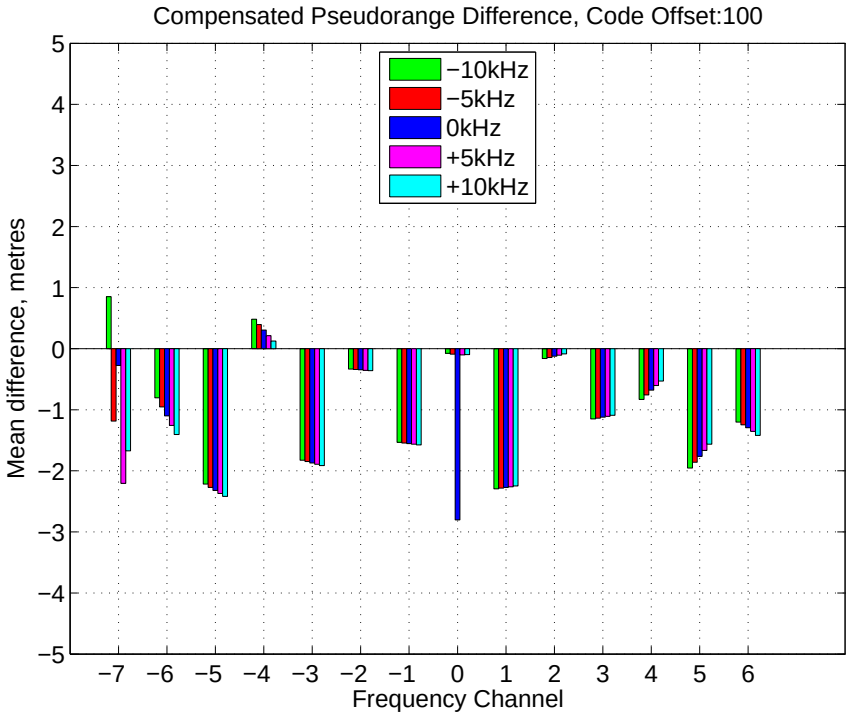


FIGURE 6.31: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 100

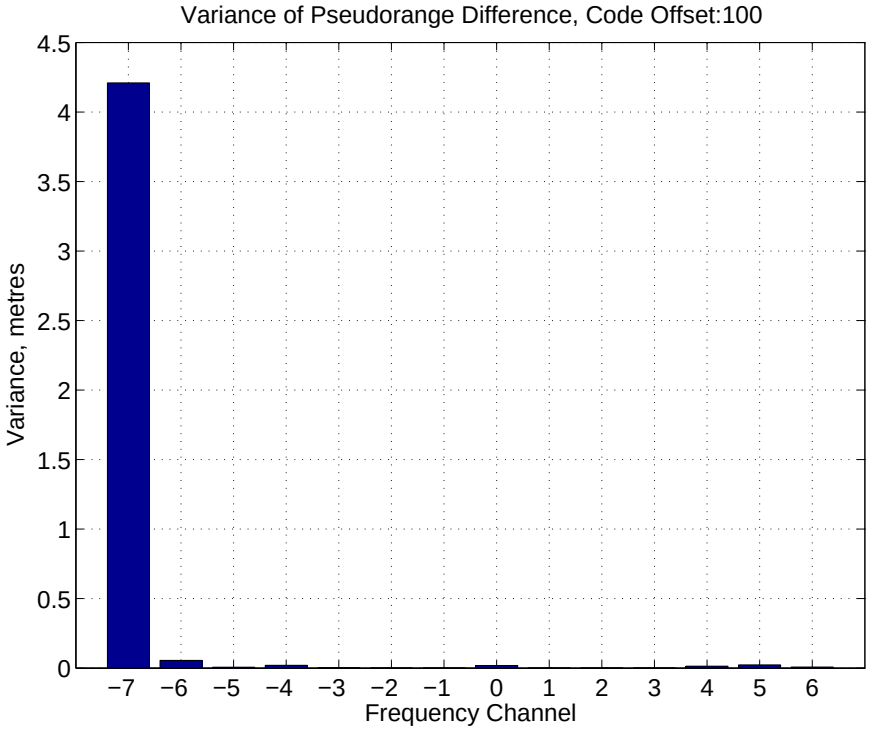


FIGURE 6.32: Variance for code offset 100

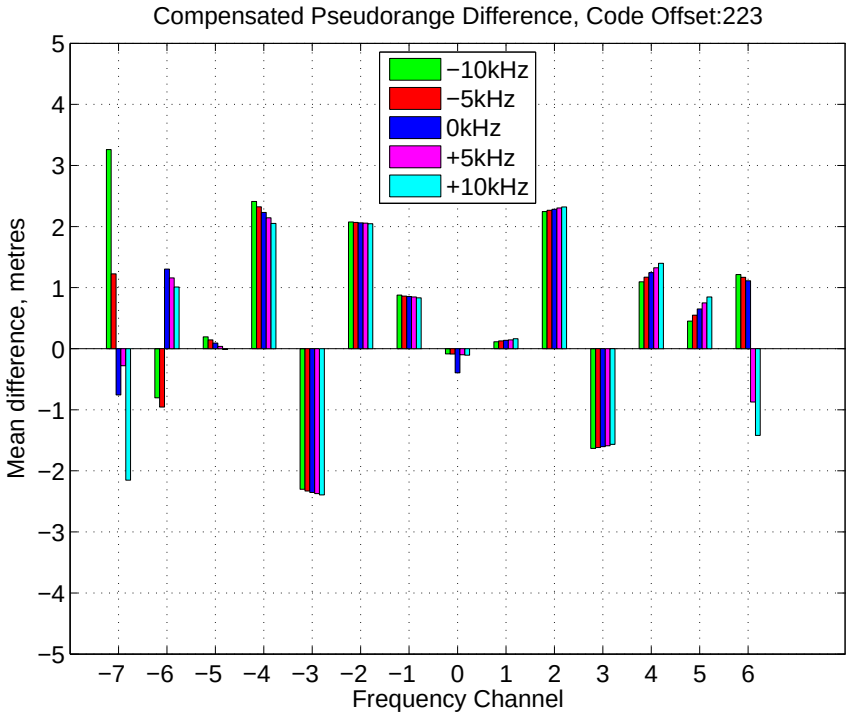


FIGURE 6.33: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 223

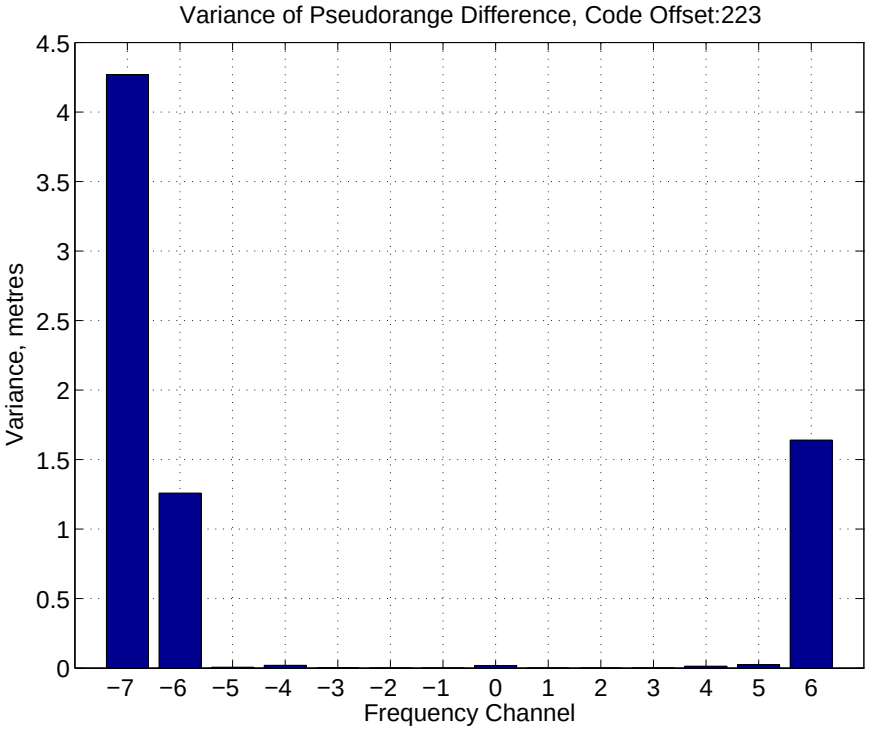


FIGURE 6.34: Variance for code offset 223

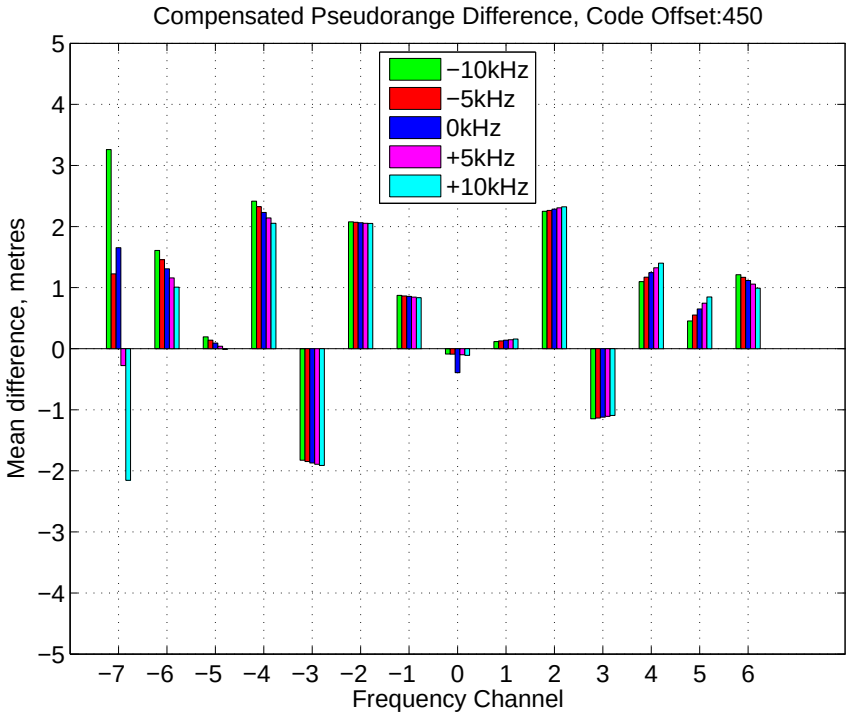


FIGURE 6.35: GLONASS Pseudorange correction using polynomial curve fitting subtraction method for code offset 450

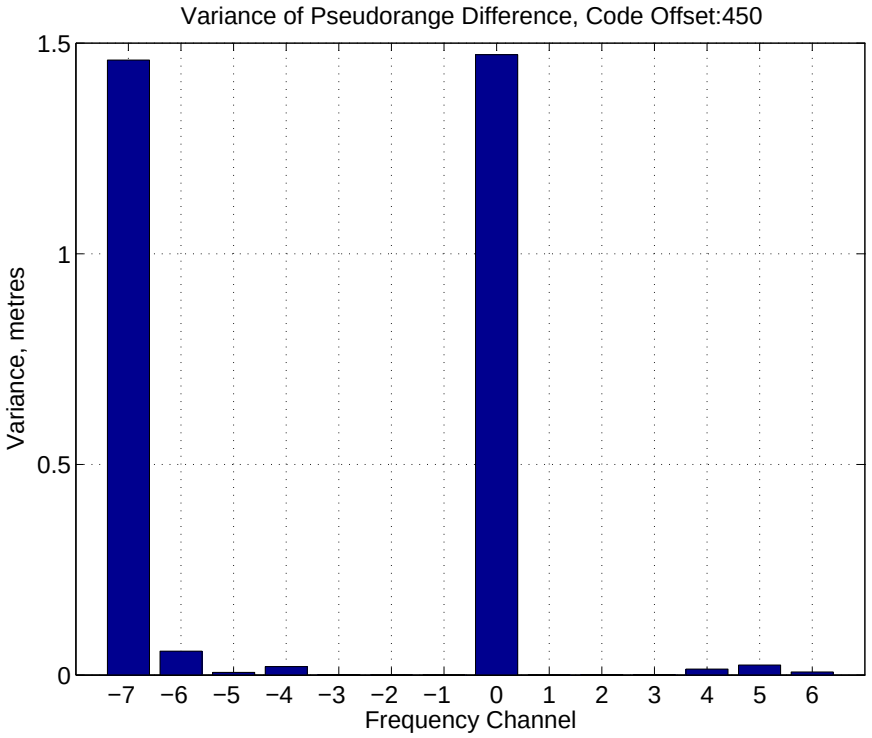


FIGURE 6.36: Variance for code offset 450

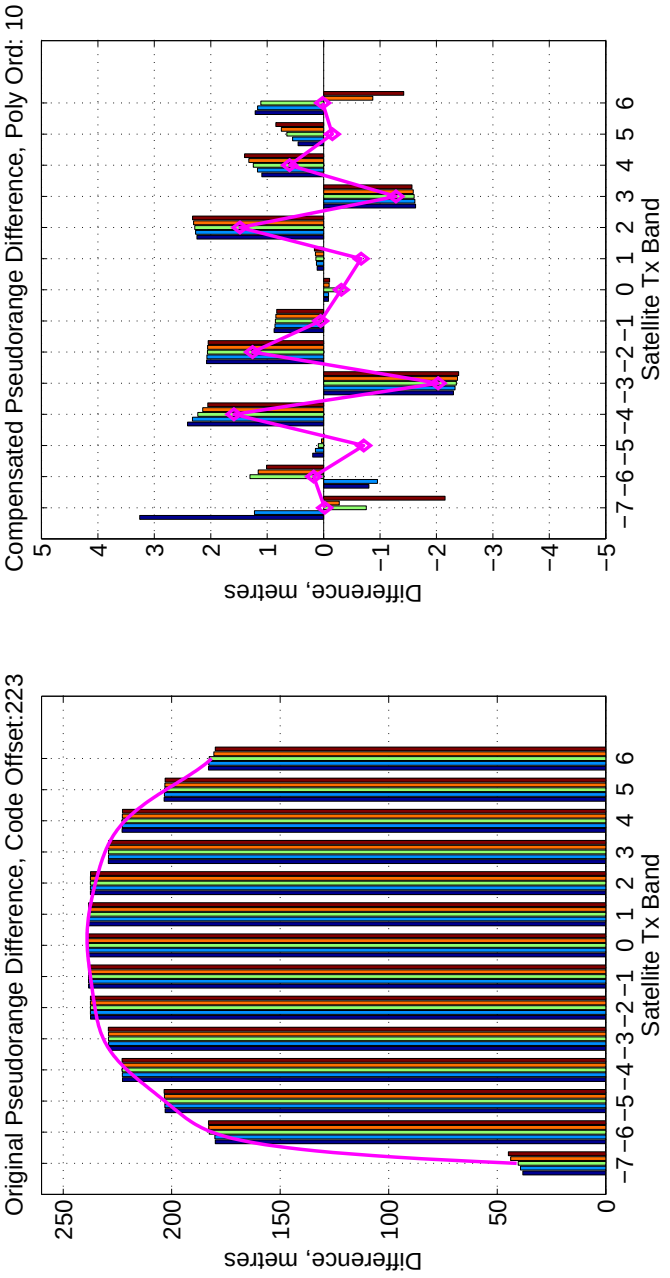


FIGURE 6.37: 10th order polynomial curve fitting on the Pseudoranges

6.4.4 Table look-up linear approximation

Although the previous method of using a 10th order polynomial function corrects the pseudorange errors, it was not a low-power solution. So an alternative method is proposed. Instead of using a high-order polynomial for all the frequency channels, a low order polynomial is sufficient to correct the effect of the Doppler shift if the frequency channels were corrected separately. So the last proposed method is to use a small look-up table as a function of the GLONASS channel to which is added straight line approximation of the effect of the Doppler shift in order to correct the pseudorange. The slope of the Doppler correction is also a function of the channel so the total table requires only 14x2 entries (1 slope and 1 offset for each 14 different satellites). The correction term is then simply

$$d_c = a(n_c) + b(n_c).f_d \tag{6.5}$$

where d_c, n_c and f_d are Doppler correction term, channel number and Doppler frequency respectively and a and b are constant and slope of the line approximation. The values of a and b were derived from the pseudorange error profile.

Each frequency channel is treated individually and the pseudorange error was corrected using a straight line approximation. Thus only one multiplication and one addition is required to correct the impact of the filter's phase non-linearity. Figures 6.38, 6.39 and 6.40 show the pseudoranges after they are corrected with the straight line approximation method.

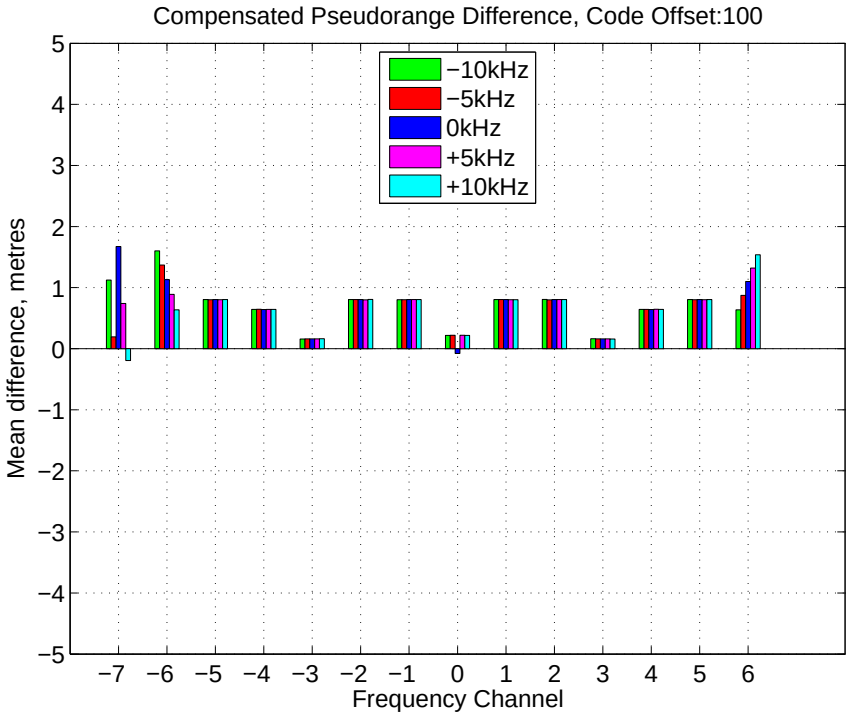


FIGURE 6.38: GLONASS Pseudorange correction using straight line approximation method for code offset 100

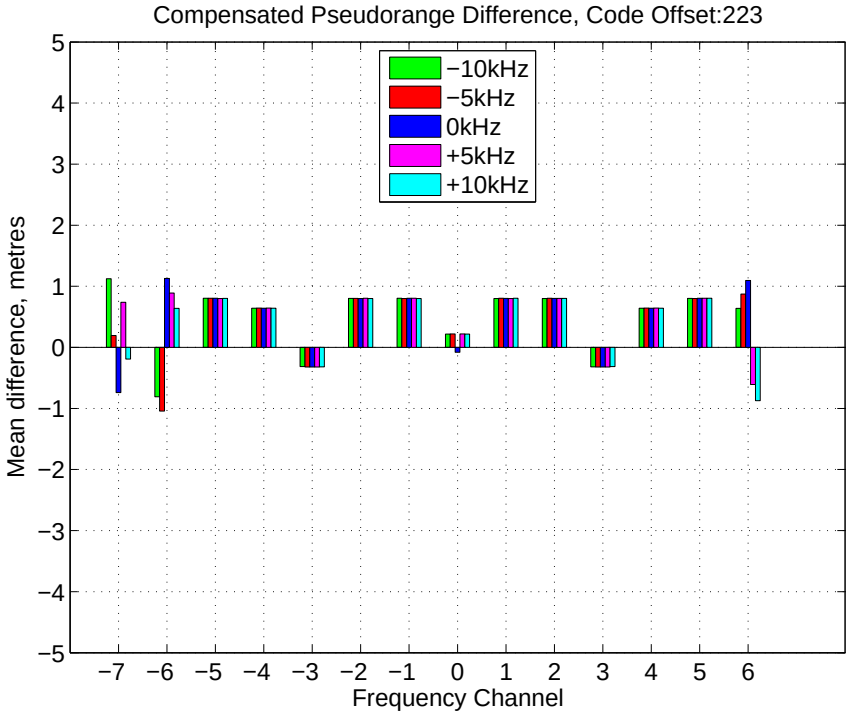


FIGURE 6.39: GLONASS Pseudorange correction using straight line approximation method for code offset 223

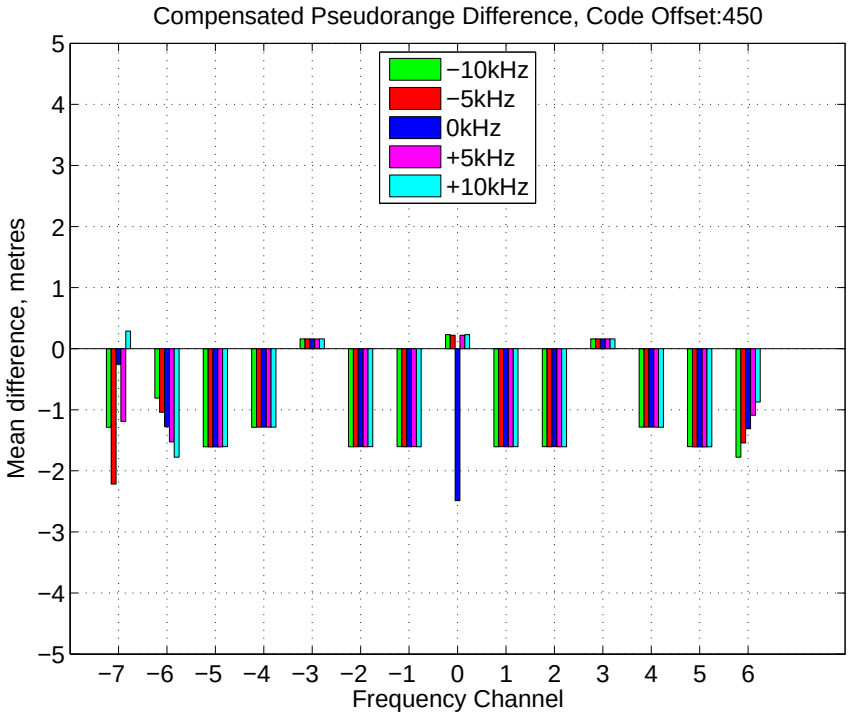


FIGURE 6.40: GLONASS Pseudorange correction using straight line approximation method for code offset 450

It can be seen from the figures that the linear approximation method corrected the pseudorange estimation that showed a better compensation performance compared with the 10th order polynomial method. However, the required computational load is much lower. Comparing the performance, in the measurements with all code offsets, all the pseudoranges were estimated with less than 2 metres difference. However, from the figures it can be observed that at some particular frequency channels, especially at channels -7,-6 and 6 the corrected pseudorange is less effective. This is because those frequencies are close to the filter's cut-off where the group delay changes rapidly. Because of that the linear approximation is unable to correct for every different code offsets.

6.5 Chapter Conclusion

This chapter presented the results of using different filter types with different decimation ratio combinations, establish the positioning accuracy. It has been established that the positioning performance does not deteriorate when using an IIR filter which has non-linear phase. Also, different decimation ratio combinations do not impact on the final receiver position. This leads to two important conclusions: Firstly, by using different decimation stages, as oppose to single stage filtering, the same positioning performance can be achieved while saving significant power dissipation and hardware utilisation as demonstrated in Chapter 5. Secondly, using a minimum-phase IIR or an almost-linear-phase IIR filter does not worsen the final receiver positioning performance. It has been shown that there is no correlation between the phase non-linearity and the positioning error when the experiment has been carried out on GPS L1 C/A signal.

This chapter also presented performance evaluation via pseudorange measurement. Two different measurements were performed. The set of experiments measured the pseudorange difference by applying a set of Doppler frequencies for a GPS L1 C/A signal and then filtered with two extreme filter types; a linear-phase FIR filter and a minimum-phase IIR filter. The results showed that the phase non-linearity does not play a role on the final user position. The second set of experiments repeated the same experiment but used a GLONASS L1 signal and then filtering with these two type of filters. This time, the results showed that, when a minimum-phase IIR filter was deployed for decimation, the pseudorange measurements were changed greatly. This was due to the fact that GLONASS uses an FDMA channel access technique. This

means that, if two satellites were transmitting from the same location but if they were using two different frequency channels, then their pseudorange measurements could differ up to 200 metres.

The final part of the chapter proposed various methods of correcting the pseudorange errors caused due to the non-linear phase of the IIR filters deployed. Three different approaches were considered. All the proposed methods subtracted a correction term during the pseudorange calculation. The first proposed method was to deduct the group delay of the filter since the filter response is fixed. However, the performance was not good enough. The second method was first to perform an experiment and establish the pseudorange variation between FIR and IIR filtered data and then to fit a polynomial curve on this error profile. Various polynomial orders were considered and it has been established that at least a 10th order polynomial is required . However, this increases the complexity of the overall solution of using an IIR filtered system instead of an FIR one. The final proposed solution has overcome this complexity problem by replacing the high-order polynomial with individual straight line approximations for each GLONASS frequency channel which is essentially a 1st-order polynomial. It has shown that the final method outperformed the previous methods in terms of pseudorange correction performance as well as complexity.

Chapter 7

FPGA based Decimation Filter Processor Design

This chapter presents low–power implementation of the filter models that are reported in Chapter 5. Similar minimum-phase IIR filters as well as Slink decimators were used in order to perform the decimation process. The test and validation of the hardware design concept was performed by utilizing a low–frequency model was targeted for a Continuous-Time (CT) $\Sigma\Delta$ modulator. The filters and decimation methods are also used in GNSS as well as many other systems. This work was published at a conference [70].

7.1 Specification of the decimation filter process

The specification used for this implementation model is shown in Table 7.1 and the decimation stages with corresponding bandwidths are given in Figure 7.1. It shows the stages of decimation with their corresponding decimation ratios and with the required frequency responses at each stage.

TABLE 7.1: Specification of the C-T ΣΔ Modulator

ΣΔ Order	3^{rd} order
Frequency range	300 Hz - 10 kHz
Dynamic range	86 dB
Maximum input voltage	125 mV single/250 mV differential
Sampling rate	2.56 MHz
Over sampling ratio	128

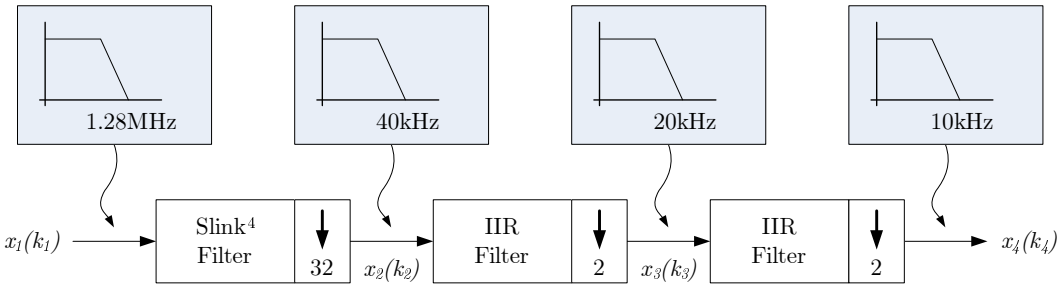


FIGURE 7.1: Decimation by stages and corresponding bandwidth

As it can be seen from Figure 7.1, it was established that a 3-stage classical decimation chain was sufficient here. The overall passband and stopband distortion of the entire decimation chain was set to be 0.1dB and -90dB respectively.

7.2 Slink Decimator Implementation

An efficient way of implementing the slink filter is as shown in Figure 7.2 where the down sampler is moved in between the accumulator and the differencer which saves N-1 delayers. It should be noted that the arithmetic processing in this structure has to be circular (i.e. two's complement) so that incrementing beyond the maximum positive value can wrap around to the most negative value.

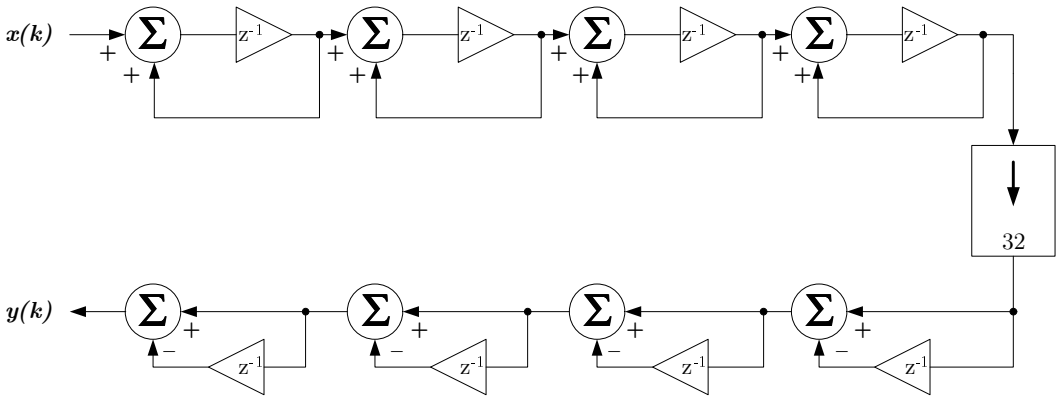


FIGURE 7.2: 4^{th} order slink filter implementation

7.3 Second and Third Stage Decimation

Once the slink decimator has attenuated the out-of-band frequencies, the signal was further decimated by four in order to obtain the required overall decimation ratio of 128. It is more computationally efficient to perform this decimation in two stages as demonstrated in Chapter 5.

For these setups, Polyphase All-Pass based IIR filters were used. These filters have a minimum phase response and hence minimized group delays compared to FIR filters running at the baseband, delivering high fidelity with micro-bell pass band ripples and

very deep stop band attenuation. The Filter coefficients have been derived using the approach given in [62]. In Figure 7.3, is that of a two-path Polyphase band splitter.

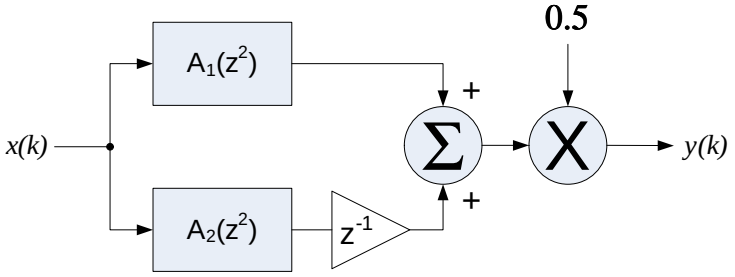


FIGURE 7.3: Two-path Low Pass Polyphase band splitter

Both upper and lower branches of the filter use Numerator-Denominator (N-D) TDL structures. They are used in their Half-band form which has excellent dynamic range [65]. Figure 5 shows a 2nd order N-D TDL structure in its Half-band form. As it can be seen from the Figure 7.4 this structure requires 4 delayers, 1 multiplier, 1 subtractor and 1 adder.

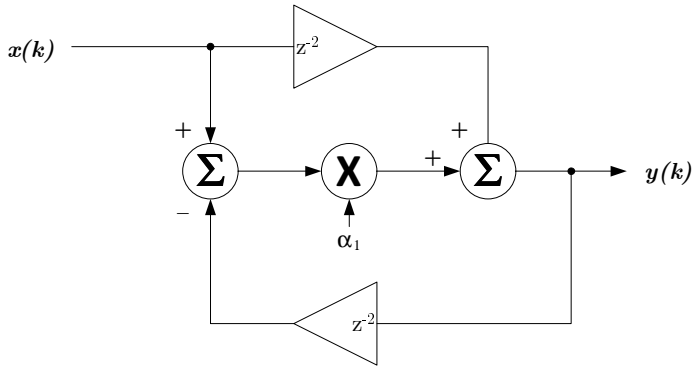


FIGURE 7.4: 2nd order N-D TDL Half Band filter structure

With the given specification a 13th order Polyphase lowpass filter was required. This is realized by cascading 3 N-D TDL Half-band filters in each path. Furthermore, the cascaded filters share the feedback state stores thus only 14 state stores are required rather than 24 state stores.

7.4 Final Stage Compensation

The last stage of the decimation process was to cascade another filter right after the Half-band filters at the third stage in order to compensate the slink roll-off in the pass band region. The desired response of this filter is ideally the inverse of the slink filter ($1/\text{slink}_4(32, \nu_1/32)$) within the band of interest (i.e. up to 10 kHz). Figure 7.5 shows the structure of the slink roll-off compensator that was used to approximate the response required for the roll-off compensation. This structure is based on the Difference Multiply Accumulate (DMAC) structure of the All-Pass processor structure as shown in Figure 7.4 with slight modification. Its response within the band of interest can be seen in Figure 7.6 (cyan) and it can be seen from the Figure 7.6 that using alpha=1/9 the overall response is almost flat in the pass band [71].

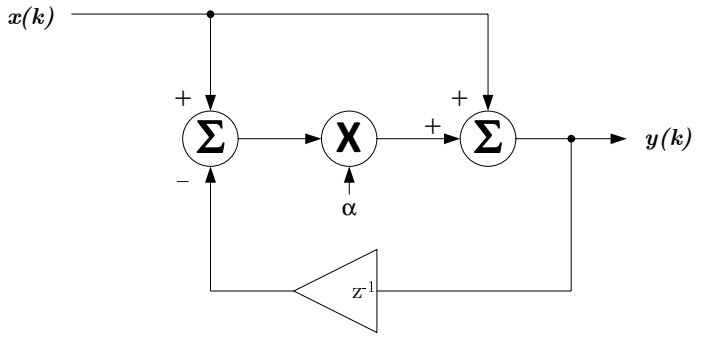


FIGURE 7.5: Structure used to compensate slink roll-off

7.5 Decimation Chain Filter Response

Overall system simulation was performed using MATLAB in order to validate the decimation chain. Figure 7.6 shows the complete decimation chain's magnitude response

at the various stages. As can be seen from the Figure 7.6 the designed decimation chain fit the given specification.

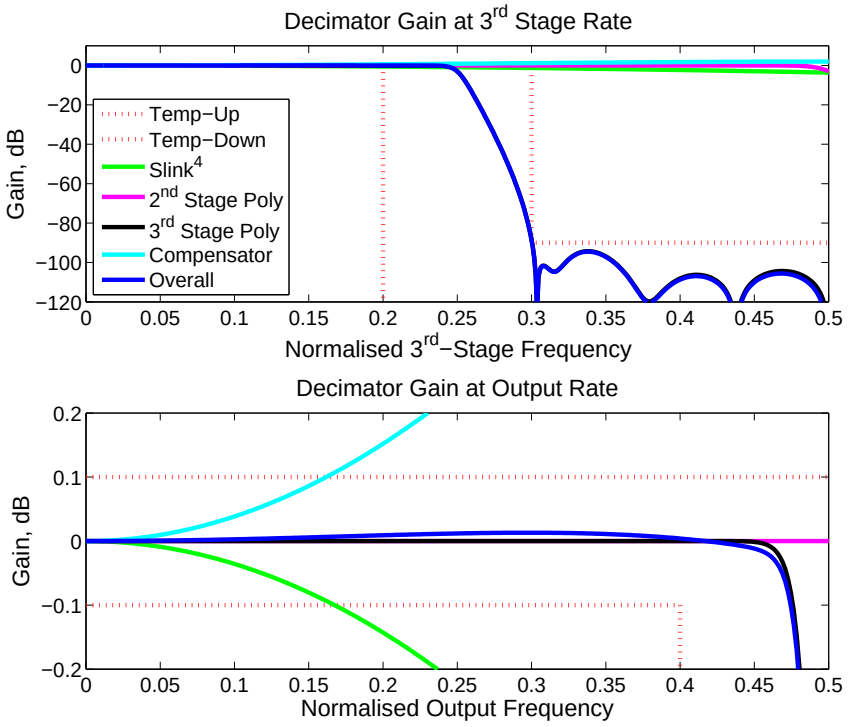


FIGURE 7.6: Decimator gain at the 3rd stage and at the output rate

7.6 Test Parameters

This part outlines the parameters used during the decimation process. Upon arriving at the Slink filter coprocessor to the All-Pass based Decimation and Compensation engine, the bit stream coming from the modulator output is sign extended from 1 bit to 21 bits in order to be able to perform arithmetic operations without losing precision in the decimation chain. At the output of the Slink filter co-processor the data is truncated down to 16 bits with 4 guard bits, where all the data path lengths throughout the rest of the decimation chain was set to 20 bits. The rest of the decimation has been

processed using the ADVRGs proprietary DSP engine. The accumulators have 4 extra guard bits in order to avoid saturation and use convergent rounding quantization to restrict the data path growth.

7.7 Test Setup

The tests have been carried out by configuring an FPGA prototyping the DSP engine as mentioned previously. The analog data is fed to the ΣΔ Modulator as shown in Figure 7.7(b) and the digitized output that the modulator generated is fed to the Xilinx Spartan 3 FPGA development system, Figure 7.7(a), where the decimation process takes place. The DSP engine is controlled with a Host PC using an RS-232 interface. The overall output is captured with a logic analyzer where the captured data was analyzed using the MATLAB environment.

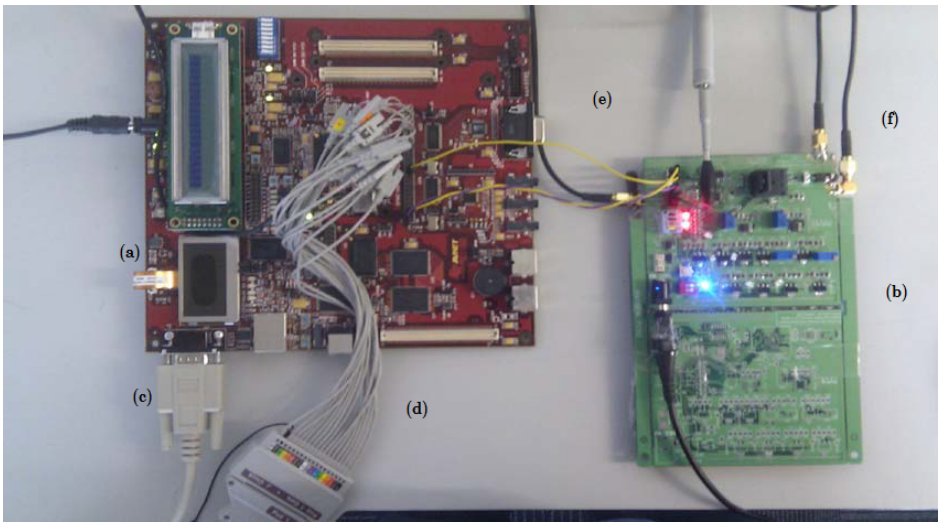


FIGURE 7.7: Test Setup, a)Xilinx Spartan 3 FPGA Development System, b) ΣΔ Modulator, c)RS-232 Serial Interface to a Host PC, d)Parallel probe connecting to the logic analyzer to capture the overall output, e)Data and synchronization signals flowing from the modulator to the decimator, f) Differential Input signal fed from the ultra-low distortion signal generator

7.8 Results

The results presented here were produced by supplying a 6kHz sine wave to the S-D modulator then the modulator's output is fed to the FPGA development board for decimation. 512K samples are captured using logic analyser then analysed using the MATLAB environment by dividing 512K samples into 32K blocks and taking 16 averages. The Power Spectral Density (PSD) is computed by taking 32K point FFT points. Figure 7.8 shows the measured PSD of the modulator output fed to the FPGA.

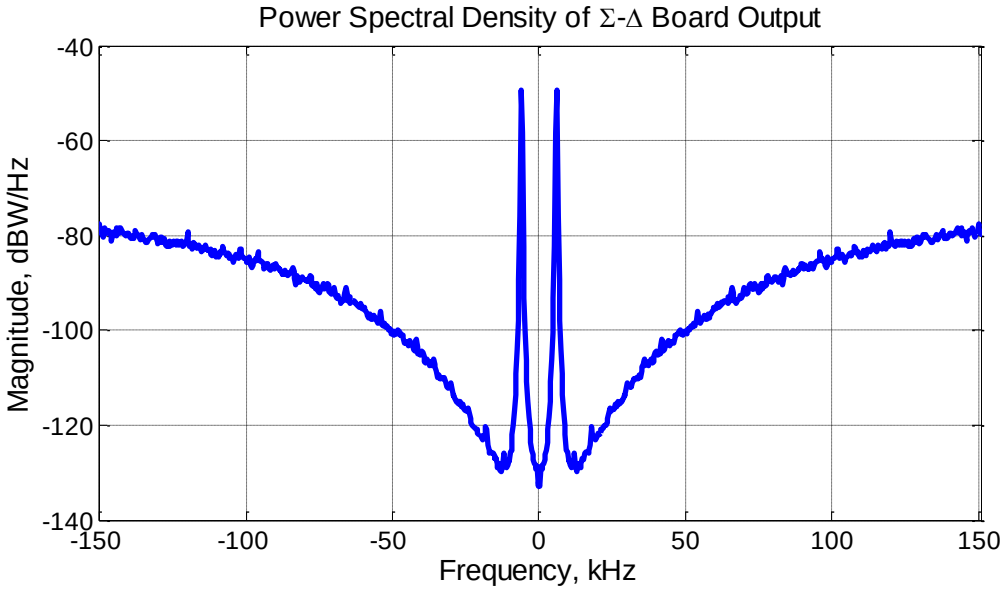


FIGURE 7.8: Measured PSD of $\Sigma - \Delta$ Modulator Output

The Figure 7.9 shows the measured PSD of the final output from the decimator chain. As it can be seen from the Figure 7.9, the decimation chain processor analyses and delivers the modulator output for the 6 kHz sine wave with a noise floor which is approximately -130 dBW/Hz.

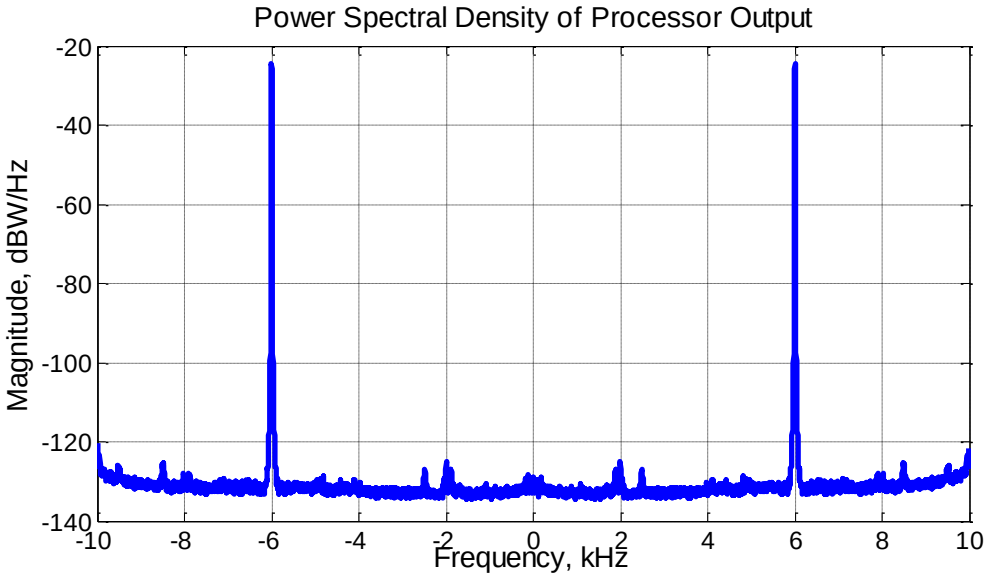


FIGURE 7.9: Measured PSD of Decimator chain Output

7.9 Chapter Conclusion

In this chapter, the overall decimation chain processor that was prototyped on an FPGA platform and used for the measurement of a Continuous Time ΣΔ Modulator has been presented. The results obtained demonstrated that the performance claimed in the Modulator's specification were justified and confirmed through our measurement setup. The oversampled ΣΔ modulator cascaded with a decimation filter chain is also known as an Analog to Digital Converter (ADC) and the results presented here are not just limited to a measurement setup, but can be put together as two IP blocks to form an efficient integrated ADC with minimal effort.

Chapter 8

Conclusions and Future Work

8.1 Conclusions

The main motivation behind this research was to minimise the power consumption as well as reduction in computational complexity of a GNSS receiver which would then maximize the battery life of the mobile devices that are using positioning systems. The work reported in this thesis first proposed a modified tracking loop processor which keeps track of the satellites with reduced computational complexity compared with available solutions. Then a power estimation tool has been developed that enables the user to estimate the power dissipation and hardware utilisation of a digital design without requiring to design the detailed hardware. When the power estimation tool is used to estimate where most of the power dissipated it was established that the filtering and decimation processor (which comes right after the analog-to-digital conversion) consumes most power in the digital part of the GNSS receiver. This led

to the research being focused on the filtering and decimation process. The proposed alternative method greatly reduces the power dissipation as well as the computational complexity without any performance degradation. The main accomplishments of this research are summarised in the following paragraphs.

In chapter 3, a novel solution is proposed that overcomes the Doppler frequency shift related problem and outperforms the pre-existing solutions in terms of accuracy, computational complexity and power dissipation.

During the research, it was necessary to investigate where most of the power was dissipated in a GNSS receiver. In order to be able to achieve this, a power estimation tool was developed and described in chapter 4. This also provides the area utilisation of a digital circuit without designing the actual circuit. This enabled the most expensive sub-systems in terms of power computation to visualise the impact of different design choices for these sub-systems.

The power estimation tool revealed that most of the power was dissipated at the decimation and filtering part of the processing chain. Therefore chapter 5 reported on the details of the study of various decimation and filter techniques for the GNSS receivers with their characteristics, their hardware implementation, power consumption and their area utilisation. Then it proposed various suitable methods that greatly reduced the power dissipation and the computational complexity of this part of the GNSS receiver. By comparing various filter's power dissipation and area utilisation, it can be concluded that implementing the IIR filters using polyphase decomposition

method and using 2nd order decimation ratio where the IIR filters were deployed had the least power consumption.

By measuring the positioning performance on hardware with real-time GPS signals the effects on positioning performance of the various decimator designs were assessed. The effect on the pseudorange estimate was also assessed with artificial GPS signals containing real navigation data. The signals were generated with range of Doppler frequencies in order to assess the positioning performance over the full range of Doppler offsets in chapter 6. The study described in chapter 6, concluded that the use of non-linear phase IIR filters does not deleteriously effect the positioning performance when a GPS signal was being tracked. However, for GLONASS signals, it was discovered that non-linear phase IIR filters have a negative impact on the GLONASS receiver positioning performance. The pseudorange measurements differed by up to 200 metres when non-linear phase IIR filters were used. Various methods were proposed that can easily be deployed which makes it possible to use reduced complexity IIR filters, as opposed to power and area hungry FIR filters, which mitigates the non-linearity effect of the IIR filters. The proposed methods were assessed in terms of their effectiveness on the filter's phase non-linearity and their computational efficiency. The results has shown that the best method, both in terms of performance and computational efficiency, was to use the decimation combination of 6 by 2 by 2 with minimum-phase IIR filters with a piecewise linear approximation to mitigate the IIR filter's non-linear phase characteristic.

Chapter 7 showed a low–frequency implementation model of a decimation process and it detailed how the required filters are implemented that enabled minimum hardware

usage as well as the lowest power consumption possible.

8.2 Future Work

The results and conclusion of this study could be used to implement a self-contained GNSS receiver processor with at least 94% power reduction in the decimation and filtering part.

It would also be necessary to investigate the impact of digital filters stopband attenuation on the position accuracy. Therefore the experiment could be repeated with higher and lower stopband attenuations and establish the effects on the overall positional accuracy.

Due to the time limitation, the research considered only GPS L1 C/A and GLONASS L1 signals which use BPSK modulation scheme. In future, the study undertaken can be extended to consider GNSS signals that uses BOC modulation scheme such as Galileo, modernised GPS, COMPASS and other emerging GNSS systems which have wider bandwidth than currently available GNSS signals.

Although the navigation data used in the GLONASS pseudorange measurements were extracted from real signals, rest of the GLONASS signal had to be created artificially. This is because GLONASS signal with range of carrier Doppler frequencies were required for the experiment. Also the positional accuracy was assessed in terms of pseudorange measurements. In the future the experiment can be repeated with real-time real world signals for GLONASS in order to establish the overall positional accuracy.

The experiments for GPS L1 C/A signals were carried out from a fixed location with a fixed point antenna. In the future, the experiment can be repeated with more extensive field trials in order to establish the effects of designed filters phase non-linearity on GPS L1 C/A signal.

References

[1] Borre, K., et al.;. *A Software Defined GPS and Galileo Receiver: A Single Frequency Approach*. Boston: Birkhäuser, 2007.

[2] Kewen S.; Presti, L.L.;. A differential post detection technique for two steps GNSS signal acquisition algorithm. In *Position Location and Navigation Symposium (PLANS), 2010 IEEE/ION*, pages 752–764, May 2010.

[3] Ucar, A.; Adane, Y.; Bardak, B.; Paparo, C.; Berry, R.; Kale, I.;. A Chip Scale Atomic Clock Driven Receiver for Multi-Constellation GNSS. *Journal of Navigation*, 66:449–464, 5 2013. ISSN 1469-7785.

[4] Ledvina, B.M.; Powell, S.P.; Kintner, P.M.; Psiaki, M.L.;. A 12-Channel Real-Time GPS L1 Software Receiver. In *Proceedings of the 2003 National Technical Meeting of The Institute of Navigation, Anaheim, CA*, pages 767–782, January 2003.

[5] Akos, D. M.; Ene, A.; Thor, J.;. A Prototyping Platform for Multi-Frequency GNSS Receivers. *Proceedings of the ION GPS/GNSS Conference*, pages 117–128, 2003.

[6] Weiler, R. M.;. *Architectures and Techniques for Improved Receiver Performance with Wideband Navigation Signals*. PhD Thesis, University of Surrey, July 2009.

[7] IGS. International GNSS Service [Online] Available at: . http://igscb.jpl.nasa.gov/, [Accessed 14 May 2013].

[8] Doberstein, D.;. *Fundamentals of GPS Receiver: A Hardware Approach*. New York: Springer, 2012.

[9] Federal Space Agency. Information-analytical Center [Online] Available at: . http://www.glonass-center.ru/en/GLONASS/, [Accessed 17 May 2013].

[10] SPACE NEWS. European Commission Report Shines Harsh Light on Galileo [Online] Available at: . http://www.spacenews.com/article/galileo-assessment-pulls-no-punches#.UfJghJz3PNo, [Accessed 26 July 2013].

[11] CHINA'S MILITARY. Beidou satellite navigation system to cover whole world in 2020 [Online] Available at: . http://eng.chinamil.com.cn/news-channels/china-military-news/2010-05/20/content_4222569.htm, [Accessed 10 June 2013].

[12] Kaplan, E.D.; Hegarty, C.J.;. *Understanding GPS: Principles and Applications*. Boston: Artech House, 2nd edition, 2006.

[13] Simon, M., et. al.;. *Spread Spectrum Communications Handbook*. New-York:McGraw-Hill, 1994.

[14] Jack K. Holmes. *Spread Spectrum Systems for GNSS and Wireless Communications*. Artech House, 2007.

[15] Peterson, R. L.; Ziemer, R. E.; Borth, D. E.;. *Introduction to Spread-Spectrum Communications*. New Jersey: Prentice Hall, 1995.

[16] Gold, R.;. Optimal Binary Sequences for Spectrum Multiplexing. *IEEE Trans. on Information Theory*, 13(4):619–621, 1967.

[17] *Navstar GPS Space Segment/Navigation User Interfaces*. IS-GPS-200G, 5 September 2012.

[18] Misra, P.; Enge, P.;. *Global Positioning System: Signals, Measurements, and Performance*. Ganga-Jamuna Press, 2nd edition, 2006.

[19] Betz, J.;. Binary Offset Carrier Modulations for Radionavigation. *Journal of The Institute of Navigation*, 48(4), 2001-2002.

[20] Fontana, R.D.; Cheung, W.; Novak, P.M.; Stansell, T.A.;. The New L2 Civil Signal. In *Proceedings of the ION GPS 2001*, pages 617–631, Sep 2001.

[21] European GNSS Agency. Galileo Is The European Global Satellite-Based Navigation System [Online] Available at: . http://www.gsa.europa.eu/galileo-0, [Accessed 09 April 2013].

[22] *European GNSS (Galileo) Open Service Signal In Space Interface Control Document*, September 2010.

[23] *Galileo Mission High Level Definition*, 23 September 2002.

[24] *Galileo: Secure satellite navigation for emergency and security services*, 8 October 2010.

[25] *GLONASS Interface Control Document Navigational Radiosignal in bands L1, L2.* ICD-GLONASS-5.1, 2012.

[26] Hofmann-Wellenhof, B.; Lichtenegger, H.; Wasle, E.;. *GNSS: Global Navigation Satellite Systems: GPS, GLONASS, Galileo and More.* Springer, 2008.

[27] El-Rabbany, A.;. *Introduction to GPS: The Global Positioning System.* Boston: Artech House, 2002.

[28] Akos, D.M.; Stockmaster, M.; Tsui, J.B.Y.; Caschera, J.;. Direct bandpass sampling of multiple distinct RF signals. *IEEE Transactions on Communications*, 47(7):983–988, Jul 1999.

[29] Ramakrishnan, S.; Xingxin, G.; Lorenzo, D.; Walter, T.; Enge, P.; Akos, D.;. Design and Analysis of Reconfigurable Embedded GNSS Receivers using Model-Based Design Tools. In *Proceedings of the 21st International Technical Meeting of the Satellite Division of The Institute of Navigation (ION GNSS 2008)*, 2008.

[30] Brown, A.; Wolt, B.;. Digital L-band receiver architecture with direct RF sampling. In *IEEE Position Location and Navigation Symposium* , pages 209–216, April 1994.

[31] Crochiere, R. E.; and Rabiner, L. R.;. *Multirate Digital Signal Processing.* New Jersey:Prentice Hall, 1983.

[32] Vaidyanathan, P.P.;. *Multirate Systems and Filter Banks.* New Jersey:Prentice Hall, 1993.

[33] Patel, V.; Shukla, P.;. Faster methods for GPS signal acquisition in frequency domain. In *Emerging Trends in Networks and Computer Communications (ETNCC), 2011 International Conference on*, pages 84–88, April 2011.

[34] van Nee, D.J.R.; Coenen, AJ.R.M.;. *Electronics Letters, title=*.

[35] Molino, A.; Girau, G.; Nicola, M.; Fantino, M.; Pini, M.;. Evaluation of a FFT-Based Acquisition in Real Time Hardware and Software GNSS Receivers. In *IEEE 10th International Symposium on Spread Spectrum Techniques and Applications, ISSSTA '08*, pages 32–36, Aug 2008.

[36] Babu, S.R.; Selvam, P.; Rao, G.S.; Wang, J.;. Optimization of GPS L1 acquisition using Radix-4 FFT. In *2011 International Conference on Recent Trends in Information Technology (ICRTIT)*, pages 875–879, June 2011.

[37] Yuying Zheng. A software-based frequency domain parallel acquisition algorithm for GPS signal. In *2010 International Conference on Anti-Counterfeiting Security and Identification in Communication (ASID)*, pages 298–301, July 2010.

[38] Su Cho, Y.; Kim, B.; Yun Cho, S.; Choi, W.;. The effect on tracking loop performance when using the efficient search method for fast fine frequency acquisition. In *International Conference on Control, Automation and Systems, ICCAS '07.* , pages 517–522, Oct 2007.

[39] Parkinson, B. W.; Spilker, J. J. Jr;. *Global Positioning System: Theory and Application, Volume 1.* American Institue of Astronautics and aeronautics, June 1996.

[40] Best, R. E.;. *Phase-Locked Loops: Theory, Design and Applications*. New York: McGraw-Hill, 1997.

[41] Tsui, J.;. *Fundamentals of Global Positioning System Receivers: A Software Approach*. New York: John Wiley & Sons, 2000.

[42] Cetinsel, S.; Morling, R.C.S.; and Kale, I.;. A comparative study of a low doppler shift in a carrier tracking loop for GPS. In *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 220–223, 2012.

[43] Norsworthy, S. R.; Schreier, R.; Temes, G. C.; . *Delta-sigma data converters*. New York: IEEE Press, 1997.

[44] Cherry, J.;. *Theory, Practice, and Fundamental Performance Limits of High-Speed Data Conversion Using Continuous- Time Delta-Sigma Modulators*. PhD Thesis, Carleton University, Canada, November 1998.

[45] Ismaeel, A. A.; Breuer, M. A.;. The probability of error detection in sequential circuits using random test vectors. *Journal of Electronic Testing*, 1:245–256, January 1991.

[46] Hachtel, G. D.; Macii, E. ; Pardo, A.; Somenzi, F.;. Probabilistic analysis of large nite state machines. In *31st ACM/IEEE Design Automation Conference*, pages 270–275, June 1994.

[47] Monteiro, J.; Devadas, S.;. A methodology for efficient estimation of switching activity in sequential logic circuits. In *31st ACM/IEEE Design Automation Conference*, pages 12–17, June 1994.

[48] Baker, J. R.;. *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2008.

[49] Panda, P.R. et al.;. *Power-efficient System Design*. Springer, 2010.

[50] *TSMC* 0.18μm *Process 1.8-Volt SAGE-X*^{TM} *Standard Cell Library Databook*. Artisan Components, April 2000.

[51] Volder, J. E.;. The CORDIC Trigonometric Computing Technique. *IRE Transactions on Electronic Computers*, EC-8(3):330–334, Sept 1959.

[52] Kuhlmann, M.; Parhi, K.K.;. A high-speed CORDIC algorithm and architecture for DSP applications. In *1999 IEEE Workshop on Signal Processing Systems, SiPS 99.* , pages 732–741, 1999.

[53] Orfanidis, S. J.;. *Introduction to Signal Processing*. Prentice Hall, 2010.

[54] Antoniou, A.;. *Digital Signal Processing: Signals, Systems, and Filters*. McGraw-Hill Education, 2006.

[55] Lyons, R.;. *Understanding Digital Signal Processing*. Prentice Hall, 2001.

[56] Oppenheim, Alan V.; Schafer, Ronald W.; Buck, John R.;. *Discrete-Time Signal Processing*. Prentice Hall, 2nd edition, 1999.

[57] Proakis, J. G.; Manolakis D. G.;. *Digital Signal Processing–Principles, Algorithms and Applications*. Prentice Hall, 1995.

[58] Hogenauer, E.;. An economical class of digital filters for decimation and interpolation. *Acoustics, Speech and Signal Processing, IEEE Transactions on*, 29(2):155–162, Apr 1981.

[59] Saramaki, T.; Ritoniemi, T.;. A modified comb filter structure for decimation. In *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, volume 4, pages 2353–2356 vol.4, Jun 1997.

[60] Morling, R. C. S.; Kale, I.; Tsang, C.W.; Morris, S.J.; Hague, G.; Foran, C.;. The design of a sigma-delta codec for mobile telephone applications. In *Second International Conference on Advanced A-D and D-A Conversion Techniques and their Applications* , pages 11–17, Jul 1994.

[61] Vaidyanathan, P.P.;. Multirate digital filters, filter banks, polyphase networks, and applications: a tutorial. *Proceedings of the IEEE*, 78(1):56–93, Jan 1990.

[62] Valenzuela, R.A.; Constantinides, A.G.;. Digital signal processing schemes for efficient interpolation and decimation. *IEE Proceedings G Electronic Circuits and Systems*, 130(6):225–235, December 1983.

[63] Harris, F.; M. d'Oreye de Lautremange; Constantinides, A. G.;. Digital Signal Processing With Efficient Polyphase Recursive All-Pass Filters. In *Proceeding of International Conference on Signal Processing*, pages 2192–2195, September 1991.

[64] Krukowski, A.; Kale, I.;. Almost linear-phase polyphase IIR lowpass/highpass filter approach. In *Proceedings of the Fifth International Symposium on Signal Processing and Its Applications (ISSPA '99)*, volume 2, pages 969–972, August 1999.

[65] Krukowski, A.; Morling, R.C.S.; Kale, I.;. Quantization effects in the polyphase N-path IIR structure. *IEEE Transactions on Instrumentation and Measurement*, 51(6):1271–1278, Dec 2002.

[66] Ifeachor, E.; Jervis, B.;. *Digital Signal Processing – A Practical Approach*. Prentice Hall, 2002.

[67] Morling, R. C. S.; Kale, I.;. Dynamic range of allpass filter structures. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, volume 4, pages IV–433–IV–436 vol.4, 2002.

[68] Krukowski, A.; Kale, I.;. *DSP System Design Complexity Reduced IIR Filter Implementation for Practical Applications*. New York: Kluwer Academic Publishers, 2004.

[69] Tom Van Flandern, Univ. of Maryland & Meta Research. What the Global Positioning System Tells Us about Relativity [Online] Available at: . http://metaresearch.org/cosmology/gps-relativity.asp, [Accessed 13 May 2013].

[70] Cetinsel, S.; Morling, R.C.S.; and Kale, I.;. An FPGA based decimation filter processor design for real-time continuous-time Sigma-Delta modulator performance measurement and evaluation. In *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pages 397–400, 29-31 August 2011.

[71] Morling, R. C. S.; Kale, I.; Morris, S.J.; Custode, F.;. DSP engine for ultra-low-power audio applications [codec application]. In *Proceedings of the 2003 International Symposium on Circuits and Systems, ISCAS'03.* , volume 5, pages V–357–V–360 vol.5, May 2003.

Appendix A

Filter Coefficients

This Appendix lists all the coefficients of the filters that are described in Chapter 5.

A.1 Coefficients for FIR Filters

Decimation Ratio: 4 x 3 x 2

Stage 1	Stage 2	Stage 3	
N/A	b = 0.03906250	b = 0.01953125	0.41015625
	0.19921875	0.04296875	0.17187500
	0.29296875	-0.01562500	-0.05468750
	0.29296875	-0.02343750	-0.08984375
	0.19921875	0.00781250	0.00390625
	0.03906250	0.05468750	0.05468750
		0.00390625	0.00781250
		-0.08984375	-0.02343750
		-0.05468750	-0.01562500
		0.17187500	0.04296875
		0.41015625	0.01953125

Decimation Ratio: 6 x 2 x 2

Stage 1	Stage 2	Stage 3	
N/A	b =-0.04687500	b =0.01953125	0.41406250
	0.04296875	0.04296875	0.16796875
	0.19531250	-0.01953125	-0.06640625
	0.33203125	-0.03125000	-0.09765625
	0.33203125	0.00390625	0
	0.19531250	0.04687500	0.04687500
	0.04296875	0	0.00390625
	-0.04687500	-0.09765625	-0.03125000
		-0.06640625	-0.01953125
		0.16796875	0.04296875
		0.41406250	0.01953125

Decimation Ratio: 12 x 2

Stage 1	Stage 2	
N/A	b =0.02343750	0.42968750
	0.04296875	0.17968750
	-0.01953125	-0.06640625
	-0.02734375	-0.10156250
	0.00781250	0
	0.05078125	0.05078125
	0	0.00781250
	-0.10156250	-0.02734375
	-0.06640625	-0.01953125
	0.17968750	0.04296875
	0.42968750	0.02343750

Decimation Ratio: 8 x 3

Stage 1	**Stage 2**		
N/A	b =0.00390625	0.03125000	0.00781250
	0.00781250	0.03125000	-0.01562500
	-0.01562500	0	-0.02343750
	0	-0.04687500	-0.01171875
	0.00390625	-0.06250000	0.00781250
	0.00781250	-0.01953125	0.01562500
	0.00781250	0.08593750	0.01171875
	0	0.21093750	-0.00390625
	-0.00781250	0.29296875	-0.01171875
	-0.01171875	0.29296875	-0.00781250
	-0.00390625	0.21093750	0
	0.01171875	0.08593750	0.00781250
	0.01562500	-0.01953125	0.00781250
	0.00781250	-0.06250000	0.00390625
	-0.01171875	-0.04687500	0
	-0.02343750	0	-0.01562500
	-0.01562500	0.03125000	0.00781250
	0.00781250	0.03125000	0.00390625

Decimation Ratio: 6 x 4

Stage 1	**Stage 2**		
N/A	b = 0.02343750	-0.03906250	-0.01171875
	-0.00781250	-0.00390625	0.01171875
	-0.01171875	0.05859375	0.02343750
	-0.01953125	0.12500000	0.02343750
	-0.02343750	0.18750000	0.01171875
	-0.01953125	0.22265625	-0.00390625
	-0.00390625	0.22265625	-0.01953125
	0.01171875	0.18750000	-0.02343750
	0.02343750	0.12500000	-0.01953125
	0.02343750	0.05859375	-0.01171875
	0.01171875	-0.00390625	-0.00781250
	-0.01171875	-0.03906250	0.02343750
	-0.03515625	-0.04687500	
	-0.04687500	-0.03515625	

A.2 Coefficients for IIR Filters

Decimation Ratio: 4 x 3 x 2

Stage 1	Stage 2	Stage 3
N/A	at =-0.250	at2 = 0.125000
	ab = 0.500	at3 = 0.656250
	bb =-0.875	ab2 = 0.390625
		ab3 = 0.890625

Decimation Ratio: 6 x 2 x 2

Stage 1	Stage 2	Stage 3
N/A	at0 = 0.125	at2 = 0.125
	ab0 = 0.625	at3 = 0.625
		ab2 = 0.375
		ab3 = 0.875

Decimation Ratio: 12 x 2

Stage 1	Stage 2
N/A	at2 = 0.125
	at3 = 0.625
	ab2 = 0.375
	ab3 = 0.875

Decimation Ratio: 8 x 3

Stage 1	Stage 2
N/A	at = 0.5000
	bt =-1.0000
	ab = 0.8750
	bb =-1.1875
	db =-0.4375

Decimation Ratio: 6 x 4

Stage 1	Stage 2
N/A	at = 0.59375
	bt =-1.28125
	ab = 0.90625
	bb =-1.46875
	db =-0.56250

A.3 Coefficients for ALP IIR Filters

Decimation Ratio: 4 x 3 x 2

Stage 1	Stage 2	Stage 3
N/A	b1t1coef1 = 0.390625	b1t1coef1 = 0.75000
	b1t1coef2 =-0.109375	b1t1coef2 =-0.28125
	b2t1coef1 = 0.671875	b1t2coef1 = 0.03125
	b2t1coef2 =-0.062500	b2t2coef2 = 0.09375

Decimation Ratio: 6 x 2 x 2

Stage 1	Stage 2	Stage 3
N/A	b1t1coef1 = 0.5000	b1t1coef1 = 0.7500
	b1t1coef2 =-0.0625	b1t2coef1 =-0.2500
		b1t2coef2 = 0.0625

Decimation Ratio: 12 x 2

Stage 1	Stage 2
N/A	b1t1coef1 = 0.828125
	b1t1coef2 =-0.437500
	b1t2coef1 = 0.203125
	b1t2coef2 = 0.093750

Decimation Ratio: 8 x 3

Stage 1	Stage 2
N/A	b1t1coef1 = 0.84375
	b1t1coef2 =-0.62500
	b1t2coef1 = 0.40625
	b1t2coef2 = 0.71875
	b1t2coef3 = 0.40625
	b1t2coef4 =-0.59375
	b2t1coef1 = 0.93750
	b2t1coef2 =-0.46875
	b2t2coef1 = 0.28125
	b2t2coef2 = 0.65625
	b2t2coef3 = 0.25000
	b2t2coef4 =-0.43750

Decimation Ratio: 6 x 4

Stage 1	Stage 2
N/A	b1t1coef1 = 0.484375
	b1t1coef2 =-0.250000
	b2t1coef1 = 0.687500
	b2t1coef2 =-0.203125
	b3t1coef1 = 0.843750
	b3t1coef2 =-0.109375